United States Patent [19]

Oguchi et al.

[11] **4,071,905**

[45] **Jan. 31, 1978**

[54] **FULL ADDER/SUBTRACTOR CIRCUIT EMPLOYING EXCLUSIVE OR LOGIC**

[75] Inventors: **Tetsuji Oguchi; Hirokazu Kawai,** both of Tokyo, Japan

[73] Assignee: **Nippon Electric Co., Ltd.,** Tokyo, Japan

[21] Appl. No.: **736,236**

[22] Filed: **Oct. 27, 1976**

[30] **Foreign Application Priority Data**

Oct. 31, 1975 Japan 50-130534

[51] **Int. Cl.²** **G06F 7/50**

[52] **U.S. Cl.** **364/784**

[58] **Field of Search** 235/176, 175

[56] **References Cited**

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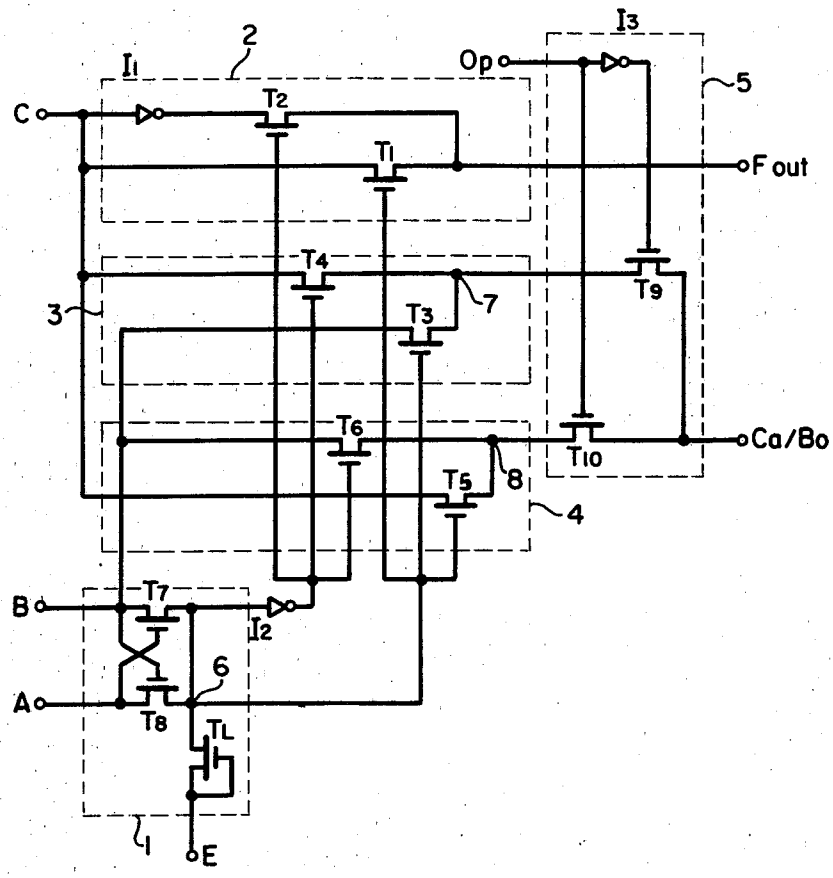
3,843,876	10/1974	Fett et al.	235/175
3,919,536	11/1975	Cochran et al.	235/176 X
3,932,734	1/1976	Parsons	235/175

Primary Examiner—David H. Malzahn

[57] **ABSTRACT**

A binary full adder/subtractor circuit includes an exclusive OR gate operating upon augend/minuend and addend/subtrahend binary input signals. The sum/difference output from the circuit is the carry/borrow input signal or its inverse depending upon the output state of the exclusive OR gate. The carry/borrow output of the circuit comprises either the carry/borrow input or the addend/subtrahend input, as determined by the output of the exclusive OR gate and by an operation (sum/difference) specifying input signal.

9 Claims, 2 Drawing Figures



United States Patent [19]

Oguchi

[11] **4,356,482**

[45] **Oct. 26, 1982**

[54] **IMAGE PATTERN CONTROL SYSTEM**

[75] Inventor: **Tetsuji Oguchi**, Tokyo, Japan

[73] Assignee: **Nippon Electric Co., Ltd.**, Tokyo, Japan

[21] Appl. No.: **155,378**

[22] Filed: **Jun. 2, 1980**

[30] **Foreign Application Priority Data**

Jun. 5, 1979 [JP] Japan 54-70341

[51] **Int. Cl.**[3] **G09G 1/16**; G06F 3/14

[52] **U.S. Cl.** **340/731**; 340/744; 340/799; 364/200

[58] **Field of Search** ..... 340/731, 798, 799; 364/200 MS File

[56] **References Cited**

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Hewlett-Packard Journal, Jan. 1978, vol. 29, No. 5, 24 pp.

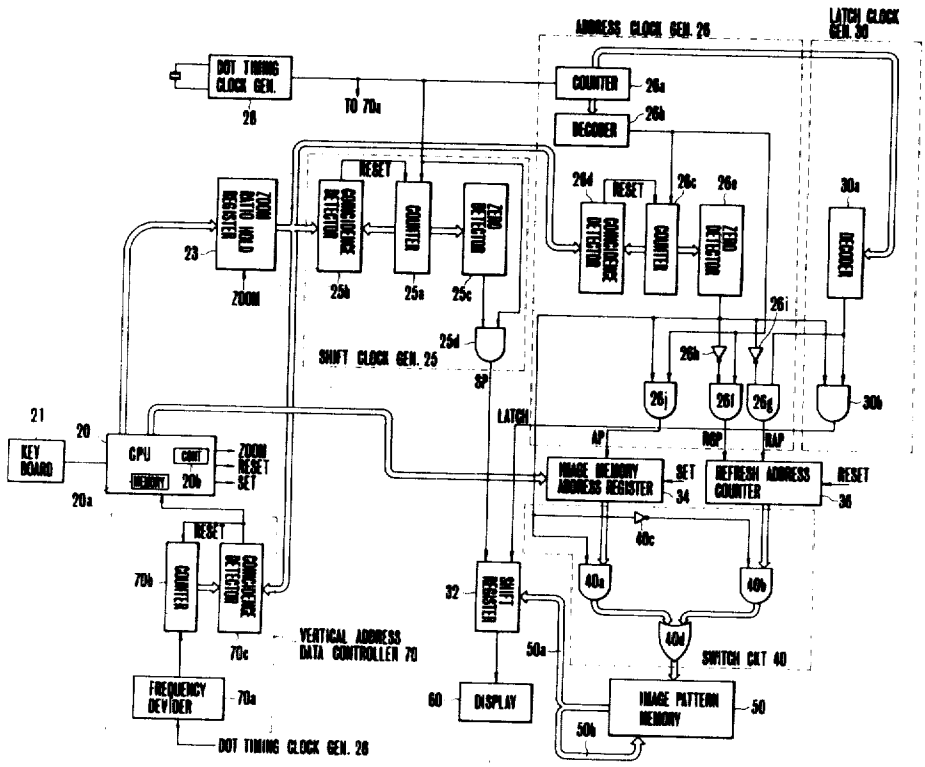
Primary Examiner—David L. Trafton

Attorney, Agent, or Firm—Townsend and Townsend

[57] **ABSTRACT**

An image pattern control system of the type having a dynamic memory which operates during a first period to read and rewrite the contents of memory according to address data sent from an address register and to refresh stored data according to the output of a refresh counter during a subsequent second period. The first and second periods are switched according to the output of a zoom ratio hold register.

9 Claims, 8 Drawing Figures



United States Patent [19]

Oguchi

[11] **Patent Number: 4,459,676**

[45] **Date of Patent: Jul. 10, 1984**

[54] **PICTURE IMAGE PRODUCING APPARATUS**

[75] Inventor: **Tetsuji Oguchi**, Tokyo, Japan

[73] Assignee: **Nippon Electric Co., Ltd.**, Tokyo, Japan

[21] Appl. No.: **275,206**

[22] Filed: **Jun. 18, 1981**

[30] **Foreign Application Priority Data**

Jun. 18, 1980 [JP] Japan 55-82484

[51] **Int. Cl.**[3] **G06F 3/13**; G06F 3/153; G06F 15/20

[52] **U.S. Cl.** **364/521**; 364/520

[58] **Field of Search** 364/520, 521, 522, 720; 340/747

[56] **References Cited**

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Bresenham: A Linear Algorithm for Incremental Digital Display of Circular Arcs. Communications of the A C M, vol. 20, No. 2, Feb. 1977, pp. 100–106.

Pitteway: Algorithm for Drawing Ellipses or Hyperbolae with a Digital Plotter. The Computer Journal, vol. 10, No. 3, Nov. 1967, (British Computer Society–London), pp. 282–289.

Jordan et al.: An Improved Algorithm for the Generation of Nonparametric Curves. IEEE–Transactions on Computers, vol. C–22, No. 12, Dec. 1973, pp. 1052–1060.

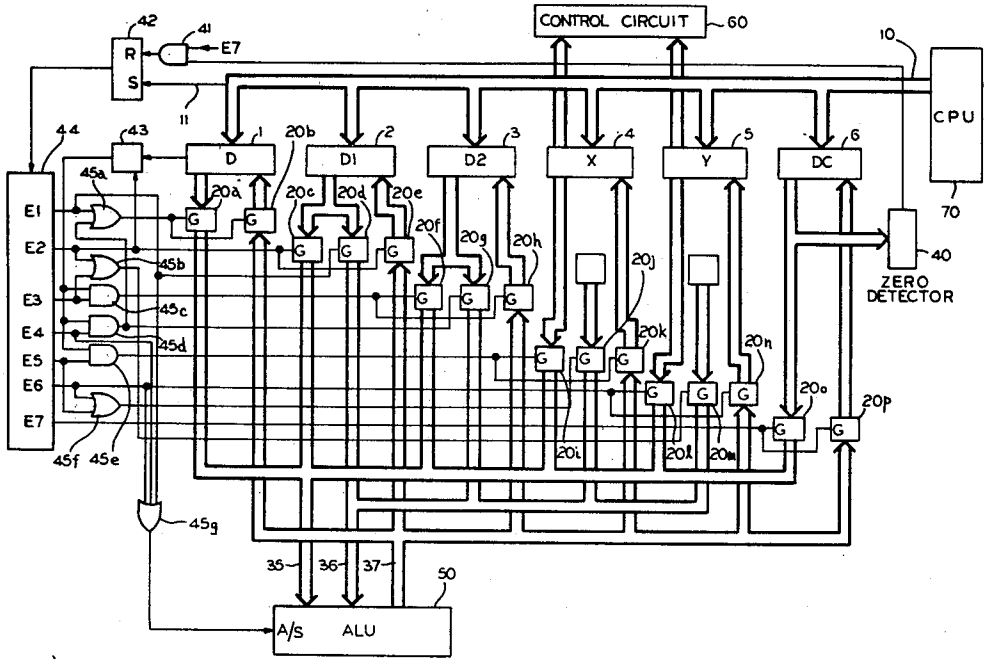
Primary Examiner—Felix D. Gruber

Attorney, Agent, or Firm—Laff, Whitesel, Conte & Saret

[57] **ABSTRACT**

A picture image producing apparatus has a control unit for designating picture image calculation, a display unit for displaying a picture image, and a processing unit for storing standard information used in the picture image calculation. The standard information is x-coordinate data and y-coordinate data of the picture image to be displayed. A first calculator computes a first group information of the picture image, in response to vary the x-coordinate data of the standard information. A second calculation computes second group information of the picture image in response to the varying y-coordinate data of the standard information. The picture image information of the first and second group information is transferred to the display unit.

7 Claims, 15 Drawing Figures



United States Patent [19]

Oguchi

[11] **Patent Number: 4,491,834**

[45] **Date of Patent: Jan. 1, 1985**

[54] **DISPLAY CONTROLLING APPARATUS**

[75] Inventor: **Tetsuji Oguchi**, Tokyo, Japan

[73] Assignee: **Nippon Electric Co., Ltd.**, Tokyo, Japan

[21] Appl. No.: **598,360**

[22] Filed: **Apr. 12, 1984**

Related U.S. Application Data

[63] Continuation of Ser. No. 304,583, Sep. 22, 1981, abandoned.

[30] **Foreign Application Priority Data**

Sep. 22, 1980 [JP] Japan 55-132009

[51] **Int. Cl.**[3] **G09G 1/16**

[52] **U.S. Cl.** **340/726;** 340/723; 340/750

[58] **Field of Search** 340/723, 726, 744, 748, 340/749, 750

[56] **References Cited**

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4,320,395	3/1982	Meissen	340/726
4,375,638	3/1983	O'Keefe	340/726
4,386,410	5/1983	Pandya et al.	340/726

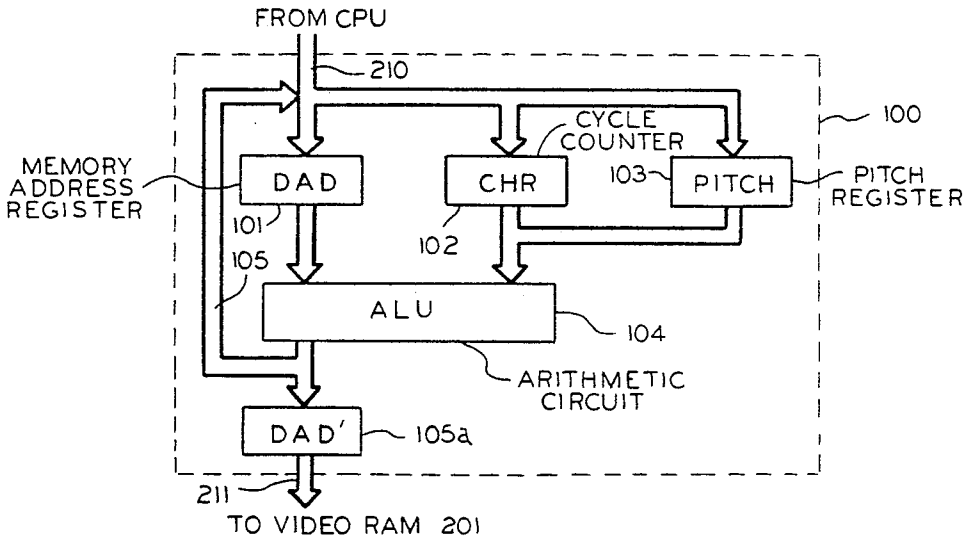
Primary Examiner—Marshall M. Curtis

Attorney, Agent, or Firm—Laff, Whitesel, Conte & Saret

[57] **ABSTRACT**

A display control system has a memory for storing display information and a memory access circuit for reading display information out of this memory. This memory access circuit includes a first circuit in which a memory address is set, a second circuit for sequentially varying the memory address by a predetermined value, and a third circuit for adding to the memory address a preset value, which is different from the predetermined value. A control circuit gives a designation of the addresses to the memory, as a result of the cooperation of the second circuit and the third circuit. The control circuit can be achieved so that display information is read while a memory address may be varied by at least two different means (the second and third circuits above). Thus, it becomes possible to selectively designate a part of a memory region and to display the information of the selected memory region.

4 Claims, 9 Drawing Figures



United States Patent [19]

Oguchi

[11] **Patent Number: 4,545,014**

[45] **Date of Patent: Oct. 1, 1985**

[54] **INFORMATION PROCESSING APPARATUS**

[75] Inventor: **Tetsuji Oguchi**, Tokyo, Japan

[73] Assignee: **Nippon Electric Co., Inc.**, Tokyo, Japan

[21] Appl. No.: **325,086**

[22] Filed: **Nov. 25, 1981**

[30] **Foreign Application Priority Data**

Nov. 26, 1980 [JP] Japan 55-166297

[51] **Int. Cl.**[4] **G06F 9/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** 364/200, 900

[56] **References Cited**

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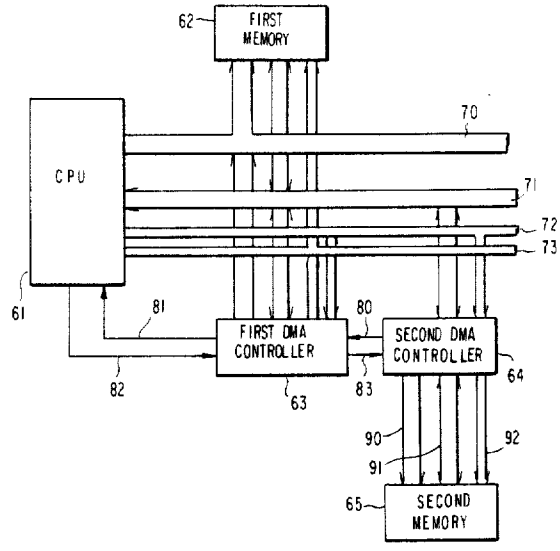
Primary Examiner—Gareth D. Shaw
Assistant Examiner—John G. Mills
Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak, and Seas

[57] **ABSTRACT**

An information processing apparatus employs first and second direct memory access controllers which cooperate during transfer of information between first and second devices, e.g. memories. The first controller controls information transfer from the first memory to the second controller and the second controller transfers the information from its own internal storage to the second memory while simultaneously receiving further information under the control of the first controller. The second controller includes address control circuitry for high speed generation of non-sequential addresses for writing into the second memory.

1 Claim, 8 Drawing Figures



United States Patent [19]

Oguchi

[11] **Patent Number: 4,570,222**

[45] **Date of Patent: Feb. 11, 1986**

[54] **INFORMATION PROCESSOR HAVING INFORMATION CORRECTING FUNCTION**

[75] Inventor: **Tetsuji Oguchi**, Tokyo, Japan

[73] Assignee: **Nippon Electric Co., Ltd.**, Tokyo, Japan

[21] Appl. No.: **529,921**

[22] Filed: **Sep. 6, 1983**

Related U.S. Application Data

[63] Continuation of Ser. No. 206,061, Nov. 12, 1980, abandoned.

[30] **Foreign Application Priority Data**

Nov. 15, 1979 [JP] Japan 54-148031

[51] **Int. Cl.**[4] **G06F 13/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** 364/200, 900; 340/703, 340/717, 709, 723

[56] **References Cited**

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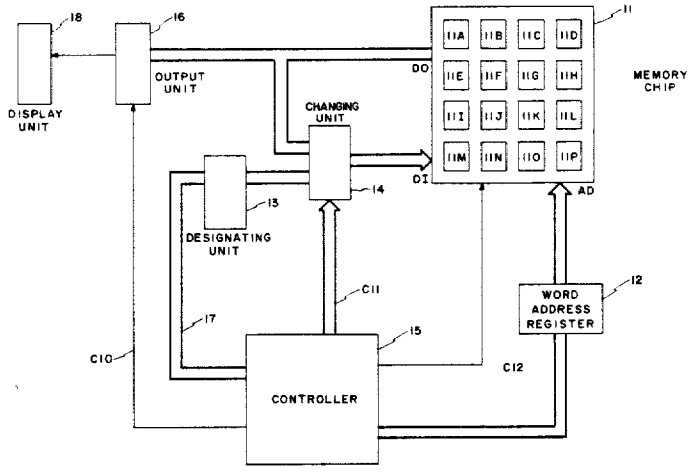
Primary Examiner—Thomas M. Heckler

Attorney, Agent, or Firm—Laff, Whitesel, Conte & Saret

[57] **ABSTRACT**

The invention selectively designates a specific portion of information which is stored in a memory to identify information which is to be corrected. It further enables a correction of only the suitably designated portion. The read out of information having the corrected information is set in a state which is ready for use. Accordingly, it is not necessary to use a bit addressing circuit, as used in the prior art, this simplifying both the circuit design and the wiring. It is also possible to designate more than one arbitrary item of information as portions which are to be corrected and then to correct all designated information simultaneously. Thus, the read out information is corrected at a high speed. In addition, the number of information items which are capable of correction is not limited by unnecessary bit addressing. This enables an increase in the number of memory elements, and makes the system quite useful as a control device for CRT display systems.

8 Claims, 12 Drawing Figures



United States Patent [19]

Oguchi

[11] **Patent Number: 4,870,563**

[45] **Date of Patent: Sep. 26, 1989**

[54] **INFORMATION PROCESSING APPARATUS HAVING A MASK FUNCTION**

[75] Inventor: **Tetsuji Oguchi**, Tokyo, Japan

[73] Assignee: **NEC Corporation**, Tokyo, Japan

[21] Appl. No.: **36,754**

[22] Filed: **Apr. 8, 1987**

[30] **Foreign Application Priority Data**

Apr. 8, 1986 [JP] Japan 61-81709

[51] **Int. Cl.**[4] **G06F 7/10**; G06F 13/00

[52] **U.S. Cl.** **364/200**; 364/252.5; 364/259.7

[58] **Field of Search** 364/200, 900

[56] **References Cited**

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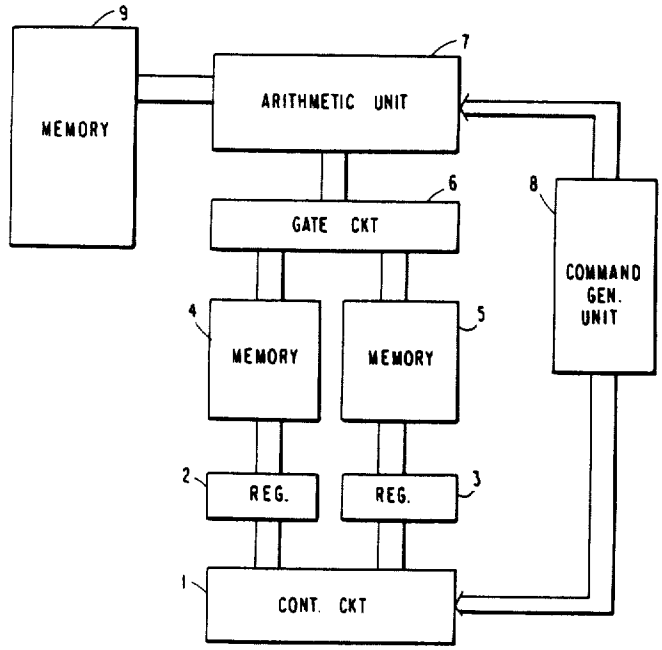
Primary Examiner—Felix D. Gruber

Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak & Seas

[57] **ABSTRACT**

An information processing apparatus having a mask operation includes a first circuit generating a first mask control signal indicating a start bit position of a data to be processed and a second circuit generating a second mask control signal indicating an end bit position of that data. The first mask control signal and the second mask control signal are applied to a gate circuit by which a non-mask signal is produced for a bit or bits from the start bit position to the end bit position and a mask signal is produced for the other bit or bits.

9 Claims, 5 Drawing Sheets



United States Patent [19]

Oguchi

[11] **Patent Number: 4,878,191**

[45] **Date of Patent: Oct. 31, 1989**

[54] **MULTIPLICATION CIRCUIT CAPABLE OF OPERATING AT A HIGH SPEED WITH A SMALL AMOUNT OF HARDWARE**

[75] Inventor: **Tetsuji Oguchi**, Tokyo, Japan

[73] Assignee: **NEC Corporation**, Tokyo, Japan

[21] Appl. No.: **155,771**

[22] Filed: **Feb. 16, 1988**

[30] **Foreign Application Priority Data**

Feb. 13, 1987 [JP] Japan 62-31026

[51] **Int. Cl.**[4] **G06F 7/50**

[52] **U.S. Cl.** **364/759**

[58] **Field of Search** 364/759, 760

[56] **References Cited**

U.S. PATENT DOCUMENTS

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Gerberich et al, "Multiplier/Divider Hardware Design Accelerates Microprocessor Throughput", *Computer Design*, Jun. 1979, pp. 105-112.

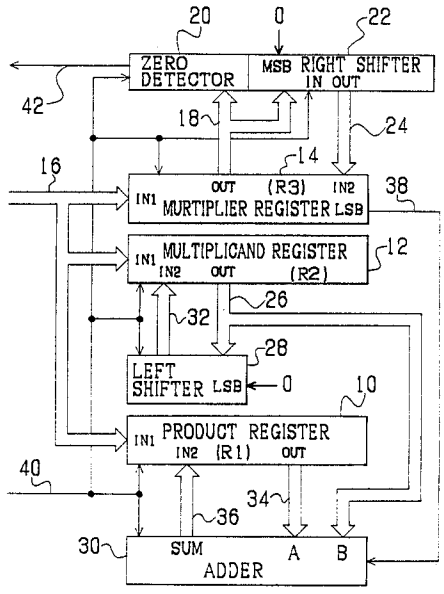
Primary Examiner—David H. Malzahn

Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak & Seas

[57] **ABSTRACT**

A multiplication circuit comprises a zero detector coupled to a multiplier register so as to generate a signal indicative of completion of the multiplication operation when all of predetermined bits of the multiplier register are zero. A right shifter is coupled to the multiplier register so as to shift the input data one bit rightwardly and to put "0" at its most significant bit. The right shifter rewrites the multiplier register with the shifted data having the MSB of "0". Further, a left shifter is coupled to a multiplicand register so as to shift the input data one bit leftwardly and to put "0" at its least significant bit. The left shifter rewrites the multiplicand register with the leftwardly shifted data having the LSB of "0". An adder is coupled to receive a content of a product register and a content of the multiplicand register and to rewrite the product register with the result of an addition between the content of the product register and the content of the multiplicand register when the LSB of the multiplier register is "1".

4 Claims, 3 Drawing Sheets



United States Patent [19]

Oguchi

[11] **Patent Number: 4,943,801**

[45] **Date of Patent: Jul. 24, 1990**

[54] **GRAPHICS DISPLAY CONTROLLER EQUIPPED WITH BOUNDARY SEARCHING CIRCUIT**

[75] Inventor: **Tetsuji Oguchi**, Tokyo, Japan

[73] Assignee: **NEC Corporation**, Tokyo, Japan

[21] Appl. No.: **161,690**

[22] Filed: **Feb. 29, 1988**

[30] **Foreign Application Priority Data**

Feb. 27, 1987 [JP] Japan 62-44840

[51] **Int. Cl.**[5] **G09G 1/00**

[52] **U.S. Cl.** **340/723**; 340/747; 340/799; 382/22; 382/48

[58] **Field of Search** 340/703, 720, 723, 724, 340/728, 747, 798, 799; 358/96; 382/22, 48

[56] **References Cited**

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Simmons et al.; "Polygon Filling in Graphics Display System"; IBM Technical Disclosure Bulletin; vol. 24 No. 1A; Jun. 1981.

Van Wyk; "Clipping to the Boundary of a Circular-Arc Polygon"; Computer Vision, Graphics, and Image Processing; Mar. 1984; pp. 383-392.

Primary Examiner—David K. Moore

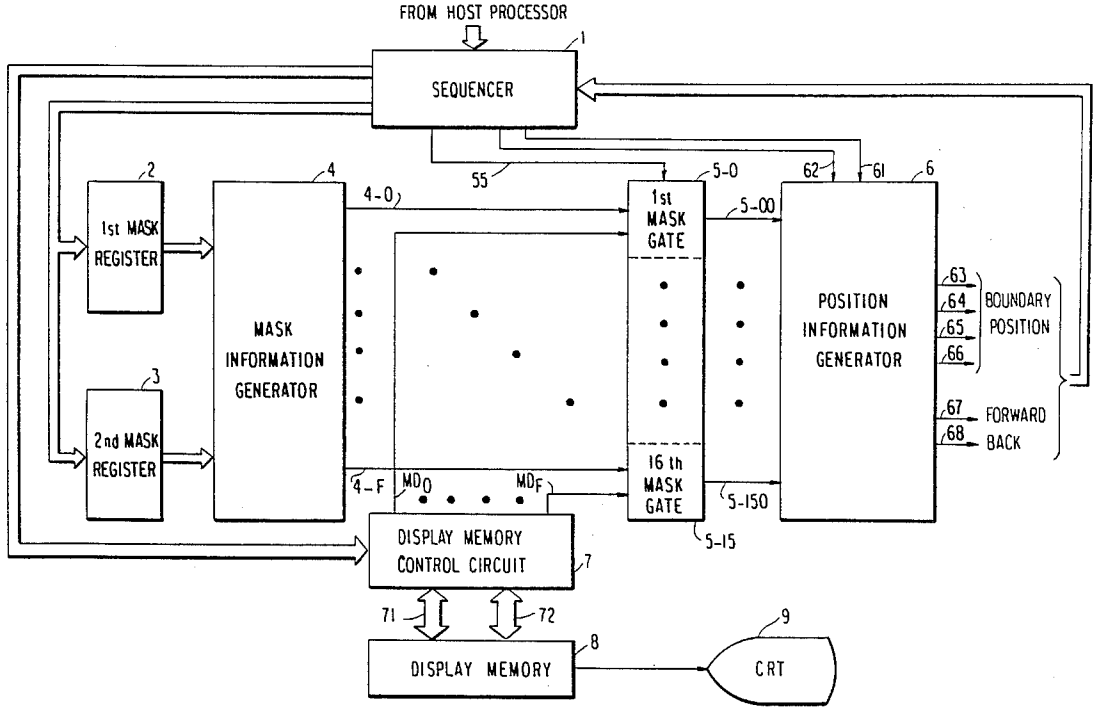
Assistant Examiner—Richard Hjerpe

Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak & Seas

[57] **ABSTRACT**

A graphics display controller equipped with a boundary search circuit is disclosed. There is provided a mask information generator generating mask information consisting of a plurality of bits in response to control data, at least one bit of the mask information taking non-mask data and the remaining bits thereof taking mask data. Each bit data of the mask information is supplied to the associated one of a plurality of mask gates along with the associated bit data of display data of one word read from a display memory. Each of the mask gates outputs the associated bit data of the display data when the associated mask information bit data is the non-mask data. The output data of the mask gates are supplied to a position information generator wherein the position information relative to a position of a bit taking a predetermined logic level is generated.

8 Claims, 9 Drawing Sheets



United States Patent [19]

Johary et al.

[11] **Patent Number: 5,018,076**

[45] **Date of Patent: May 21, 1991**

[54] **METHOD AND CIRCUITRY FOR DUAL PANEL DISPLAYS**

[75] Inventors: **Arun Johary; Tetsuji Oguchi**, both of San Jose, Calif.

[73] Assignee: **Chips and Technologies, Inc.**, San Jose, Calif.

[21] Appl. No.: **245,862**

[22] Filed: **Sep. 16, 1988**

[51] **Int. Cl.**[5] **G06F 15/62**

[52] **U.S. Cl.** **364/518**; 340/716; 340/723; 364/521

[58] **Field of Search** 364/518, 521; 340/721, 340/723, 724, 725, 726, 709, 716, 752, 756; 358/240

[56] **References Cited**

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4,924,432	5/1990	Asai et al.	364/900

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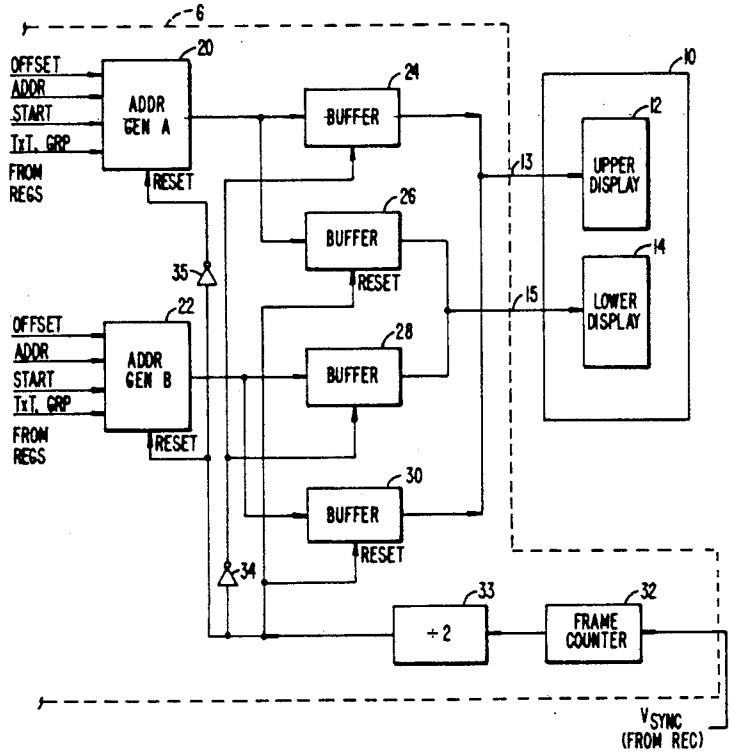
2085257 9/1984 United Kingdom .

Primary Examiner—Heather R. Herndon
Attorney, Agent, or Firm—Townsend and Townsend

[57] **ABSTRACT**

A data processing system includes a video controller and a flat panel display system. The flat panel display system includes first and second flat panel displays adapted so as to appear to be essentially a single display. The video controller includes a first and second address generator for generating first and second address information and a counter for counting vertical sync position to identify alternating first and second display frames. The controller outputs the first address information to drive the first display and the second address information to drive the second display during the first display frames and outputs the second address information to drive the first display and the first address information to drive the second display during the second display frames. The displays are identical and the address generators are identical. The use of dual displays with dual, flip-flopping address generators is more advantageous than using a single address generator to drive two display panels.

24 Claims, 5 Drawing Sheets



US005196839A

United States Patent [19]

Johary et al.

[11] Patent Number: 5,196,839

[45] Date of Patent: Mar. 23, 1993

[54] **GRAY SCALES METHOD AND CIRCUITRY FOR FLAT PANEL GRAPHICS DISPLAY**

[75] Inventors: **Arun Johary; Tetsuji Oguchi**, both of San Jose, Calif.

[73] Assignee: **Chips and Technologies, Inc.**, San Jose, Calif.

[21] Appl. No.: **598,582**

[22] Filed: **Oct. 15, 1990**

Related U.S. Application Data

[63] Continuation of Ser. No. 245,875, Sep. 16, 1988, abandoned.

[51] **Int. Cl.**[5] **G09G 3/20**

[52] **U.S. Cl.** **340/793**; 340/805

[58] **Field of Search** 340/723, 767, 793, 805, 340/812; 358/240, 241, 455, 456, 457, 458, 459

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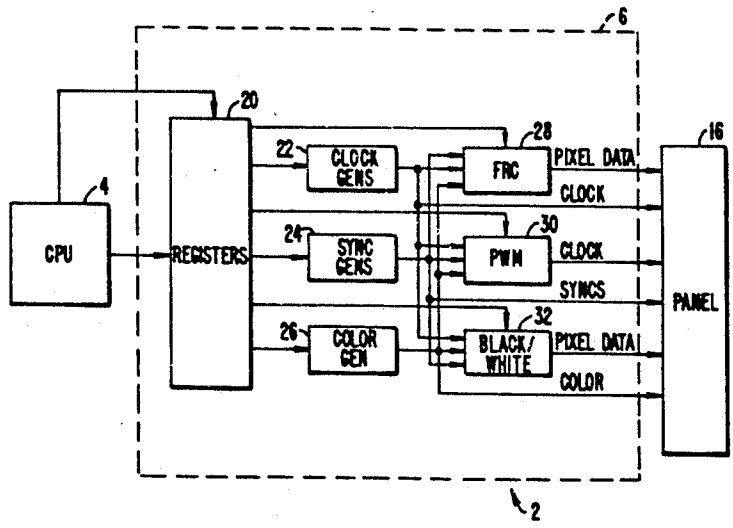
Primary Examiner—Alvin E. Oberley
Assistant Examiner—Richard Hjerpe
Attorney, Agent, or Firm—Townsend and Townsend

[57] **ABSTRACT**

A controller for providing O to N gray scales at a monochrome display. The monochrome display is of the type having an array of pixels energized by a display voltage over time to generate the gray scales. The controller generates a baseline time and uses the baseline time to provide gray scales at the display. In particular, each pixel is energized at least the baseline time for any gray scale above level 0 to reduce flicker in the display. In one embodiment, the baseline time corresponds to a point on the intensity response curve for the display at which the display exhibits a linear intensity response for a given display voltage versus time. In one embodiment, the baseline time is used to generate pixel on/off data to provide gray scales at the display. In yet another embodiment, the baseline time information is used to generate weighted clock information to provide gray scales at the display. In another aspect, the controller includes a plurality of programmable gray scale generators which provide pixel on/off data, weighted clock information, and black/white pixel data to provide gray scales at the display. One of the gray scale generators is selected and programmed depending on the identity of the display device.

6 Claims, 4 Drawing Sheets



US005222212A

United States Patent [19]

Johary et al.

[11] Patent Number: 5,222,212

[45] Date of Patent: Jun. 22, 1993

[54] FAKEOUT METHOD AND CIRCUITRY FOR DISPLAYS

[75] Inventors: **Arun Johary; Tetsuji Oguchi**, both of San Jose, Calif.

[73] Assignee: **Chips and Technologies, Inc.**, San Jose, Calif.

[21] Appl. No.: **614,056**

[22] Filed: **Nov. 13, 1990**

Related U.S. Application Data

[63] Continuation of Ser. No. 245,874, Sep. 16, 1988, abandoned.

[51] **Int. Cl.**[5] **G06F 15/40**; G09G 3/28

[52] **U.S. Cl.** **395/162**; 395/153; 395/154; 340/717; 340/771

[58] **Field of Search** ... 364/200 MS File, 900 MS File, 364/518, 521, 522; 340/758, 785, 771, 716, 717; 395/162, 153, 154

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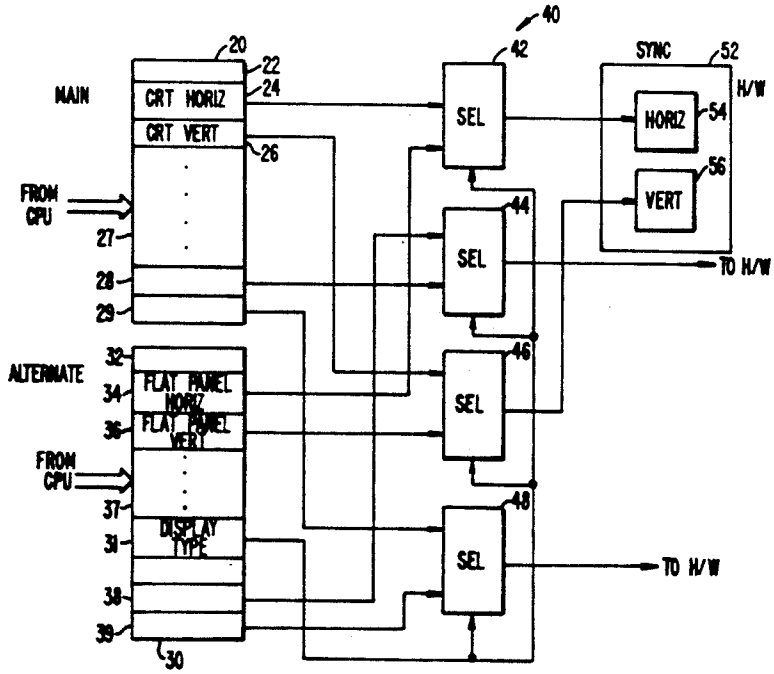
Primary Examiner—Phu K. Nguyen

Attorney, Agent, or Firm—Townsend and Townsend Khourie and Crew

[57] **ABSTRACT**

A video display controller capable of providing video control information for either a flat panel or a CRT display. The controller includes a plurality of main circuits, alternate circuits, select circuits, and a circuit for identifying the display device used in the system. Each main circuit receives information from the processor and generates main video information compatible with a CRT. Each alternate circuit receives information from the processor and generates alternate video information compatible with a flat panel display. Each select circuit receives main and alternate video information and outputs main video information when the display device is a CRT display and the alternate video information when the display device is a flat panel display. In one embodiment, the alternate circuits are programmable registers. In another embodiment, tables are used to program the alternate registers to provide compatibility for a number of possible display devices.

9 Claims, 3 Drawing Sheets



US005285192A

United States Patent [19]

Johary et al.

[11] **Patent Number: 5,285,192**

[45] **Date of Patent: Feb. 8, 1994**

[54] **COMPENSATION METHOD AND CIRCUITRY FOR FLAT PANEL DISPLAY**

[75] Inventors: **Arun Johary; Tetsuji Oguchi**, both of San Jose, Calif.

[73] Assignees: **Chips and Technologies, Inc.**, San Jose, Calif.; **ASCII Corporation**, Tokyo, Japan

[21] Appl. No.: **815,840**

[22] Filed: **Dec. 30, 1991**

Related U.S. Application Data

[63] Continuation of Ser. No. 617,483, Nov. 21, 1990, abandoned, which is a continuation of Ser. No. 245,866, Sep. 16, 1988, abandoned.

[51] **Int. Cl.**[5] **G09G 5/00**

[52] **U.S. Cl.** **345/3**; 345/132

[58] **Field of Search** 340/716, 717, 723, 731, 340/735, 771, 784, 793, 812, 790, 805

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Primary Examiner—Richard Hjerpe
Attorney, Agent, or Firm—Townsend and Townsend Khourie and Crew

[57] **ABSTRACT**

A video controller for a personal computing system. The controller compensates CRT video information to generate a display compatible with a flat panel device. The controller includes registers and logic circuits which compensate CRT address information. The compensated addresses are used to repeat lines of display, insert blank lines between lines of display, center a display, and force font types.

7 Claims, 10 Drawing Sheets