# United States Patent [19]

**Oguchi**

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[54] **MULTIPLICATION CIRCUIT CAPABLE OF OPERATING AT A HIGH SPEED WITH A SMALL AMOUNT OF HARDWARE**


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[51] **Int. Cl.**[4] ..... **G06F 7/50**

[52] **U.S. Cl.** ..... **364/759**

[58] **Field of Search** ..... 364/759, 760



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[57] **ABSTRACT**

A multiplication circuit comprises a zero detector coupled to a multiplier register so as to generate a signal indicative of completion of the multiplication operation when all of predetermined bits of the multiplier register are zero. A right shifter is coupled to the multiplier register so as to shift the input data one bit rightwardly and to put "0" at its most significant bit. The right shifter rewrites the multiplier register with the shifted data having the MSB of "0". Further, a left shifter is coupled to a multiplicand register so as to shift the input data one bit leftwardly and to put "0" at its least significant bit. The left shifter rewrites the multiplicand register with the leftwardly shifted data having the LSB of "0". An adder is coupled to receive a content of a product register and a content of the multiplicand register and to rewrite the product register with the result of an addition between the content of the product register and the content of the multiplicand register when the LSB of the multiplier register is "1".


**4 Claims, 3 Drawing Sheets**