

1. Introduction

ILI9341 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9341 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

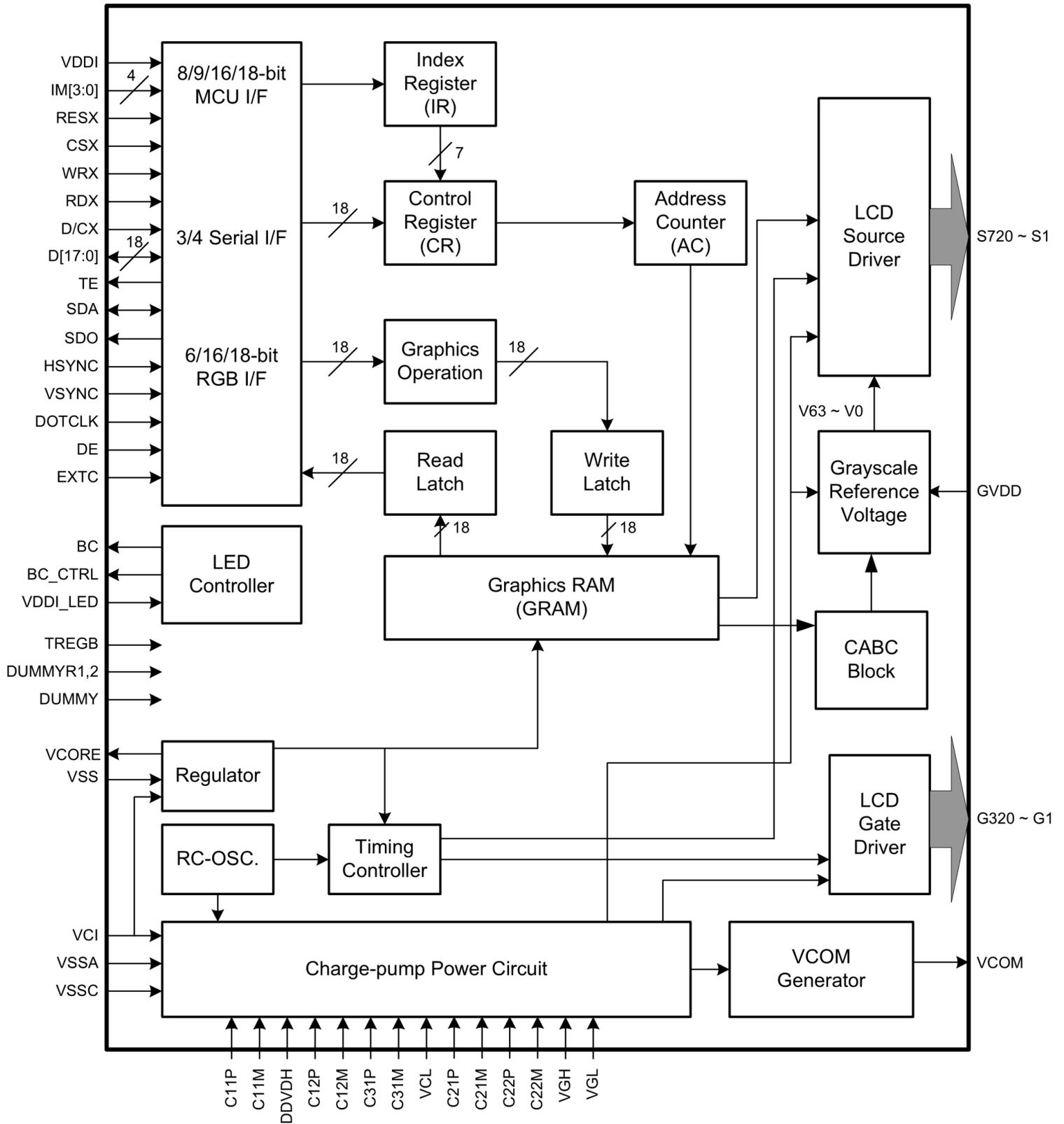
ILI9341 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9341 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9341 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- ◆ Display resolution: [240xRGB](H) x 320(V)
- ◆ Output:
 - 720 source outputs
 - 320 gate outputs
 - Common electrode output (VCOM)
- ◆ a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- ◆ System Interface
 - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080- I /8080- II series MCU
 - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
 - 3-line / 4-line serial interface
- ◆ Display mode:
 - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
 - Reduce color mode (Idle mode ON): 8-color
- ◆ Power saving mode:
 - Sleep mode
- ◆ On chip functions:
 - VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - Line/frame inversion
 - 1 preset Gamma curve with separate RGB Gamma correction
- ◆ Content Adaptive Brightness Control
- ◆ MTP (3 times):
 - 8-bits for ID1, ID2, ID3
 - 7-bits for VCOM adjustment

- ◆ Low -power consumption architecture
 - Low operating power supplies:
 - VDDI = 1.65V ~ 3.3V (logic)
 - VCI = 2.5V ~ 3.3V (analog)
- ◆ LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH - GND = 4.5V ~ 5.8V
 - VCL - GND = -1.5V ~ -2.5V
 - Gate driver output voltage
 - VGH - GND = 10.0V ~ 18.0V
 - VGL - GND = -5.0V ~ -10.0V
 - VGH - VGL \leq 28V
 - VCOM driver output voltage
 - VCOMH = 3.0V ~ (DDVDH - 0.2)V
 - VCOML = (VCL+0.2)V ~ 0V
 - VCOMH - VCOML \leq 6.0V
- ◆ Operate temperature range: -40°C to 85°C
- ◆ a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Pin Descriptions

Power Supply Pins			
Pin Name	I/O	Type	Descriptions
VDDI	I	P	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)
VDDI_LED	I		Power supply for LED driver interface. (1.65 ~ 3.3 V) If LED driver is not used, fix this pin at VDDI.
VCI	I	Analog Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)
Vcore	O	Digital Power	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad
VSS3	I	I/O Ground	System ground level for I/O circuits.
VSS	I	Digital Ground	System ground level for logic blocks
VSSA	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.
VSSC	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise

Interface Logic Signals									
Pin Name	I/O	Type	Descriptions						
IM[3:0]	I	(VDDI/VSS)	- Select the MCU interface mode						
			IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use	
								Register/Content	GRAM
			0	0	0	0	80 MCU 8-bit bus interface I	D[7:0]	D[7:0]
			0	0	0	1	80 MCU 16-bit bus interface I	D[7:0]	D[15:0]
			0	0	1	0	80 MCU 9-bit bus interface I	D[7:0]	D[8:0]
			0	0	1	1	80 MCU 18-bit bus interface I	D[7:0]	D[17:0]
			0	1	0	1	3-wire 9-bit data serial interface I	SDA: In/OUT	
			0	1	1	0	4-wire 8-bit data serial interface I	SDA: In/OUT	
			1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]
			1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]
			1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]
			1	0	1	1	80 MCU 9-bit bus interface II	D[17:10]	D[17:9]
			1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Out	
1	1	1	0	4-wire 8-bit data serial interface II	SDI: In SDO: Out				
MPU Parallel interface bus and serial interface select									
If use RGB Interface must select serial interface.									
* : Fix this pin at VDDI or VSS.									

RESX	I	MCU (VDDI/VSS)	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
EXTC	I	MCU (VDDI/VSS)	Extended command set enable. Low: extended command set is discarded. High: extended command set is accepted. Please connect EXTC to VDDI to read/write extended registers (RB0h~RCFh, RE0h~RFFh)
CSX	I	MCU (VDDI/VSS)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. * note1,2
D/CX (SCL)	I	MCU (VDDI/VSS)	This pin is used to select "Data or Command" in the parallel interface or 4-wire 8-bit serial data interface. When DCX = '1', data is selected. When DCX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to VDDI or VSS.
RDX	I	MCU (VDDI/VSS)	8080- I /8080- II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use.
WRX (D/CX)	I	MCU (VDDI/VSS)	- 8080- I /8080- II system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. Fix to VDDI level when not in use.
D[17:0]	I/O	MCU (VDDI/VSS)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to VSS level when not in use
SDI/SDA	I/O	MCU (VDDI/VSS)	When IM[3] : Low, Serial in/out signal. When IM[3] : High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or VSS.
SDO	O	MCU (VDDI/VSS)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (VDDI/VSS)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (VDDI/VSS)	Dot clock signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
VSYNC	I	MCU (VDDI/VSS)	Frame synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
HSYNC	I	MCU (VDDI/VSS)	Line synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
DE	I	MCU (VDDI/VSS)	Data enable signal for RGB interface operation. Fix to VDDI or VSS level when not in use.

Note.

1. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.
2. When CSX='1', there is no influence to the parallel and serial interface.

LCD Driver Input/Output Pins

Pin Name	I/O	Type	Descriptions
S720~S1	O	Source	Source output signals.. <i>Leave the pin to open when not in use.</i>
G320~G1	O	Gate	Gate output signals. <i>Leave the pin to open when not in use.</i>
DDVDH	O	Power Stabilizing capacitor	Output voltage of 1st step up circuit (2 x VCI). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.
VGH	O	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
VGL	O	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
VCL	0	Power Stabilizing capacitor	Power supply for VCOML. VCL = 0~ - VCI Connect this pad with a stabilizing capacitor.
C11P, C11M C12P, C12M	P	Stabilizing capacitor	Connect the charge-pumping capacitor for generating DDVDH level.
C21P, C21M C22P, C22M	P	Stabilizing capacitor	Connect the charge-pumping capacitor for generating VGH, VGL level.
GVDD	O		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VCOM	O		Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.
LEDPWM	O		Output pin for PWM (Pulse Width Modulation) signal of LED driving. If not used, open this pad.
LEDON	O		Output pin for enabling LED driving. If not used, open this pad.

Test Pins

Pin Name	I/O	Type	Descriptions
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
INT_TEST1 INT_TEST2	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.

Liquid crystal power supply specifications Table

No.	Item	Description
1	TFT Source Driver	720 pins (240 x RGB)
2	TFT Gate Driver	320 pins
3	TFT Display's Capacitor Structure	Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1 ~ S720
		G1 ~ G320
		VCOM
5	Input Voltage	V0 ~ V63 grayscales
		VGH - VGL
		VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	VDDI
		VCI
		1.65V ~ 3.30V
		2.50V ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH
		VGH
		VGL
		VCL
		VGH - VGL
		4.5V ~ 5.8V
		10.0V ~ 18.0V
		-5.0V ~ -10.0V
		-1.5V ~ -2.5V
		Max. 28.0V
7	Internal Step-up Circuits	DDVDH
		VGH
		VGL
		VCL
		VCI x2,
		VCI x6, x7
		VCI x-3, x-4,
		VCI x-1

6. Block Function Description

MCU System Interface

ILI9341 provides four kinds of MCU system interface with 8080- I /8080- II series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface II	SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,D/CX,SDO, CSX	

In 8080- I /8080- II series parallel interface, the registers are accessed by the D[17:0] data pins.

8080- I Series				8080- II Series				Operation
CSX	D/CX	RDX	WRX	CSX	D/CX	RDX	WRX	
"L"	"L"	"H"		"L"	"L"	"H"		Write command
"L"	"H"		"H"	"L"	"H"		"H"	Read parameter
"L"	"H"	"H"		"L"	"H"	"H"		Write parameter

Parallel RGB Interface

ILI9341 also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 240(RGB) x320 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9341 can display maximum 262,144 colors.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as GVDD, VGH, VGL and VCOM for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9341 incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 720-output source driver (S1~S720), 320-output gate driver (G1~G320), and VCOM signal.

7. Function Description

7.1. MCU interfaces

ILI9341 provides the 8-/9-/16-/18-bit parallel system interface for 8080- I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit format per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0], WRX, RDX, CSX, D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0], WRX, RDX, CSX, D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0], WRX, RDX, CSX, D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0], WRX, RDX, CSX, D/CX
0	1	0	1	3-wire 9-bit data serial interface I	SCL, SDA, CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL, SDA, D/CX, CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1], WRX, RDX, CSX, D/CX
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10], WRX, RDX, CSX, D/CX
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0], WRX, RDX, CSX, D/CX
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9], WRX, RDX, CSX, D/CX
1	1	0	1	3-wire 9-bit data serial interface II	SCL, SDI, SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL, SDI, D/CX, SDO, CSX	

7.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface	"L"	-		Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	"L"	'H/L"		Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	"L"	-		Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	"L"	'H/L"		Read/Write command, parameter or display data.

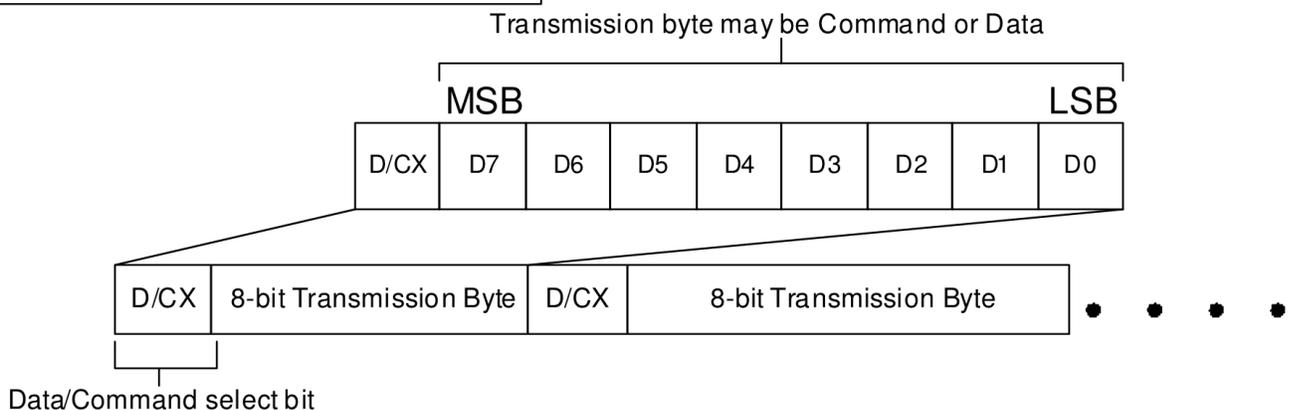
ILI9341 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9341. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.9. Write Cycle Sequence

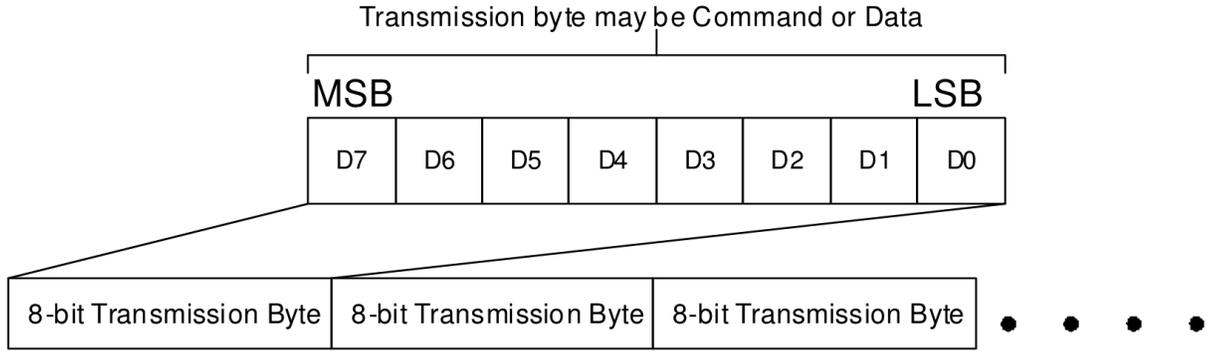
The write mode of the interface means that host writes commands or data to ILI9341. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to ILI9341 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Data Format for 3-line Serial Interface

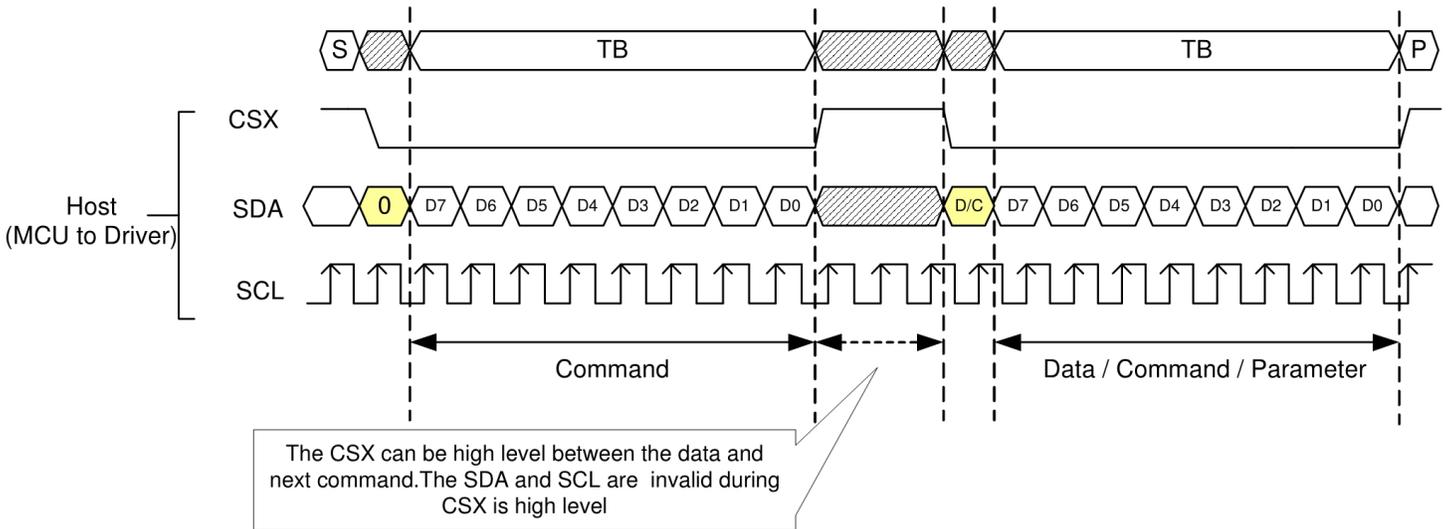


Data Format for 4-line Serial Interface

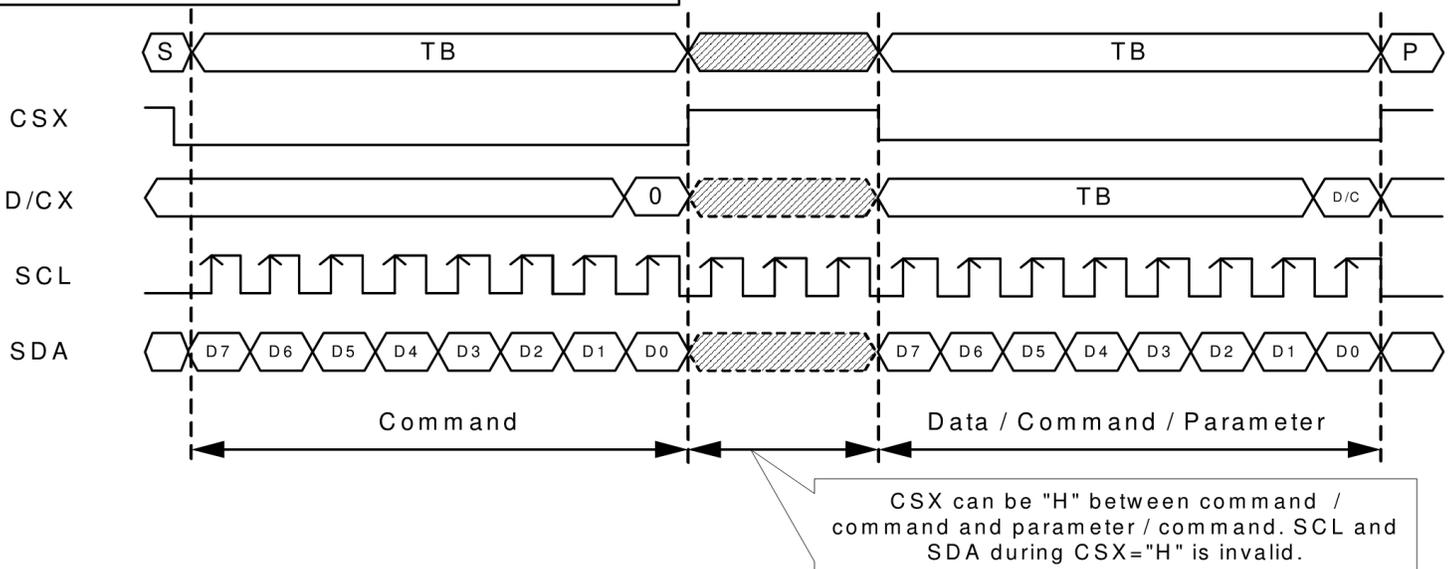


Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9341 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

3-line Serial Interface Protocol



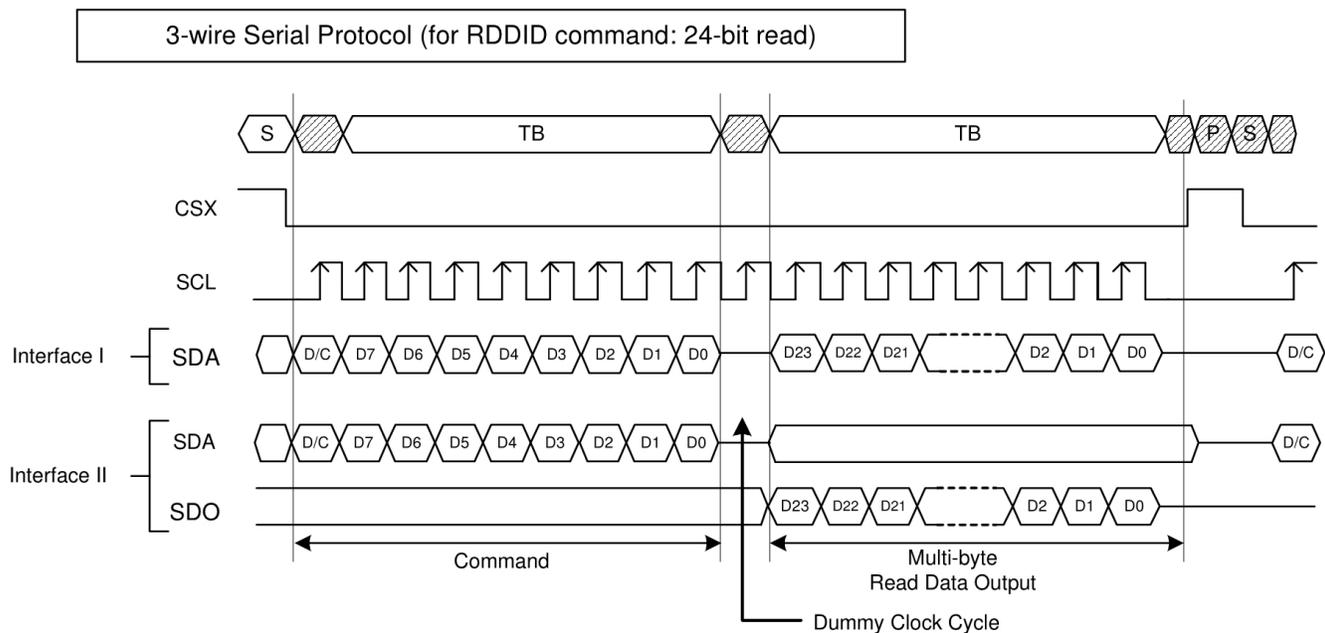
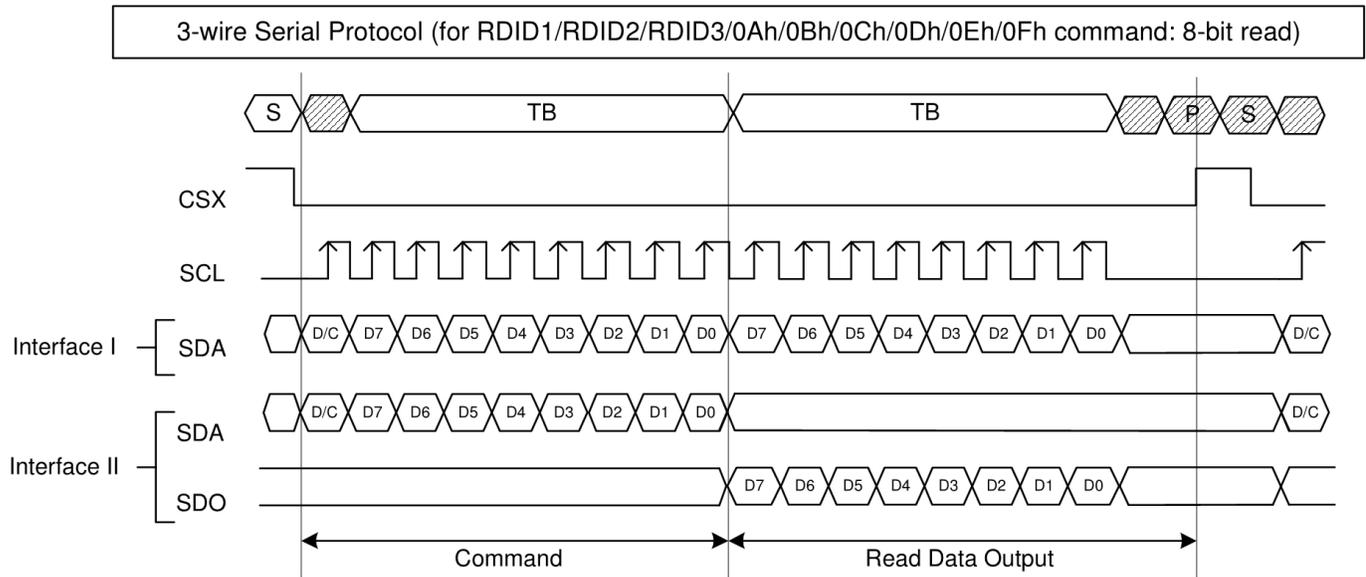
4-line Serial Interface Protocol



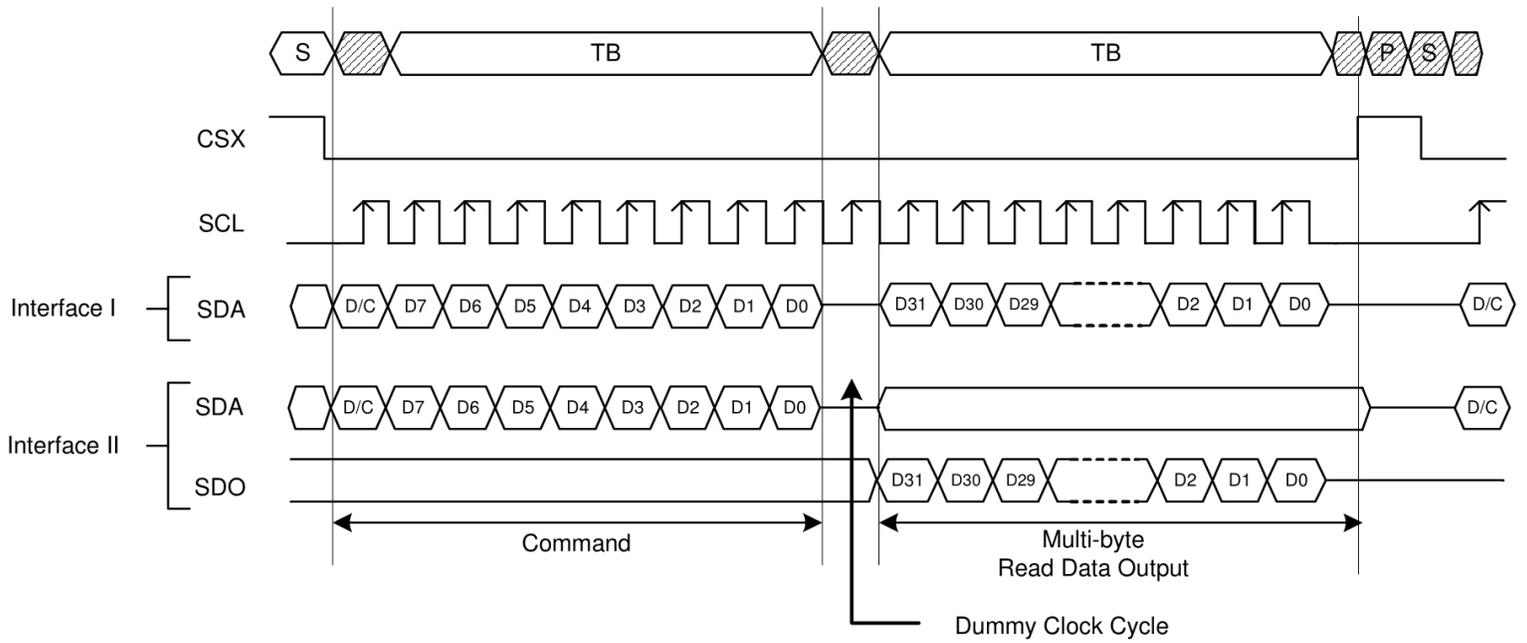
7.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter or display data from ILI9341. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9341 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according to command code.

3-wire Serial Interface Protocol

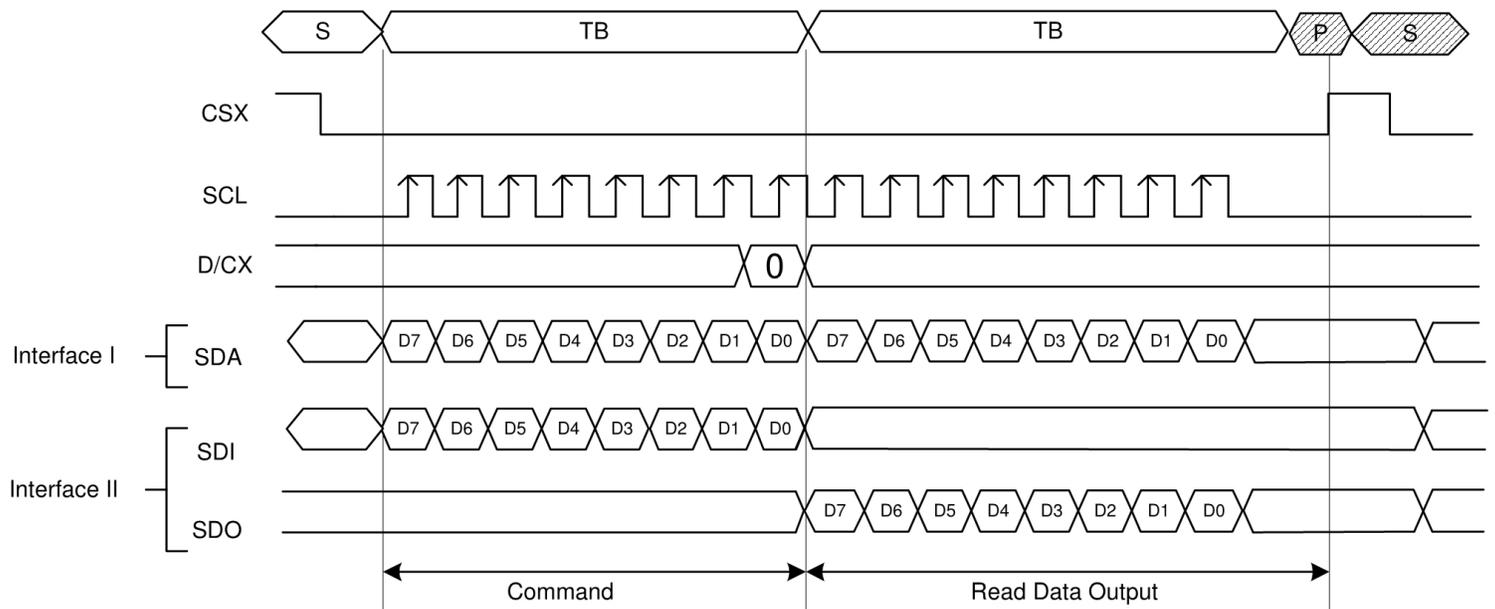


3-wire Serial Protocol (for RDDST command: 32-bit read)

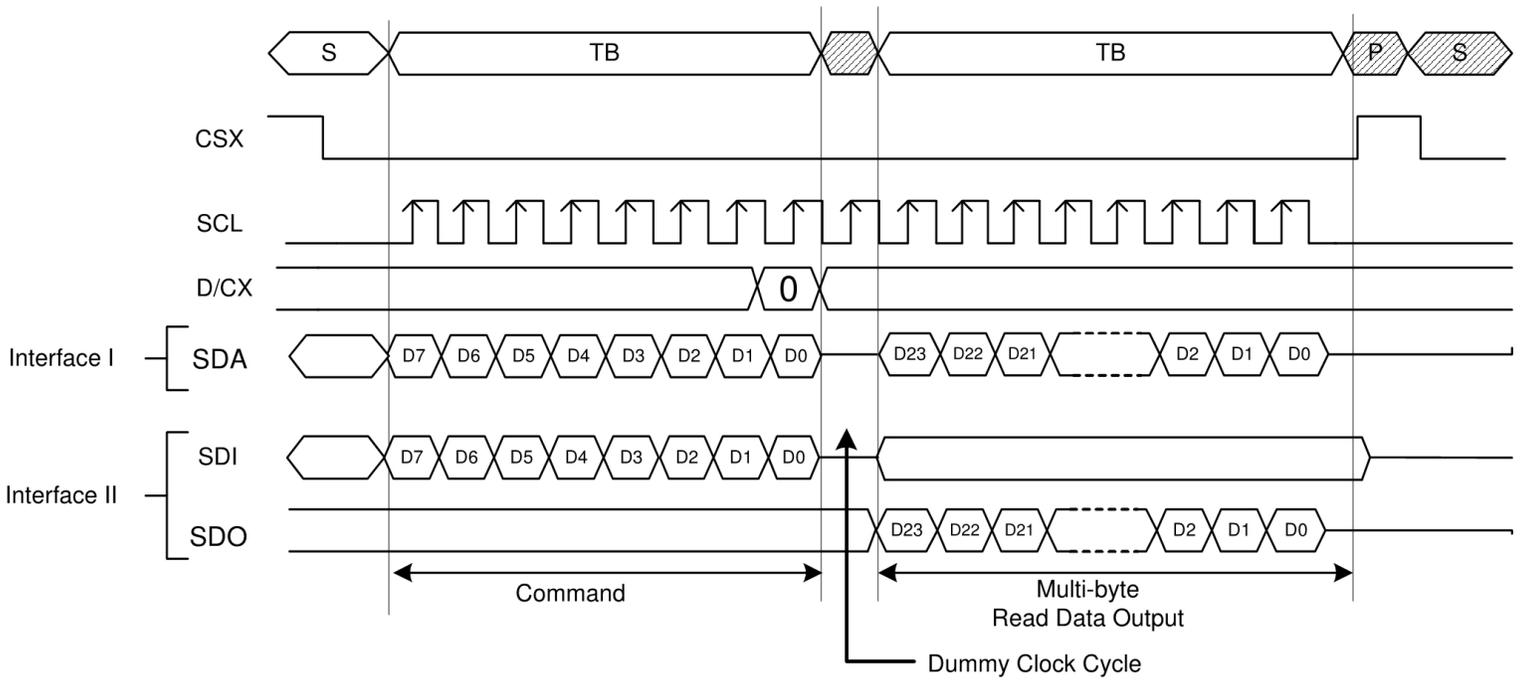


4-wire Serial Interface Protocol

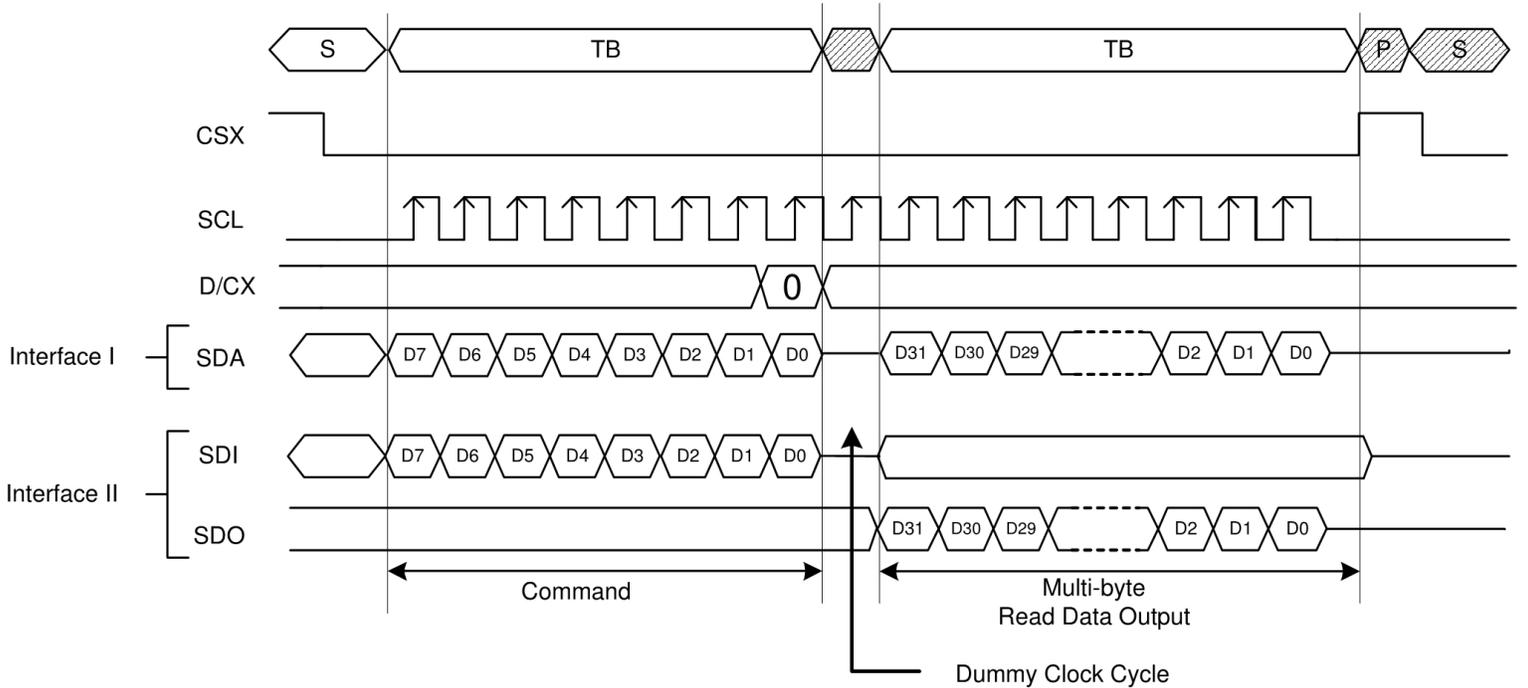
4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-wire Serial Protocol (for RDDID command: 24-bit read)

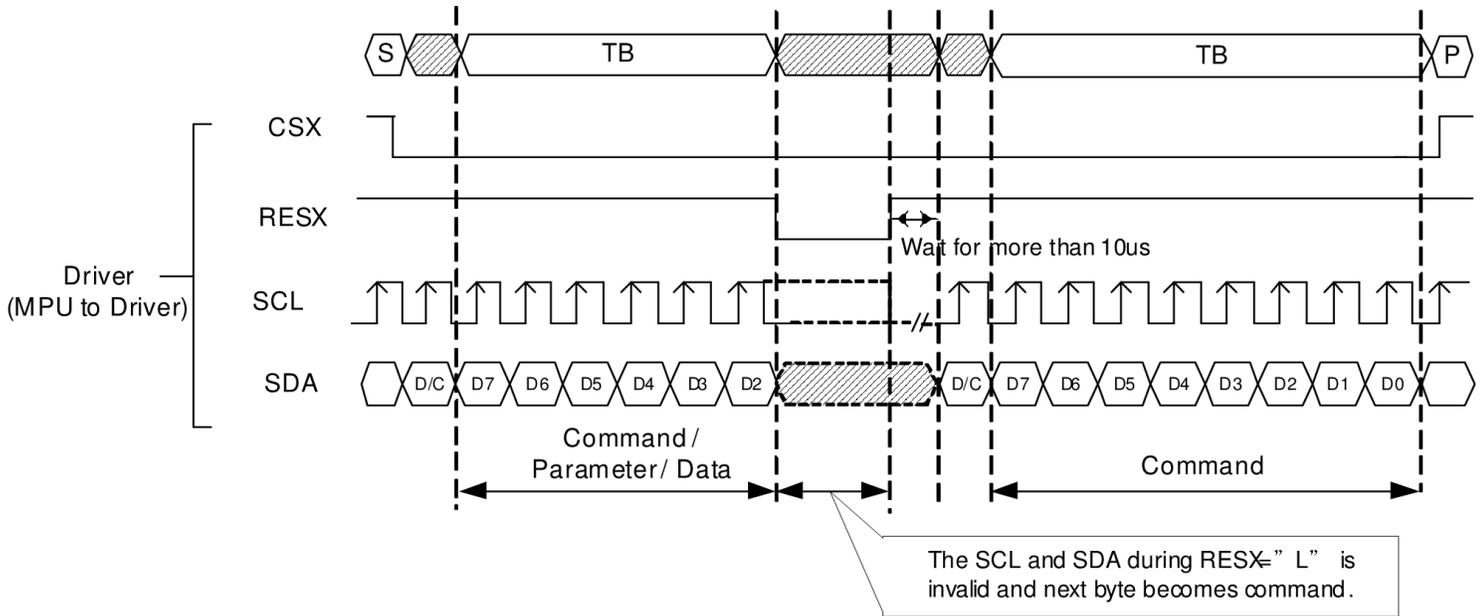


4-wire Serial Protocol (for RDDST command: 32-bit read)

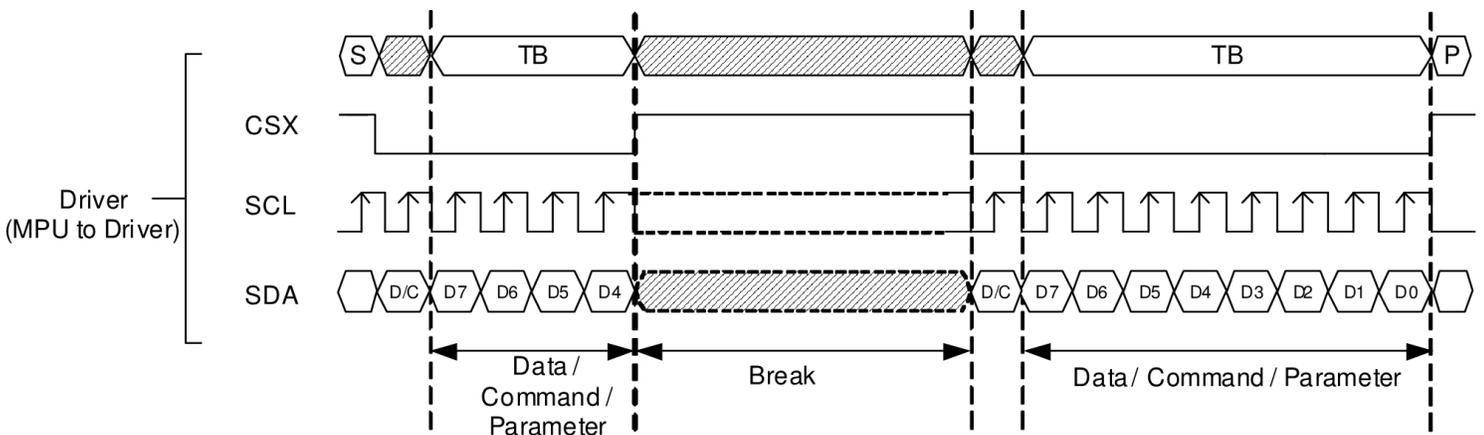


7.1.11. Data Transfer Break and Recovery

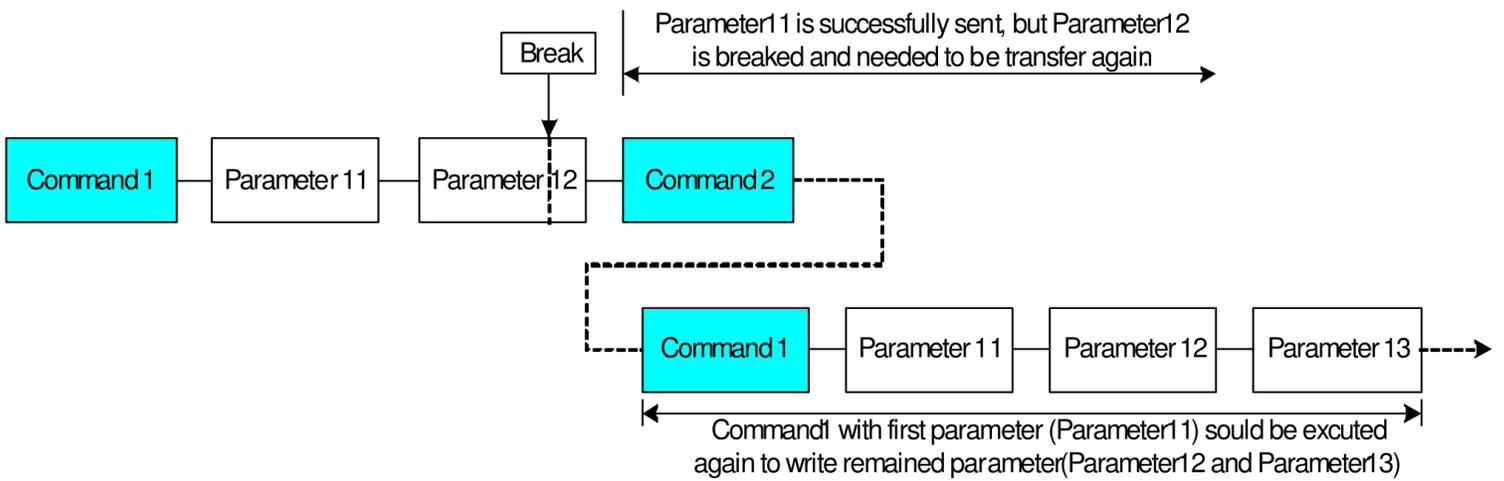
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



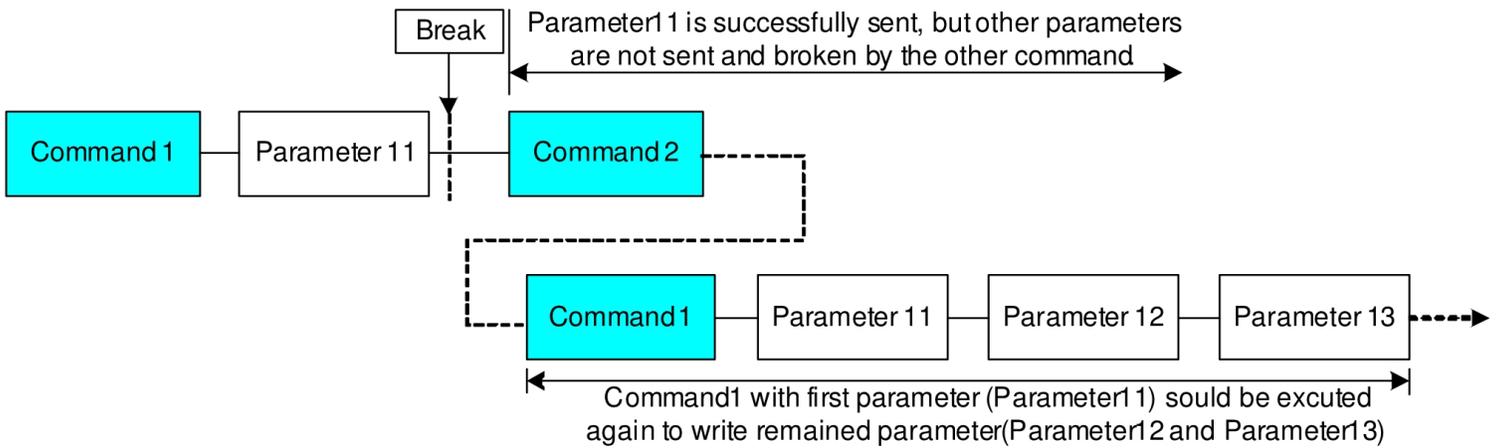
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

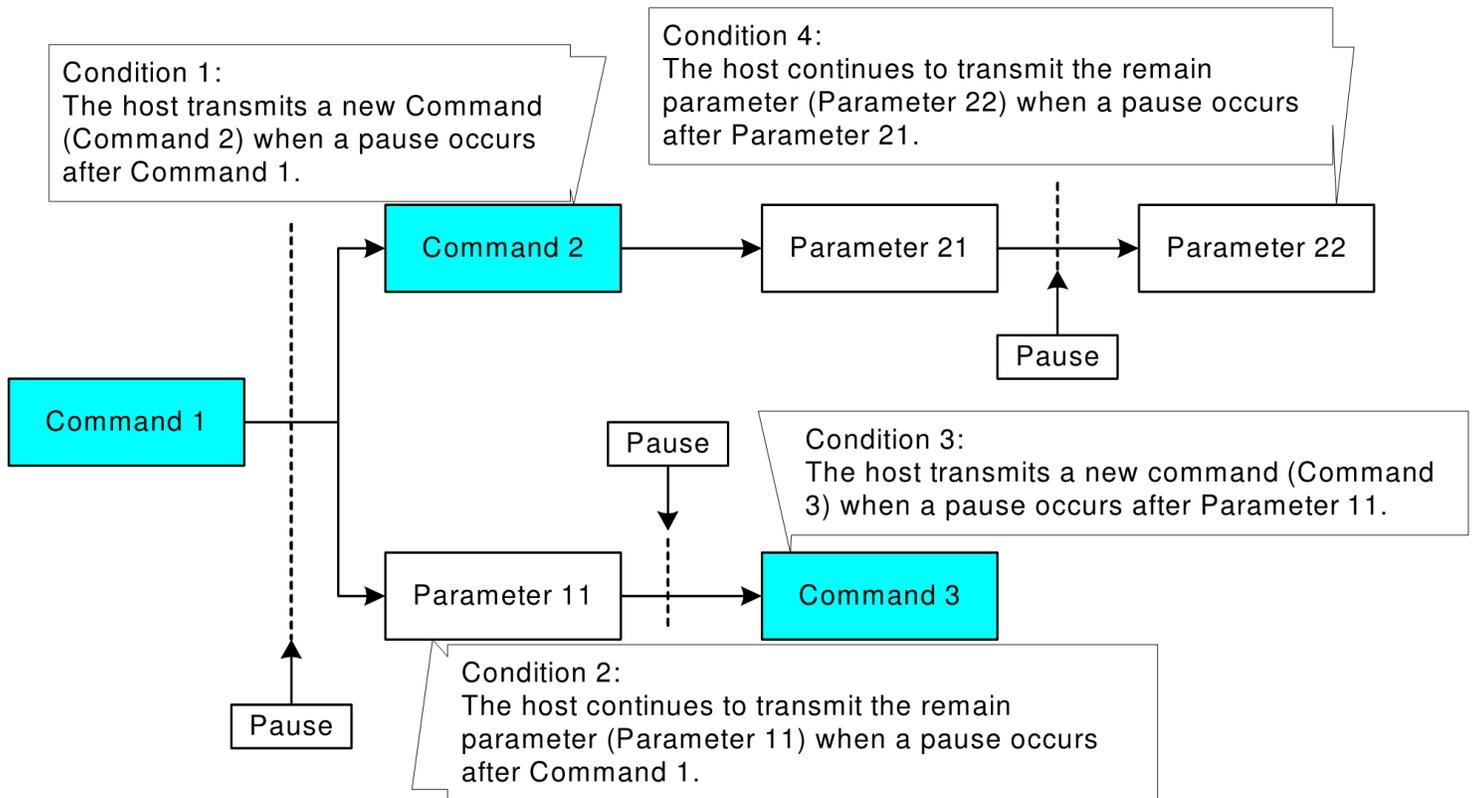


7.1.12. Data Transfer Pause

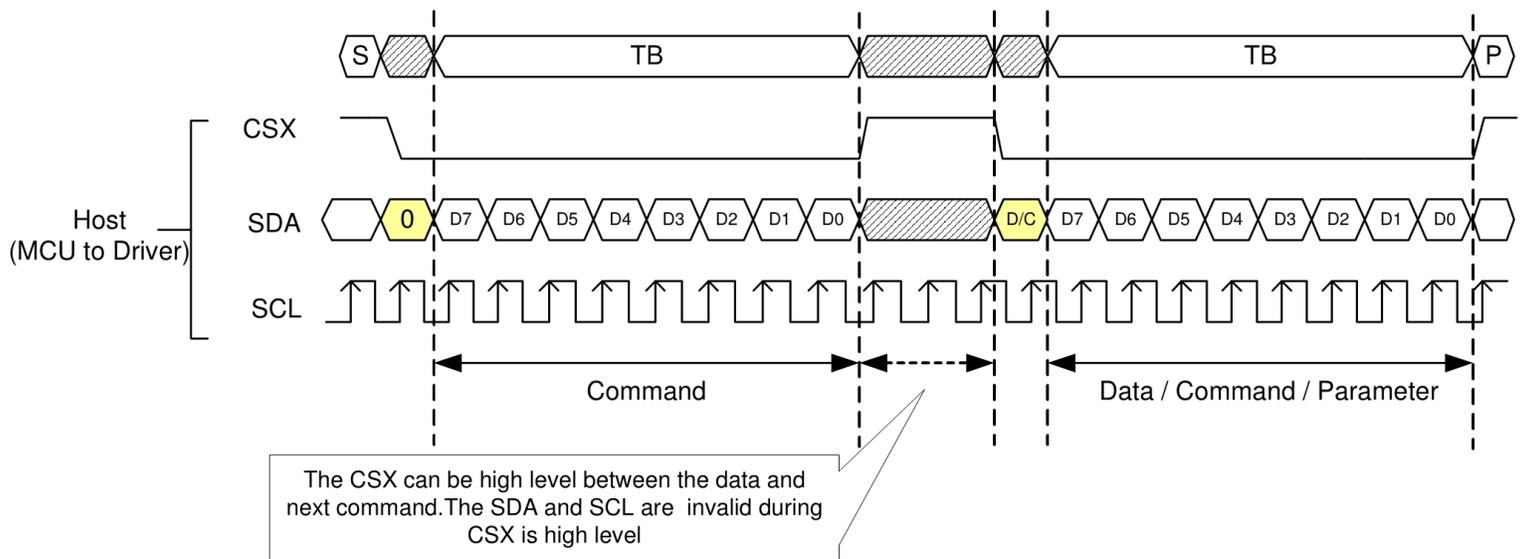
It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9341 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:

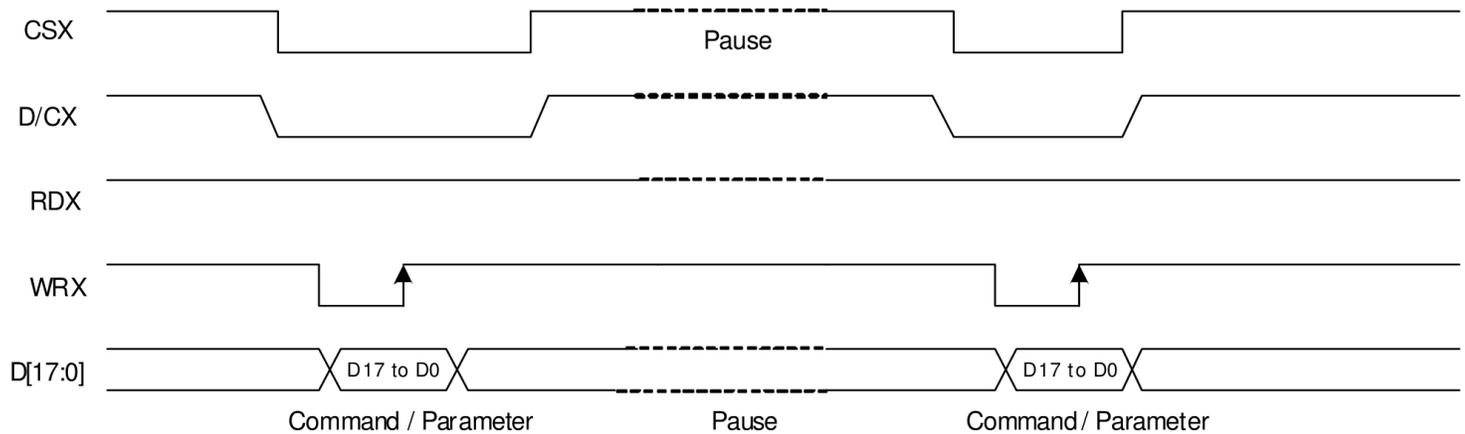
- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter



7.1.13. Serial Interface Pause (3_wire)



7.1.14. Parallel Interface Pause

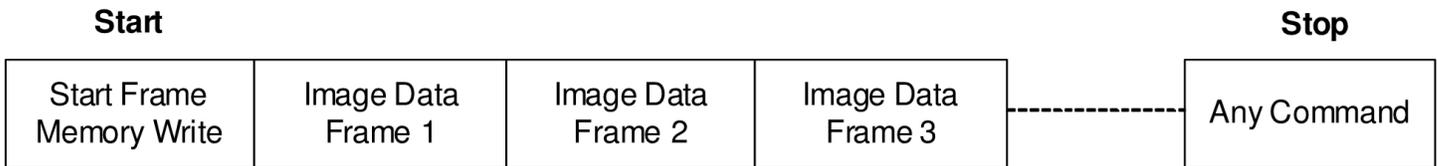


7.1.15. Data Transfer Mode

ILI9341 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

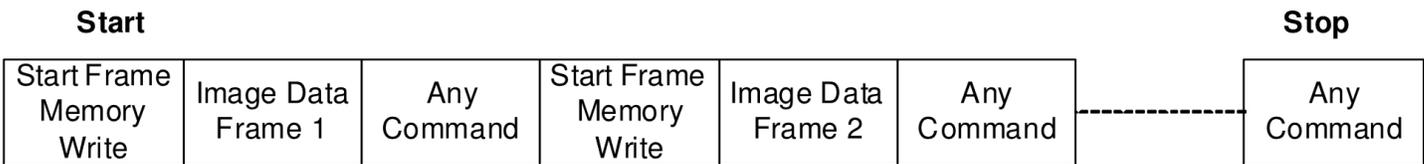
7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9341 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

ILI9341 supports several pixel formats that can be selected by DPI [2:0] bits of “Pixel Format Set (3Ah)” and RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM[1:0]		RIM	DPI[2:0]			RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	DE Mode Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK, D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, D[17:13] & D[11:1]
1	0	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	0	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	SYNC Mode In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, D[17:13] & D[11:1]
1	1	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, D[5:0]
1	1	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, D[5:0]

18-bit data bus interface (D[17:0] is used) , DPI[2:0] = 110, and RIM=0

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

The LSB data of red/blue color depends on the EPF[1:0] setting.

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 110, and RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 101, and RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

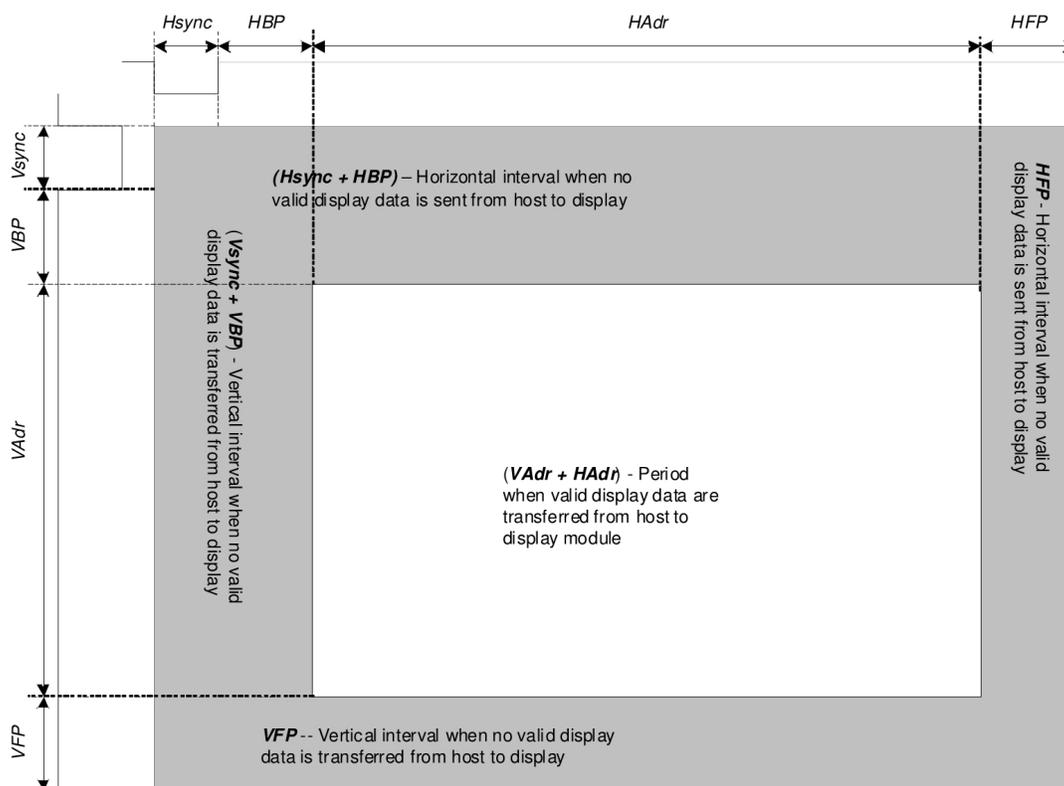
The LSB data of red/blue color depends on the EPF[1:0] setting.

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when

there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data is inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Typical values are setting example when used with panel resolution 240 x 320 (QVGA), clock frequency 6.35MHz and frame

frequency about 70Hz.

Notes:

1. Vertical period (one frame) shall be equal to the sum of $V_{sync} + VBP + VAdr + VFP$.
2. Horizontal period (one line) shall be equal to the sum of $H_{sync} + HBP + HAdr + HFP$.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

$(\text{Number of PCLK per 1 line}) \geq (\text{Number of RTN clock}) \times \text{Division ratio (DIV)} \times \text{PCDIV}$

Setting Example for Display Control Clock in RGB Interface Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

PCDIV [5:0]: Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock.

PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction

$(\text{Number of PCLK in 1H}) \geq (\text{Number of RTN clock}) \times \text{Division ratio (DIV)} \times \text{PCDIV}$.

Setting Example: To set frame frequency to 70Hz:

Internal Clock

Internal Oscillation Clock: 615KHz

$DIV[1:0] = 2'b0$ (x 1/1)

$RTN[4:0] = 5'h1b$ (27 clocks)

$FP = 7'h2$ (2 lines), $BP = 7'h2$ (2 lines), $NL = 6'h27$ (320 lines)

Frame Rate → 70.30Hz

DOTCLK

$HSYNC = 10 \text{ CLK}$

$HBP = 20 \text{ CLK}$

$HFP = 10 \text{ CLK}$

$70\text{Hz} \times (2 + 320 + 2) \text{ lines} \times (10 + 20 + 240 + 10) \text{ clocks} = 6.35\text{MHz}$

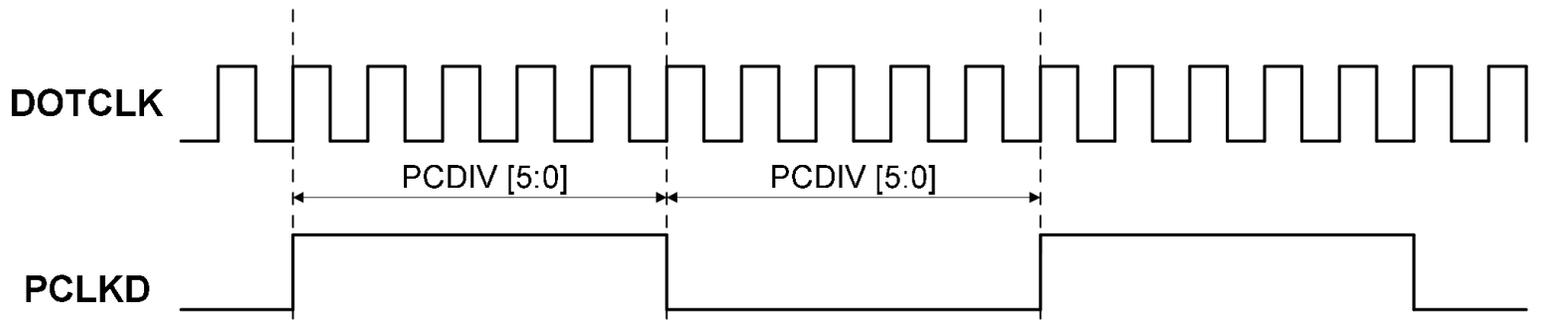
$\text{DOTCLK frequency} = 6.35\text{MHz}$

$6.35 \text{ MHz} / 615\text{KHz} = 10.32$ □ Set PCDIV so that PCLK is divided by 10.

$\text{external fosc} = 6.35 \text{ MHz} / 10 = 635\text{KHz}$

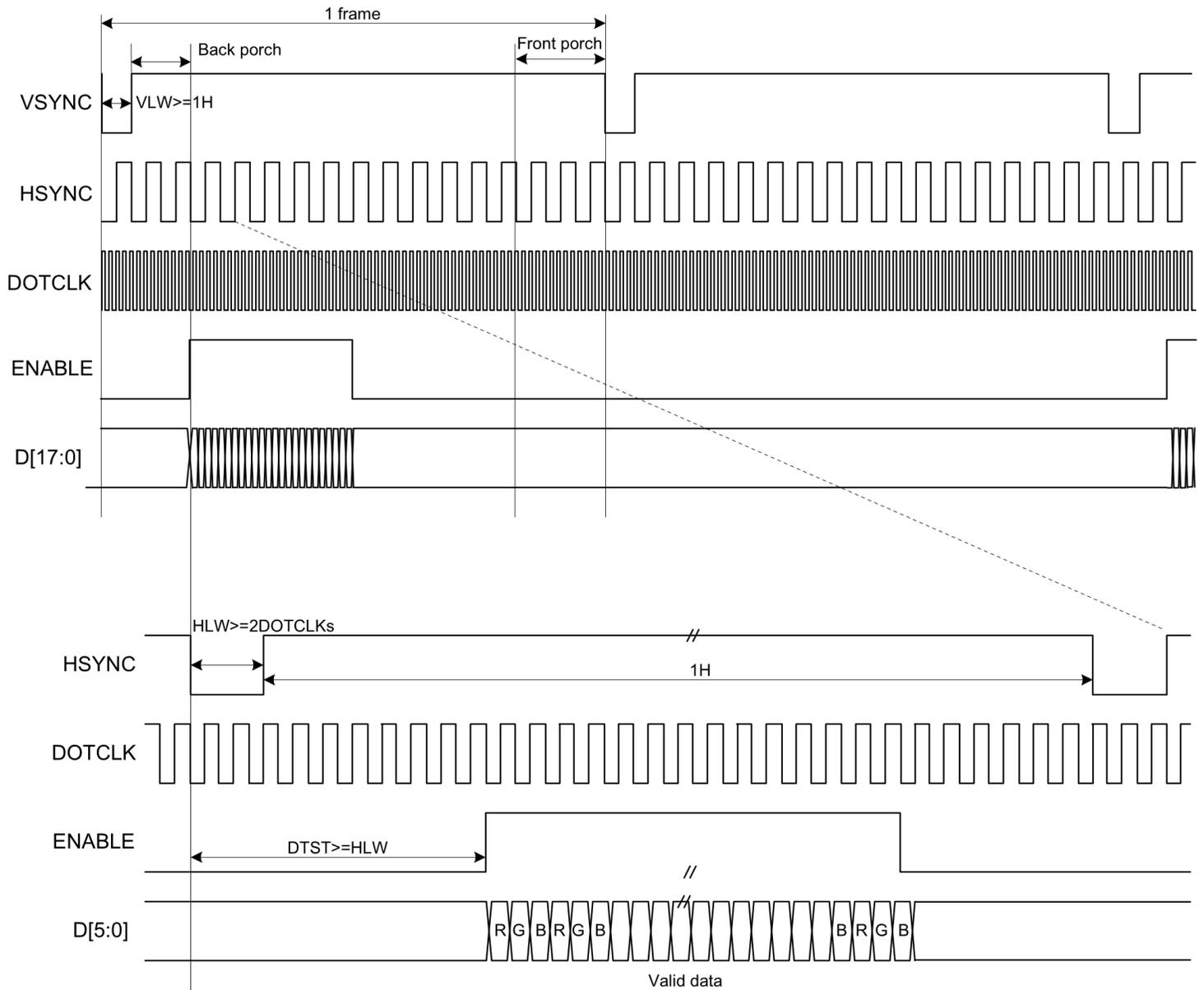
$\text{PCDIV} = [6.35\text{MHz} / 635\text{KHz}] / 2 - 1 = 4$

$\text{PCDIV}[5:0] = 6'h04$ (10 DOTCLK)

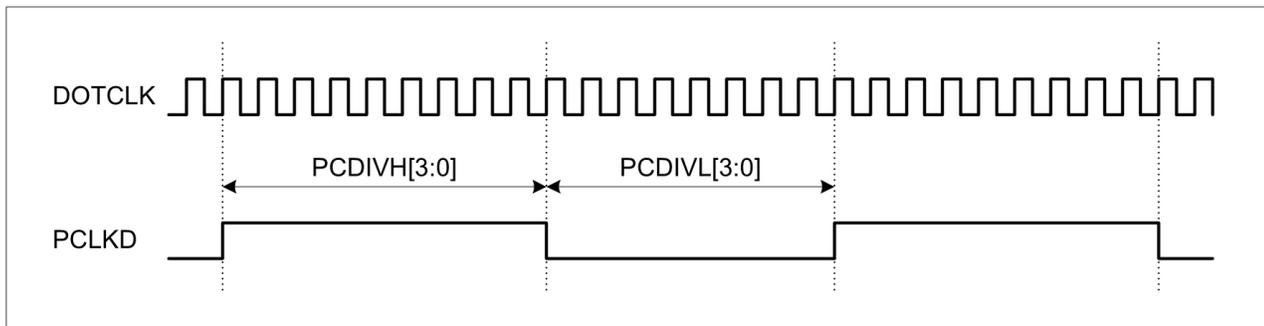


7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.



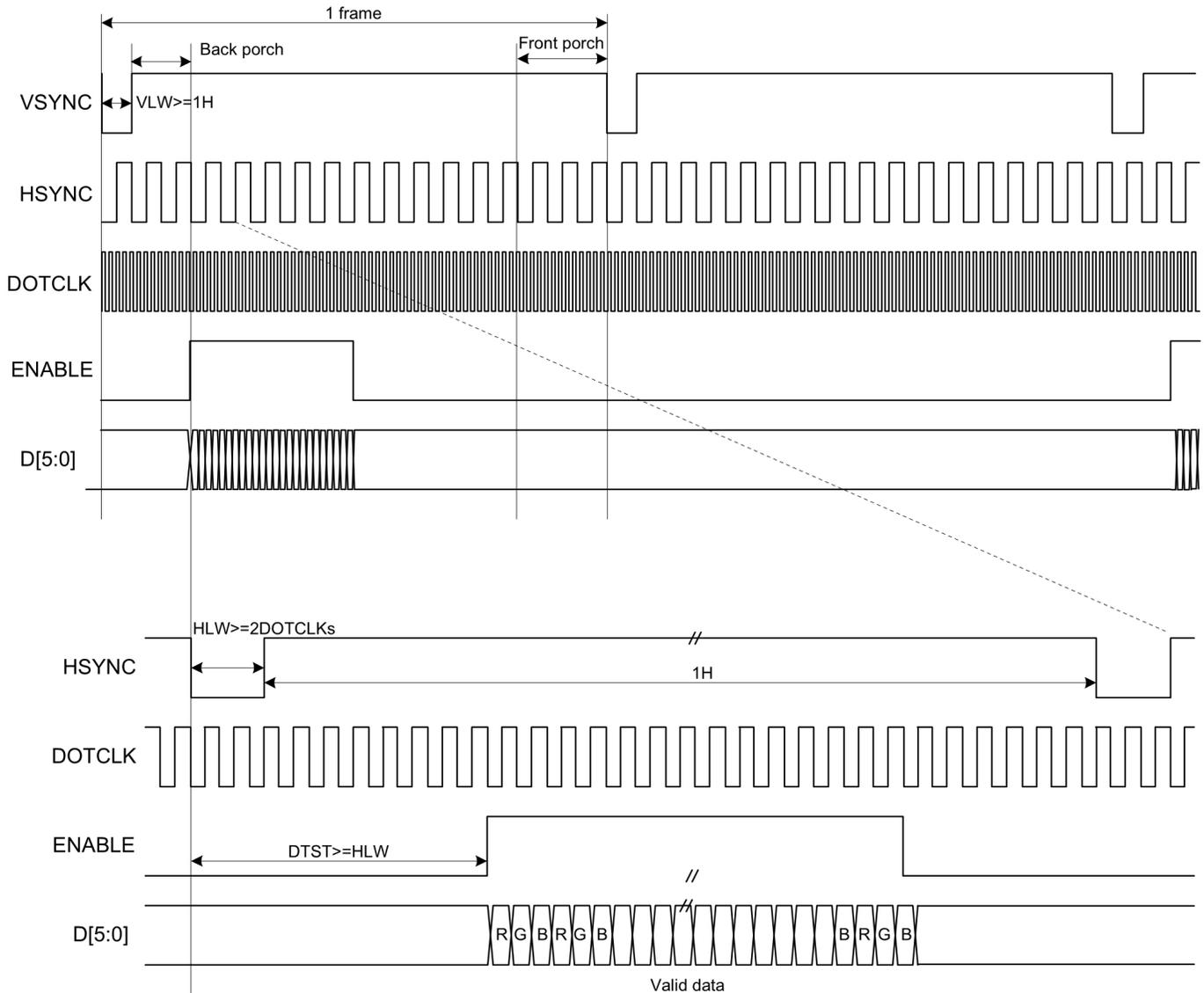
VLW : VSYNC Low Width
 HLW : HSYNC Low Width
 DTST : Data Transfer Startup Time



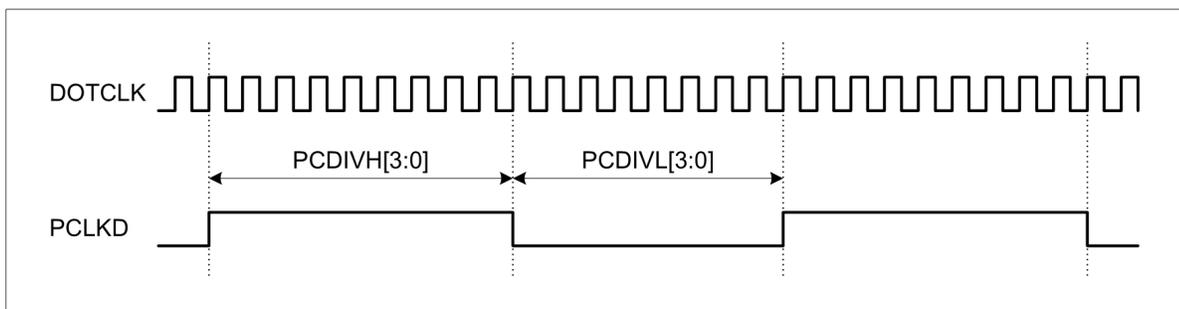
Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:



VLW : VSYNC Low Width
 HLW : HSYNC Low Width
 DTST : Data Transfer Startup Time



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

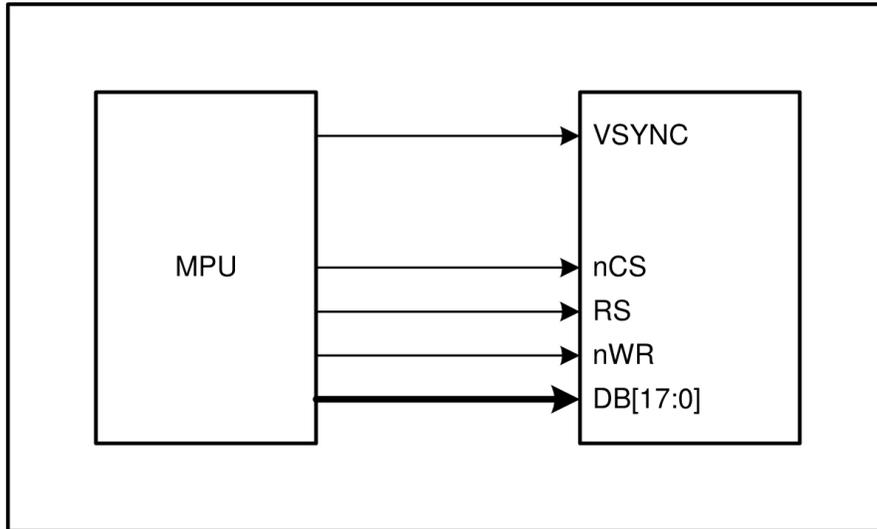
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

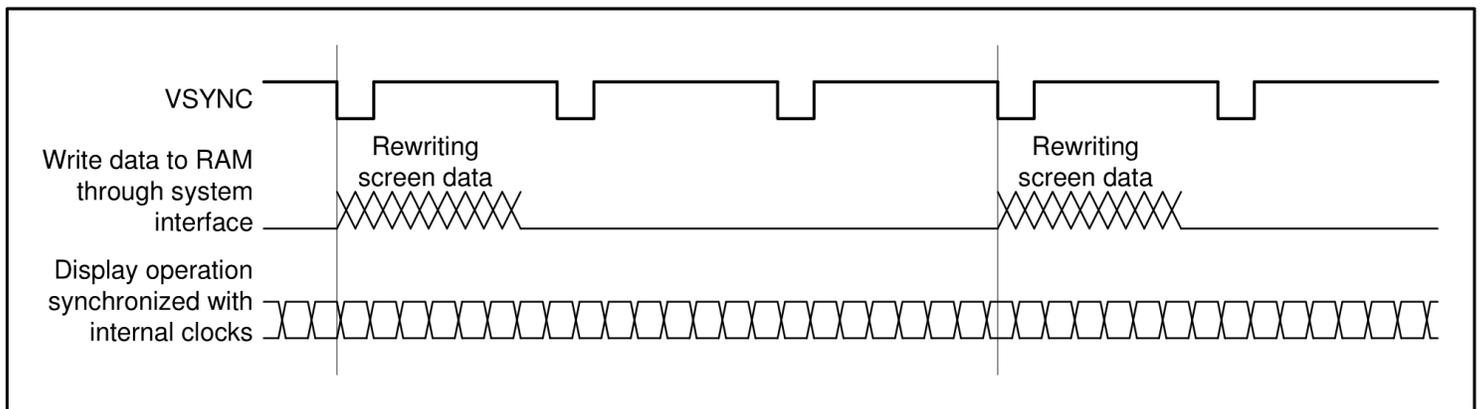
Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

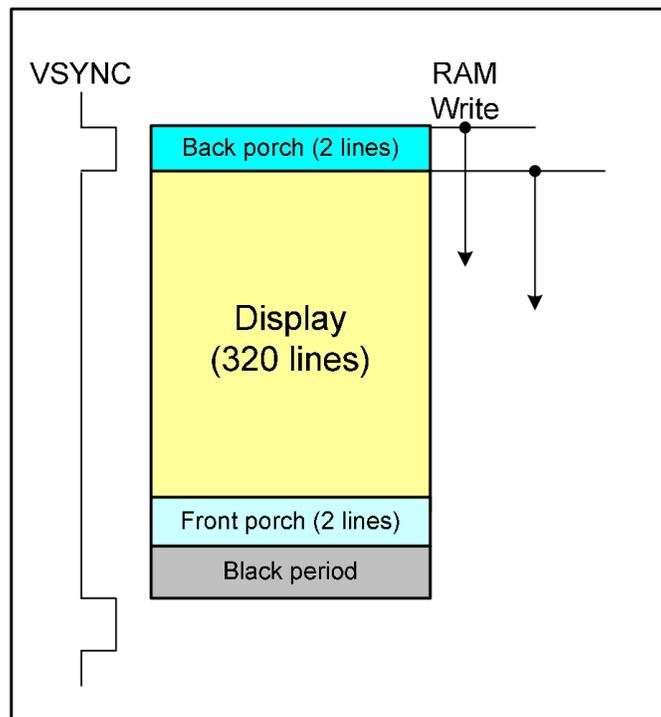
7.3. VSYNC Interface

ILI9341 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080- I /8080- II system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.



In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.





The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\text{Minimum RAM write speed [Hz]} > \frac{240 \times \text{DisplayLines(NL)}}{[\text{BackPorch(VBP)} + \text{DisplayLines(NL)} - \text{margins}] \times \text{Clocks per line} \times (1/\text{fosc})}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB x 320 lines

Lines: 320 lines (NL = 100111)

Back porch: 2 lines (VBP = 0000010)

Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz

Frequency fluctuation: 10%

$$\text{Internal oscillator clock (fosc.) [Hz]} = 70 \times [320 + 2 + 2] \times 27 \text{ clocks} \times (1.1/0.9) \doteq 748\text{KHz}$$

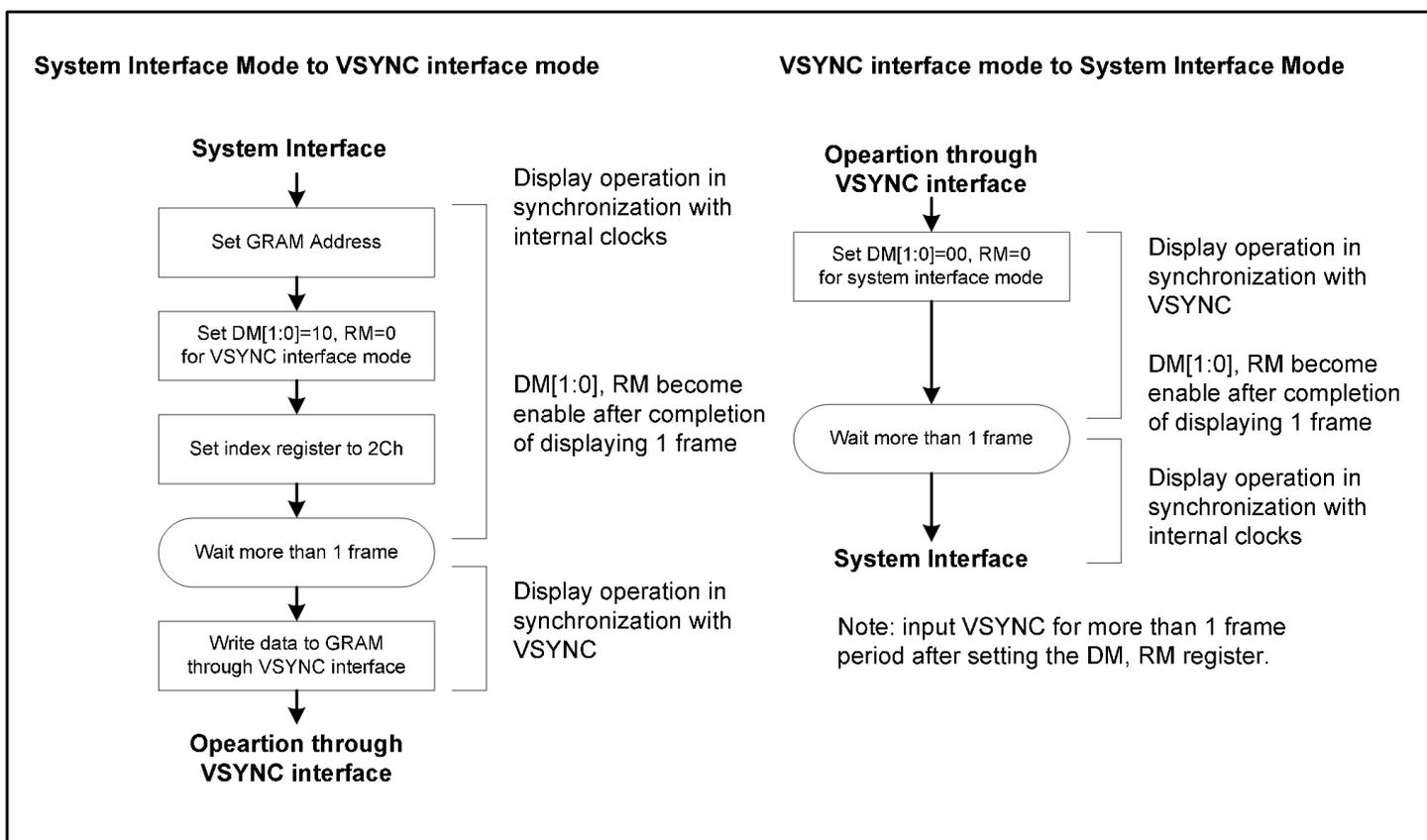
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with $\pm 10\%$ margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

$$\text{Minimum speed for RAM writing [Hz]} > 240 \times 320 \times 748K / [(2 + 320 - 2)\text{lines} \times 27\text{clocks}] \doteq 6.65 \text{ MHz}$$

The above theoretical value is calculated based on the premise that the ILI9341 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9341 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.



7.4. Color Depth Conversion Look Up Table

When ILI9341 operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detailed for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel –mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R ₀₀₅ R ₀₀₄ R ₀₀₃ R ₀₀₂ R ₀₀₁ R ₀₀₀	1
00001	R ₀₁₅ R ₀₁₄ R ₀₁₃ R ₀₁₂ R ₀₁₁ R ₀₁₀	2
00010	R ₀₂₅ R ₀₂₄ R ₀₂₃ R ₀₂₂ R ₀₂₁ R ₀₂₀	3
00011	R ₀₃₅ R ₀₃₄ R ₀₃₃ R ₀₃₂ R ₀₃₁ R ₀₃₀	4
00100	R ₀₄₅ R ₀₄₄ R ₀₄₃ R ₀₄₂ R ₀₄₁ R ₀₄₀	5
00101	R ₀₅₅ R ₀₅₄ R ₀₅₃ R ₀₅₂ R ₀₅₁ R ₀₅₀	6
00110	R ₀₆₅ R ₀₆₄ R ₀₆₃ R ₀₆₂ R ₀₆₁ R ₀₆₀	7
00111	R ₀₇₅ R ₀₇₄ R ₀₇₃ R ₀₇₂ R ₀₇₁ R ₀₇₀	8
01000	R ₀₈₅ R ₀₈₄ R ₀₈₃ R ₀₈₂ R ₀₈₁ R ₀₈₀	9
01001	R ₀₉₅ R ₀₉₄ R ₀₉₃ R ₀₉₂ R ₀₉₁ R ₀₉₀	10
01010	R ₁₀₅ R ₁₀₄ R ₁₀₃ R ₁₀₂ R ₁₀₁ R ₁₀₀	11
01011	R ₁₁₅ R ₁₁₄ R ₁₁₃ R ₁₁₂ R ₁₁₁ R ₁₁₀	12
01100	R ₁₂₅ R ₁₂₄ R ₁₂₃ R ₁₂₂ R ₁₂₁ R ₁₂₀	13
01101	R ₁₃₅ R ₁₃₄ R ₁₃₃ R ₁₃₂ R ₁₃₁ R ₁₃₀	14
01110	R ₁₄₅ R ₁₄₄ R ₁₄₃ R ₁₄₂ R ₁₄₁ R ₁₄₀	15
01111	R ₁₅₅ R ₁₅₄ R ₁₅₃ R ₁₅₂ R ₁₅₁ R ₁₅₀	16
10000	R ₁₆₅ R ₁₆₄ R ₁₆₃ R ₁₆₂ R ₁₆₁ R ₁₆₀	17
10001	R ₁₇₅ R ₁₇₄ R ₁₇₃ R ₁₇₂ R ₁₇₁ R ₁₇₀	18
10010	R ₁₈₅ R ₁₈₄ R ₁₈₃ R ₁₈₂ R ₁₈₁ R ₁₈₀	19
10011	R ₁₉₅ R ₁₉₄ R ₁₉₃ R ₁₉₂ R ₁₉₁ R ₁₉₀	20
10100	R ₂₀₅ R ₂₀₄ R ₂₀₃ R ₂₀₂ R ₂₀₁ R ₂₀₀	21
10101	R ₂₁₅ R ₂₁₄ R ₂₁₃ R ₂₁₂ R ₂₁₁ R ₂₁₀	22
10110	R ₂₂₅ R ₂₂₄ R ₂₂₃ R ₂₂₂ R ₂₂₁ R ₂₂₀	23
10111	R ₂₃₅ R ₂₃₄ R ₂₃₃ R ₂₃₂ R ₂₃₁ R ₂₃₀	24
11000	R ₂₄₅ R ₂₄₄ R ₂₄₃ R ₂₄₂ R ₂₄₁ R ₂₄₀	25
11001	R ₂₅₅ R ₂₅₄ R ₂₅₃ R ₂₅₂ R ₂₅₁ R ₂₅₀	26
11010	R ₂₆₅ R ₂₆₄ R ₂₆₃ R ₂₆₂ R ₂₆₁ R ₂₆₀	27
11011	R ₂₇₅ R ₂₇₄ R ₂₇₃ R ₂₇₂ R ₂₇₁ R ₂₇₀	28
11100	R ₂₈₅ R ₂₈₄ R ₂₈₃ R ₂₈₂ R ₂₈₁ R ₂₈₀	29
11101	R ₂₉₅ R ₂₉₄ R ₂₉₃ R ₂₉₂ R ₂₉₁ R ₂₉₀	30
11110	R ₃₀₅ R ₃₀₄ R ₃₀₃ R ₃₀₂ R ₃₀₁ R ₃₀₀	31
11111	R ₃₁₅ R ₃₁₄ R ₃₁₃ R ₃₁₂ R ₃₁₁ R ₃₁₀	32

G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
000000	G ₀₀₅ G ₀₀₄ G ₀₀₃ G ₀₀₂ G ₀₀₁ G ₀₀₀	33
000001	G ₀₁₅ G ₀₁₄ G ₀₁₃ G ₀₁₂ G ₀₁₁ G ₀₁₀	34
000010	G ₀₂₅ G ₀₂₄ G ₀₂₃ G ₀₂₂ G ₀₂₁ G ₀₂₀	35
000011	G ₀₃₅ G ₀₃₄ G ₀₃₃ G ₀₃₂ G ₀₃₁ G ₀₃₀	36
000100	G ₀₄₅ G ₀₄₄ G ₀₄₃ G ₀₄₂ G ₀₄₁ G ₀₄₀	37
000101	G ₀₅₅ G ₀₅₄ G ₀₅₃ G ₀₅₂ G ₀₅₁ G ₀₅₀	38
000110	G ₀₆₅ G ₀₆₄ G ₀₆₃ G ₀₆₂ G ₀₆₁ G ₀₆₀	39
000111	G ₀₇₅ G ₀₇₄ G ₀₇₃ G ₀₇₂ G ₀₇₁ G ₀₇₀	40
001000	G ₀₈₅ G ₀₈₄ G ₀₈₃ G ₀₈₂ G ₀₈₁ G ₀₈₀	41
001001	G ₀₉₅ G ₀₉₄ G ₀₉₃ G ₀₉₂ G ₀₉₁ G ₀₉₀	42
001010	G ₁₀₅ G ₁₀₄ G ₁₀₃ G ₁₀₂ G ₁₀₁ G ₁₀₀	43
001011	G ₁₁₅ G ₁₁₄ G ₁₁₃ G ₁₁₂ G ₁₁₁ G ₁₁₀	44
001100	G ₁₂₅ G ₁₂₄ G ₁₂₃ G ₁₂₂ G ₁₂₁ G ₁₂₀	45
001101	G ₁₃₅ G ₁₃₄ G ₁₃₃ G ₁₃₂ G ₁₃₁ G ₁₃₀	46
001110	G ₁₄₅ G ₁₄₄ G ₁₄₃ G ₁₄₂ G ₁₄₁ G ₁₄₀	47
001111	G ₁₅₅ G ₁₅₄ G ₁₅₃ G ₁₅₂ G ₁₅₁ G ₁₅₀	48
010000	G ₁₆₅ G ₁₆₄ G ₁₆₃ G ₁₆₂ G ₁₆₁ G ₁₆₀	49
010001	G ₁₇₅ G ₁₇₄ G ₁₇₃ G ₁₇₂ G ₁₇₁ G ₁₇₀	50
010010	G ₁₈₅ G ₁₈₄ G ₁₈₃ G ₁₈₂ G ₁₈₁ G ₁₈₀	51
010011	G ₁₉₅ G ₁₉₄ G ₁₉₃ G ₁₉₂ G ₁₉₁ G ₁₉₀	52
010100	G ₂₀₅ G ₂₀₄ G ₂₀₃ G ₂₀₂ G ₂₀₁ G ₂₀₀	53
010101	G ₂₁₅ G ₂₁₄ G ₂₁₃ G ₂₁₂ G ₂₁₁ G ₂₁₀	54
010110	G ₂₂₅ G ₂₂₄ G ₂₂₃ G ₂₂₂ G ₂₂₁ G ₂₂₀	55
010111	G ₂₃₅ G ₂₃₄ G ₂₃₃ G ₂₃₂ G ₂₃₁ G ₂₃₀	56
011000	G ₂₄₅ G ₂₄₄ G ₂₄₃ G ₂₄₂ G ₂₄₁ G ₂₄₀	57
011001	G ₂₅₅ G ₂₅₄ G ₂₅₃ G ₂₅₂ G ₂₅₁ G ₂₅₀	58
011010	G ₂₆₅ G ₂₆₄ G ₂₆₃ G ₂₆₂ G ₂₆₁ G ₂₆₀	59
011011	G ₂₇₅ G ₂₇₄ G ₂₇₃ G ₂₇₂ G ₂₇₁ G ₂₇₀	60
011100	G ₂₈₅ G ₂₈₄ G ₂₈₃ G ₂₈₂ G ₂₈₁ G ₂₈₀	61
011101	G ₂₉₅ G ₂₉₄ G ₂₉₃ G ₂₉₂ G ₂₉₁ G ₂₉₀	62
011110	G ₃₀₅ G ₃₀₄ G ₃₀₃ G ₃₀₂ G ₃₀₁ G ₃₀₀	63
011111	G ₃₁₅ G ₃₁₄ G ₃₁₃ G ₃₁₂ G ₃₁₁ G ₃₁₀	64
100000	G ₃₂₅ G ₃₂₄ G ₃₂₃ G ₃₂₂ G ₃₂₁ G ₃₂₀	65
100001	G ₃₃₅ G ₃₃₄ G ₃₃₃ G ₃₃₂ G ₃₃₁ G ₃₃₀	66

G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G ₃₄₅ G ₃₄₄ G ₃₄₃ G ₃₄₂ G ₃₄₁ G ₃₄₀	67
100011	G ₃₅₅ G ₃₅₄ G ₃₅₃ G ₃₅₂ G ₃₅₁ G ₃₅₀	68
100100	G ₃₆₅ G ₃₆₄ G ₃₆₃ G ₃₆₂ G ₃₆₁ G ₃₆₀	69
100101	G ₃₇₅ G ₃₇₄ G ₃₇₃ G ₃₇₂ G ₃₇₁ G ₃₇₀	70
100110	G ₃₈₅ G ₃₈₄ G ₃₈₃ G ₃₈₂ G ₃₈₁ G ₃₈₀	71
100111	G ₃₉₅ G ₃₉₄ G ₃₉₃ G ₃₉₂ G ₃₉₁ G ₃₉₀	72
101000	G ₄₀₅ G ₄₀₄ G ₄₀₃ G ₄₀₂ G ₄₀₁ G ₄₀₀	73
101001	G ₄₁₅ G ₄₁₄ G ₄₁₃ G ₄₁₂ G ₄₁₁ G ₄₁₀	74
101010	G ₄₂₅ G ₄₂₄ G ₄₂₃ G ₄₂₂ G ₄₂₁ G ₄₂₀	75
101011	G ₄₃₅ G ₄₃₄ G ₄₃₃ G ₄₃₂ G ₄₃₁ G ₄₃₀	76
101100	G ₄₄₅ G ₄₄₄ G ₄₄₃ G ₄₄₂ G ₄₄₁ G ₄₄₀	77
101101	G ₄₅₅ G ₄₅₄ G ₄₅₃ G ₄₅₂ G ₄₅₁ G ₄₅₀	78
101110	G ₄₆₅ G ₄₆₄ G ₄₆₃ G ₄₆₂ G ₄₆₁ G ₄₆₀	79
101111	G ₄₇₅ G ₄₇₄ G ₄₇₃ G ₄₇₂ G ₄₇₁ G ₄₇₀	80
110000	G ₄₈₅ G ₄₈₄ G ₄₈₃ G ₄₈₂ G ₄₈₁ G ₄₈₀	81
110001	G ₄₉₅ G ₄₉₄ G ₄₉₃ G ₄₉₂ G ₄₉₁ G ₄₉₀	82
110010	G ₅₀₅ G ₅₀₄ G ₅₀₃ G ₅₀₂ G ₅₀₁ G ₅₀₀	83
110011	G ₅₁₅ G ₅₁₄ G ₅₁₃ G ₅₁₂ G ₅₁₁ G ₅₁₀	84
110100	G ₅₂₅ G ₅₂₄ G ₅₂₃ G ₅₂₂ G ₅₂₁ G ₅₂₀	85
110101	G ₅₃₅ G ₅₃₄ G ₅₃₃ G ₅₃₂ G ₅₃₁ G ₅₃₀	86
110110	G ₅₄₅ G ₅₄₄ G ₅₄₃ G ₅₄₂ G ₅₄₁ G ₅₄₀	87
110111	G ₅₅₅ G ₅₅₄ G ₅₅₃ G ₅₅₂ G ₅₅₁ G ₅₅₀	88
111000	G ₅₆₅ G ₅₆₄ G ₅₆₃ G ₅₆₂ G ₅₆₁ G ₅₆₀	89
111001	G ₅₇₅ G ₅₇₄ G ₅₇₃ G ₅₇₂ G ₅₇₁ G ₅₇₀	90
111010	G ₅₈₅ G ₅₈₄ G ₅₈₃ G ₅₈₂ G ₅₈₁ G ₅₈₀	91
111011	G ₅₉₅ G ₅₉₄ G ₅₉₃ G ₅₉₂ G ₅₉₁ G ₅₉₀	92
111100	G ₆₀₅ G ₆₀₄ G ₆₀₃ G ₆₀₂ G ₆₀₁ G ₆₀₀	93
111101	G ₆₁₅ G ₆₁₄ G ₆₁₃ G ₆₁₂ G ₆₁₁ G ₆₁₀	94
111110	G ₆₂₅ G ₆₂₄ G ₆₂₃ G ₆₂₂ G ₆₂₁ G ₆₂₀	95
111111	G ₆₃₅ G ₆₃₄ G ₆₃₃ G ₆₃₂ G ₆₃₁ G ₆₃₀	96

B input (5-bit) 16-bit/pixel –mode 65,536 colors	B output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	B ₀₀₅ B ₀₀₄ B ₀₀₃ B ₀₀₂ B ₀₀₁ B ₀₀₀	97
00001	B ₀₁₅ B ₀₁₄ B ₀₁₃ B ₀₁₂ B ₀₁₁ B ₀₁₀	98
00010	B ₀₂₅ B ₀₂₄ B ₀₂₃ B ₀₂₂ B ₀₂₁ B ₀₂₀	99
00011	B ₀₃₅ B ₀₃₄ B ₀₃₃ B ₀₃₂ B ₀₃₁ B ₀₃₀	100
00100	B ₀₄₅ B ₀₄₄ B ₀₄₃ B ₀₄₂ B ₀₄₁ B ₀₄₀	101
00101	B ₀₅₅ B ₀₅₄ B ₀₅₃ B ₀₅₂ B ₀₅₁ B ₀₅₀	102
00110	B ₀₆₅ B ₀₆₄ B ₀₆₃ B ₀₆₂ B ₀₆₁ B ₀₆₀	103
00111	B ₀₇₅ B ₀₇₄ B ₀₇₃ B ₀₇₂ B ₀₇₁ B ₀₇₀	104
01000	B ₀₈₅ B ₀₈₄ B ₀₈₃ B ₀₈₂ B ₀₈₁ B ₀₈₀	105
01001	B ₀₉₅ B ₀₉₄ B ₀₉₃ B ₀₉₂ B ₀₉₁ B ₀₉₀	106
01010	B ₁₀₅ B ₁₀₄ B ₁₀₃ B ₁₀₂ B ₁₀₁ B ₁₀₀	107
01011	B ₁₁₅ B ₁₁₄ B ₁₁₃ B ₁₁₂ B ₁₁₁ B ₁₁₀	108
01100	B ₁₂₅ B ₁₂₄ B ₁₂₃ B ₁₂₂ B ₁₂₁ B ₁₂₀	109
01101	B ₁₃₅ B ₁₃₄ B ₁₃₃ B ₁₃₂ B ₁₃₁ B ₁₃₀	110
01110	B ₁₄₅ B ₁₄₄ B ₁₄₃ B ₁₄₂ B ₁₄₁ B ₁₄₀	111
01111	B ₁₅₅ B ₁₅₄ B ₁₅₃ B ₁₅₂ B ₁₅₁ B ₁₅₀	112
10000	B ₁₆₅ B ₁₆₄ B ₁₆₃ B ₁₆₂ B ₁₆₁ B ₁₆₀	113
10001	B ₁₇₅ B ₁₇₄ B ₁₇₃ B ₁₇₂ B ₁₇₁ B ₁₇₀	114
10010	B ₁₈₅ B ₁₈₄ B ₁₈₃ B ₁₈₂ B ₁₈₁ B ₁₈₀	115
10011	B ₁₉₅ B ₁₉₄ B ₁₉₃ B ₁₉₂ B ₁₉₁ B ₁₉₀	116
10100	B ₂₀₅ B ₂₀₄ B ₂₀₃ B ₂₀₂ B ₂₀₁ B ₂₀₀	117
10101	B ₂₁₅ B ₂₁₄ B ₂₁₃ B ₂₁₂ B ₂₁₁ B ₂₁₀	118
10110	B ₂₂₅ B ₂₂₄ B ₂₂₃ B ₂₂₂ B ₂₂₁ B ₂₂₀	119
10111	B ₂₃₅ B ₂₃₄ B ₂₃₃ B ₂₃₂ B ₂₃₁ B ₂₃₀	120
11000	B ₂₄₅ B ₂₄₄ B ₂₄₃ B ₂₄₂ B ₂₄₁ B ₂₄₀	121
11001	B ₂₅₅ B ₂₅₄ B ₂₅₃ B ₂₅₂ B ₂₅₁ B ₂₅₀	122
11010	B ₂₆₅ B ₂₆₄ B ₂₆₃ B ₂₆₂ B ₂₆₁ B ₂₆₀	123
11011	B ₂₇₅ B ₂₇₄ B ₂₇₃ B ₂₇₂ B ₂₇₁ B ₂₇₀	124
11100	B ₂₈₅ B ₂₈₄ B ₂₈₃ B ₂₈₂ B ₂₈₁ B ₂₈₀	125
11101	B ₂₉₅ B ₂₉₄ B ₂₉₃ B ₂₉₂ B ₂₉₁ B ₂₉₀	126
11110	B ₃₀₅ B ₃₀₄ B ₃₀₃ B ₃₀₂ B ₃₀₁ B ₃₀₀	127
11111	B ₃₁₅ B ₃₁₄ B ₃₁₃ B ₃₁₂ B ₃₁₁ B ₃₁₀	128

7.5. Display Data RAM (DDRAM)

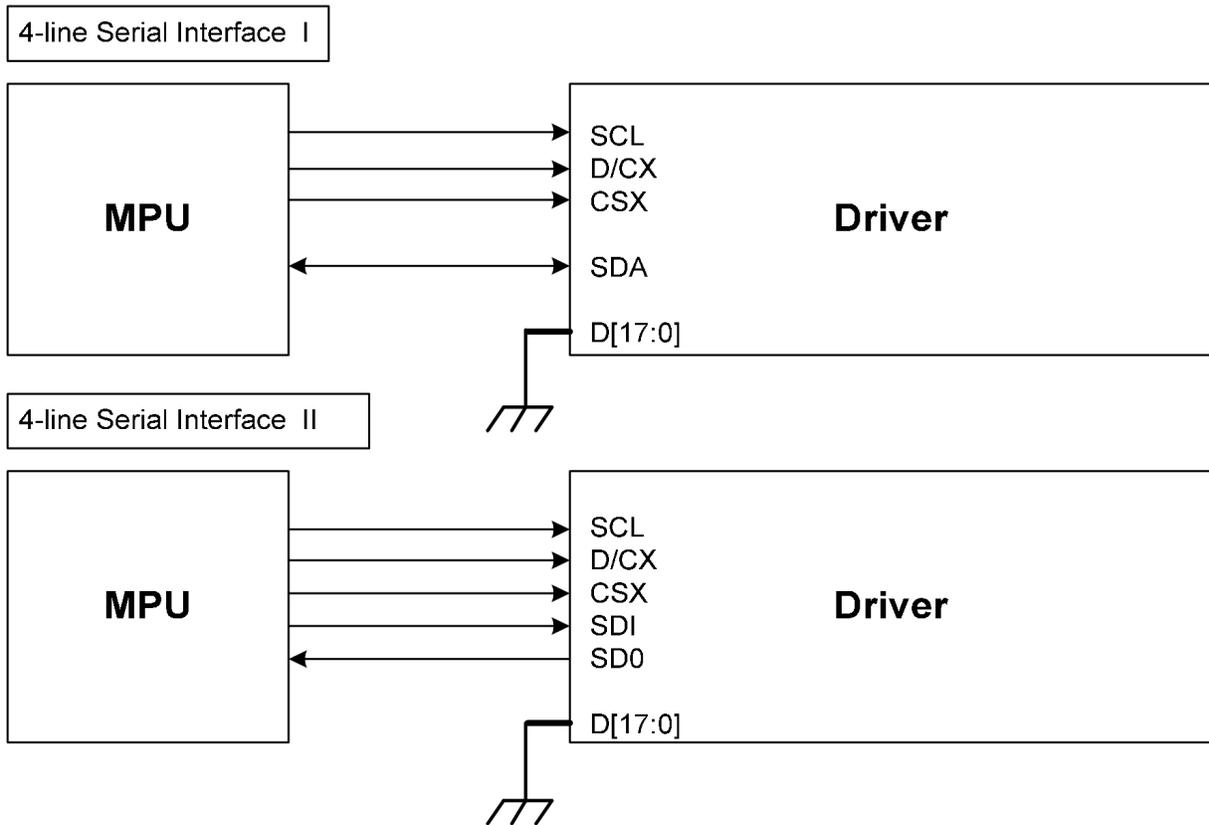
ILI9341 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

7.6. Display Data Format

ILI9341 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080- I /8080- II series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.6.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0110" for serial interface I or IM [3:0] to "1110" for serial interface II. The shown figure is the example of 4-line SPI interface.

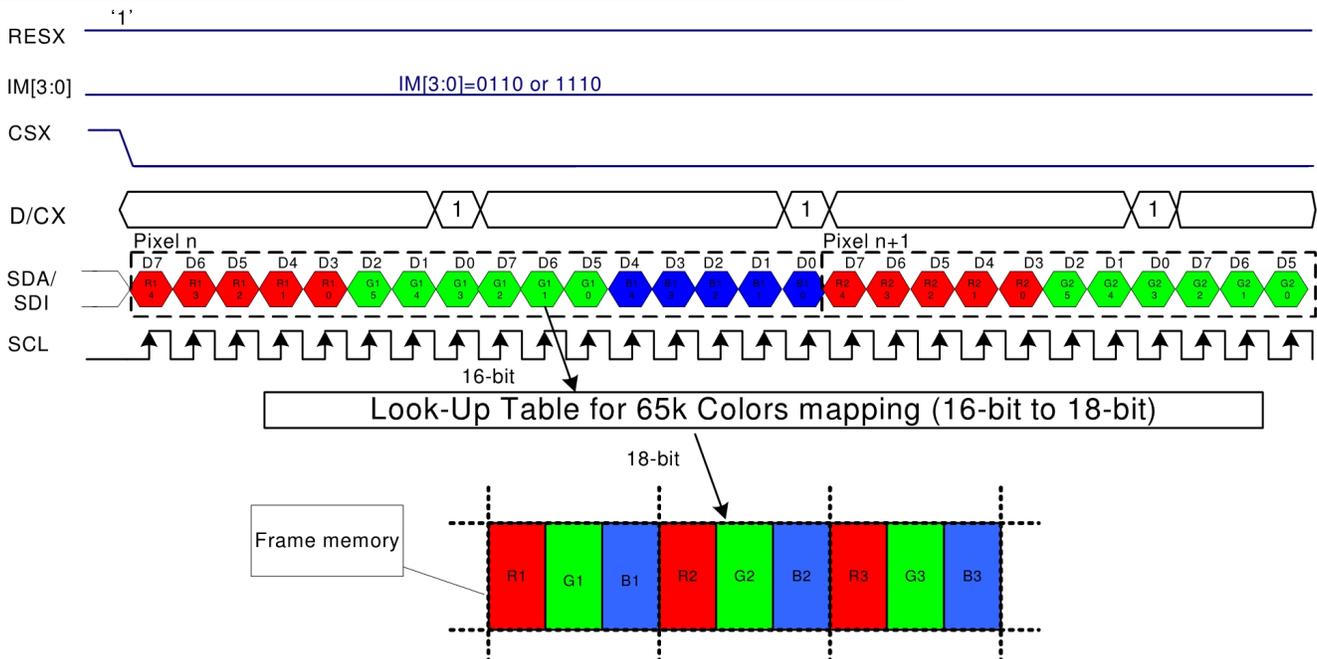


In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors



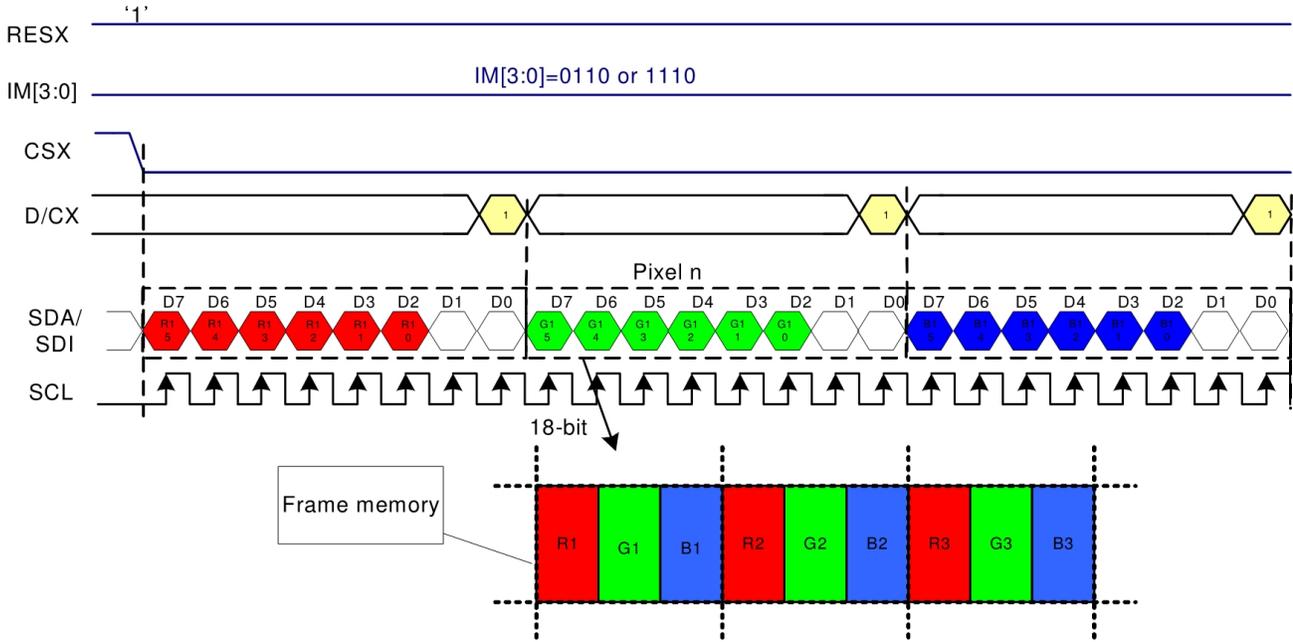
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-=' Don't care – Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



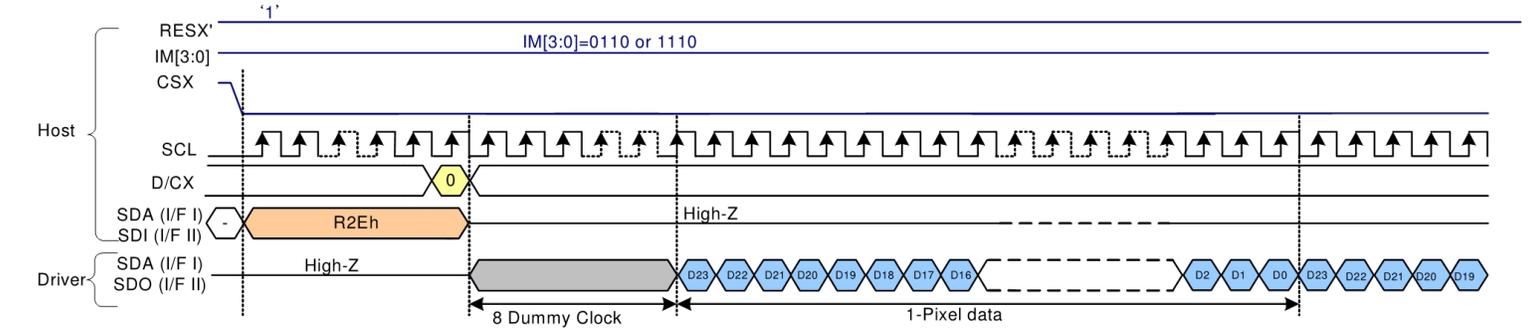
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-=' Don't care – Can be set "0" or "1".

Read data through 4-line SPI mode



Read Data format as below



Note 1: '-=' Don't care – Can be set "0" or "1".

8. Command

8.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
No Operation	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Read Display Identification Information	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]							XX	
	1	↑	1	XX	ID2 [7:0]							XX	
	1	↑	1	XX	ID3 [7:0]							XX	
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [31:25]							X	00
	1	↑	1	XX	X	D [22:20]			D [19:16]				61
	1	↑	1	XX	X	X	X	X	X	D [10:8]			00
	1	↑	1	XX	D [7:5]			X	X	X	X	X	00
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	08
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	00
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	RIM	DPI [2:0]			X	DBI [2:0]			06
Read Display Image Format	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	D [2:0]			00
Read Display Signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	00
Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:6]			X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
	1	1	↑	XX	GC [7:0]							01	
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC [15:8]							XX	
	1	1	↑	XX	SC [7:0]							XX	
	1	1	↑	XX	EC [15:8]							XX	
	1	1	↑	XX	EC [7:0]							XX	
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP [15:8]							XX	
	1	1	↑	XX	SP [7:0]							XX	
	1	1	↑	XX	EP [15:8]							XX	
	1	1	↑	XX	EP [7:0]							XX	

Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑		D [17:0]								XX
Color SET	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh
	1	↑	1	XX	0	0	0	R00 [5:0]					XX
	1	↑	1	XX	0	0	0	Rnn [5:0]					XX
	1	↑	1	XX	0	0	0	R31 [5:0]					XX
	1	↑	1	XX	0	0	0	G00 [5:0]					XX
	1	↑	1	XX	0	0	0	Gnn [5:0]					XX
	1	↑	1	XX	0	0	0	G64 [5:0]					XX
	1	↑	1	XX	0	0	0	B00 [5:0]					XX
	1	↑	1	XX	0	0	0	Bnn [5:0]					XX
	1	↑	1	XX	0	0	0	B31 [5:0]					XX
	Memory Read	0	1	↑	XX	0	0	1	0	1	1	1	0
1		↑	1	XX	X	X	X	X	X	X	X	X	XX
1		↑	1		D [17:0]								XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR [15:8]								00
	1	1	↑	XX	SR [7:0]								00
	1	1	↑	XX	ER [15:8]								01
	1	1	↑	XX	ER [7:0]								3F
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA [15:8]								00
	1	1	↑	XX	TFA [7:0]								00
	1	1	↑	XX	VSA [15:8]								01
	1	1	↑	XX	VSA [7:0]								40
	1	1	↑	XX	BFA [15:8]								00
	1	1	↑	XX	BFA [7:0]								00
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP [15:8]								00
	1	1	↑	XX	VSP [7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI [2:0]			X	DBI [2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑		D [17:0]								XX
Read Memory Continue	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1		D [17:0]								XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS [8]	00
	1	1	↑	XX	STS [7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	GTS [9:8]		00
	1	↑	1	XX	GTS [7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	1	↑	XX	DBV [7:0]								00

Read Display Brightness	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	DBV [7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read CTRL Display	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	BCTRL	X	DD	BL	X	X	00
Write Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
	1	1	↑	XX	X	X	X	X	X	X	C [1:0]		00
Read Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	C [1:0]		00
Write CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
	1	1	↑	XX	CMB [7:0]								00
Read CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	0	1	1	1	5Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	CMB [7:0]								00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Module's Manufacture [7:0]								XX
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver Version [7:0]								XX
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	ByPass_MODE	RCM [1:0]		X	VSPPL	HSPL	DPL	EPL	40
Frame Control (In Normal Mode)	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XX	X	X	X	X	X	X	DIVA [1:0]		00
	1	1	↑	XX	X	X	X	RTNA [4:0]				1B	
Frame Control (In Idle Mode)	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XX	X	X	X	X	X	X	DIVB [1:0]		00
	1	1	↑	XX	X	X	X	RTNB [4:0]				1B	
Frame Control (In Partial Mode)	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XX	X	X	X	X	X	X	DIVC [1:0]		00
	1	1	↑	XX	X	X	X	RTNC [4:0]				1B	
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XX	X	X	X	X	X	NLA	NLB	NLC	02
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	VFP [6:0]						02	
	1	1	↑	XX	0	VBP [6:0]						02	
	1	1	↑	XX	0	0	0	HFP [4:0]				0A	
	1	1	↑	XX	0	0	0	HBP [4:0]				14	

Display Function Control	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XX	X	X	X	X	PTG [1:0]		PT [1:0]		0A
	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]				82
	1	1	↑	XX	X	X	NL [5:0]						27
	1	1	↑	XX	X	X	PCDIV [5:0]						XX
Entry Mode Set	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XX	X	X	X	X	0	GON	DTE	GAS	07
Backlight Control 1	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	X	X	X	X	TH_UI [3:0]				04
Backlight Control 2	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	TH_MV [3:0]				TH_ST [3:0]				B8
Backlight Control 3	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	X	X	X	X	DTH_UI [3:0]				04
Backlight Control 4	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	DTH_MV [3:0]				DTH_ST [3:0]				C9
Backlight Control 5	0	1	↑	XX	1	0	1	1	1	1	0	0	BCh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	DIM2 [3:0]				X	DIM1 [2:0]			44
Backlight Control 7	0	1	↑	XX	1	0	1	1	1	1	1	0	BEh
	1	1	↑	XX	PWM_DIV [7:0]								0F
Backlight Control 8	0	1	↑	XX	1	0	1	1	1	1	1	1	BFh
	1	1	↑	XX	X	X	X	X	X	LEDONR	LEDONPOL	LEDPWMOPL	00
Power Control 1	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
	1	1	↑	XX	X	X	VRH [5:0]					26	
Power Control 2	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	X	X	X	X	X	BT [2:0]			00
VCOM Control 1	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
	1	1	↑	XX	X	VMH [6:0]						31	
	1	1	↑	XX	X	VML [6:0]						3C	
VCOM Control 2	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
	1	1	↑	XX	nVM	VMF [6:0]						C0	
NV Memory Write	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h
	1	1	↑	XX	X	X	X	X	X	PGM_ADR [2:0]			00
	1	1	↑	XX	PGM_DATA [7:0]								XX
NV Memory Protection Key	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h
	1	1	↑	XX	KEY [23:16]								55
	1	1	↑	XX	KEY [15:8]								AA
	1	1	↑	XX	KEY [7:0]								66
NV Memory Status Read	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	ID2_CNT [2:0]			X	ID1_CNT [2:0]			XX
	1	↑	1	XX	BUSY	VMF_CNT [2:0]			X	ID3_CNT [2:0]			XX

Read ID4	0	↑	1	XX	1	1	0	1	0	0	1	1	D3h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	0	0	0	0	0	0	00
	1	↑	1	XX	1	0	0	1	0	0	1	1	93
	1	↑	1	XX	0	1	0	0	0	0	0	1	41
Positive Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h
	1	1	↑	XX	X	X	X	X	VP0 [3:0]			08	
	1	1	↑	XX	X	X	VP1 [5:0]					0E	
	1	1	↑	XX	X	X	VP2 [5:0]					12	
	1	1	↑	XX	X	X	X	X	VP4 [3:0]			05	
	1	1	↑	XX	X	X	X	VP6 [4:0]				03	
	1	1	↑	XX	X	X	X	X	VP13 [3:0]			09	
	1	1	↑	XX	X	VP20 [6:0]						47	
	1	1	↑	XX	VP36 [3:0]			VP27 [3:0]			86		
	1	1	↑	XX	X	VP43 [6:0]						2B	
	1	1	↑	XX	X	X	X	X	VP50 [3:0]			0B	
	1	1	↑	XX	X	X	X	VP57 [4:0]				04	
	1	1	↑	XX	X	X	X	X	VP59 [3:0]			00	
	1	1	↑	XX	X	X	VP61 [5:0]					00	
	1	1	↑	XX	X	X	VP62 [5:0]					00	
	1	1	↑	XX	X	X	X	X	VP63 [3:0]			00	
	Negative Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	1
1		1	↑	XX	X	X	X	X	VN0 [3:0]			08	
1		1	↑	XX	X	X	VN1 [5:0]					1A	
1		1	↑	XX	X	X	VN2 [5:0]					20	
1		1	↑	XX	X	X	X	X	VN4 [3:0]			07	
1		1	↑	XX	X	X	X	VN6 [4:0]				0E	
1		1	↑	XX	X	X	X	X	VN13 [3:0]			05	
1		1	↑	XX	X	VN20 [6:0]						3A	
1		1	↑	XX	VN36 [3:0]			VN27 [3:0]			8A		
1		1	↑	XX	X	VN43 [6:0]						40	
1		1	↑	XX	X	X	X	X	VN50 [3:0]			04	
1		1	↑	XX	X	X	X	VN57 [4:0]				18	
1		1	↑	XX	X	X	X	X	VN59 [3:0]			0F	
1		1	↑	XX	X	X	VN61 [5:0]					3F	
1		1	↑	XX	X	X	VN62 [5:0]					3F	
1	1	↑	XX	X	X	X	X	VN63 [3:0]			0F		
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1 st Parameter	1	1	↑	XX	RCA0 [3:0]			BCA0 [3:0]			XX		
:	1	1	↑	XX	RCAx [3:0]			BCAx [3:0]			XX		
16 th Parameter	1	1	↑	XX	RCA15 [3:0]			BCA15 [3:0]			XX		
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1 st Parameter	1	1	↑	XX	RFA0 [3:0]			BFA0 [3:0]			XX		
:	1	1	↑	XX	RFAx [3:0]			BFAx [3:0]			XX		
64 th Parameter	1	1	↑	XX	RFA63 [3:0]			BFA63 [3:0]			XX		
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	X	BGR_EOR	X	X	WEMODE	01
	1	1	↑	XX	X	X	EPF [1:0]		X	X	MDT [1:0]		00
	1	1	↑	XX	X	X	ENDIAN	X	DM [1:0]		RM	RIM	00

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP

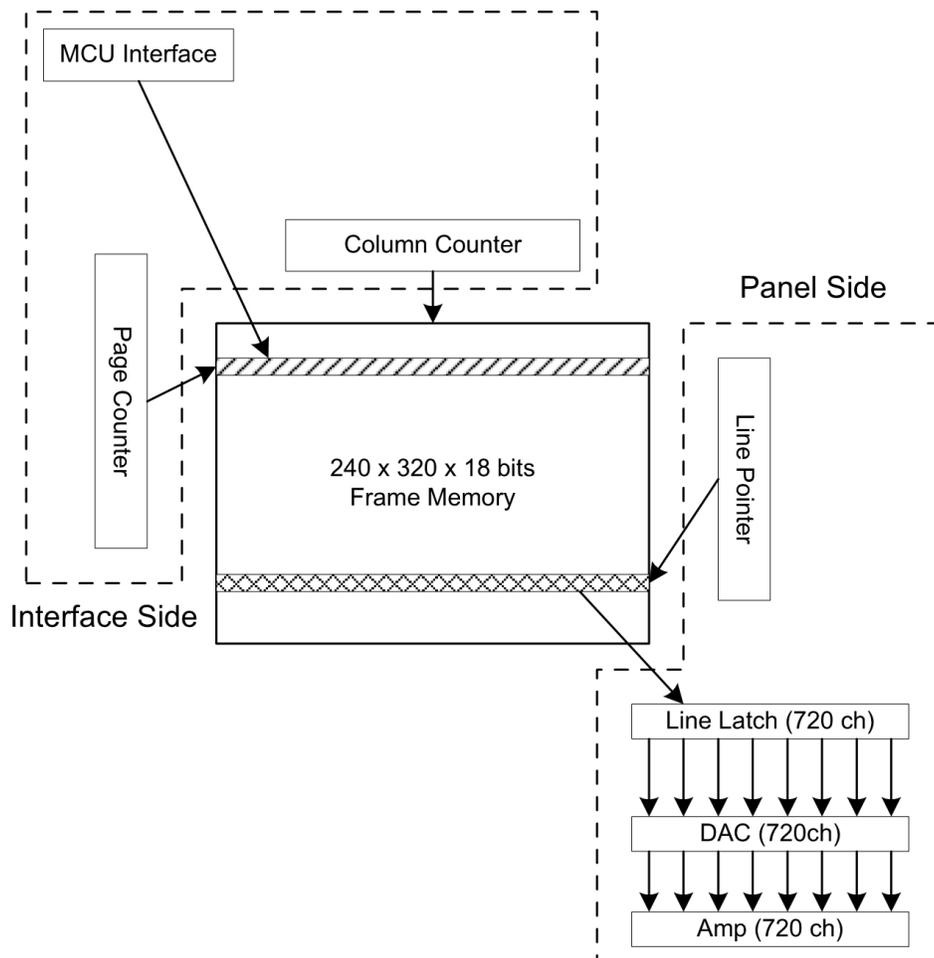
(00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9341 is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.

9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.



9.2. Memory to Display Address Mapping

9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)

