

SONY CXK58256P/M 10/10L/12/12L/15/15L

32K-word × 8 bit High Speed CMOS Static RAM

Preliminary

Description

The CXK58256P/M is a 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. The CXK58256P/M is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Low power standby: 10 μ W(Typ.)—L-version
50 μ W(Typ.)—Standard Version
- Low power operation: 40mW(Typ.)—L-version
50mW(Typ.)—Standard Version
- Fast access time: 100ns/120ns/150ns (Max.)
- Single +5V supply
- Fully static memory ... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: 3-state output
- Low voltage data retention: 2.0V (Min.)
- Directly TTL compatible: All inputs and outputs

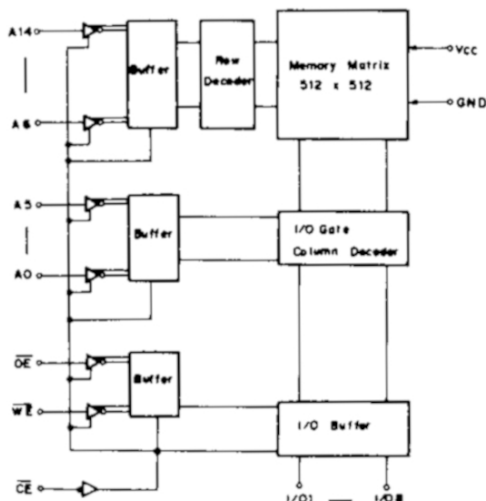
Function

32,768-word × 8 bit static RAM

Structure

Silicon gate CMOS IC

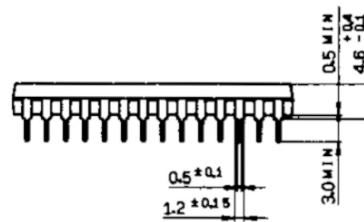
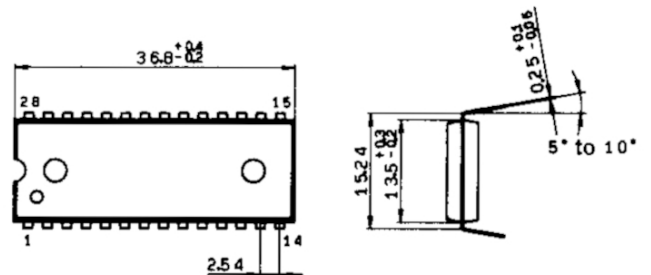
Block Diagram



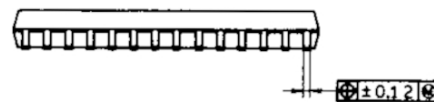
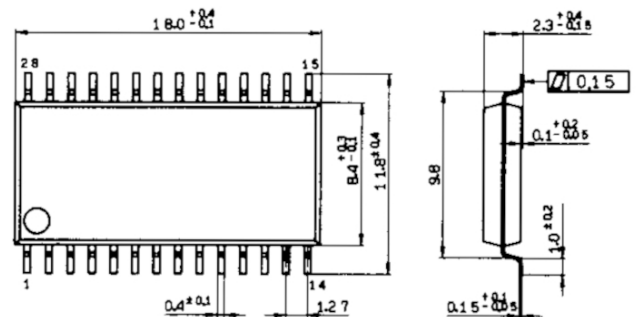
Package Outline

Unit: mm

CXK58256P 28 Pin DIP

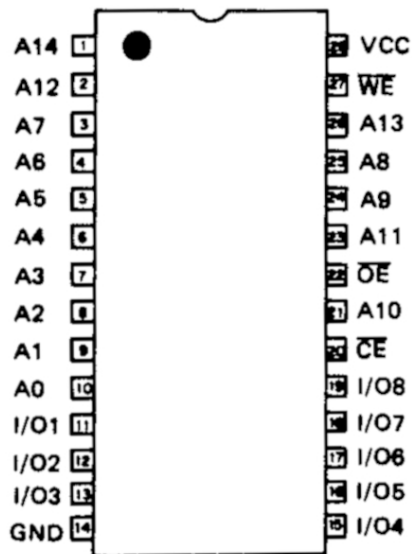


CXK58256M 28 Pin MFP



Note) All Typical values are measured under the conditions
Vcc=5.0V and Ta=25°C.

Pin Configuration (TOP VIEW)



Symbol	Description
A0 to A14	Address Input
I/O1 to I/O8	Data Input Output
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
Vcc	Power Supply
GND	Ground

Absolute Maximum Ratings

($T_a=25^\circ\text{C}$, GND=0V)

Item	Symbol	Rating	Unit
Power Supply Voltage	Vcc	-0.5 to +7.0	V
Input Voltage	V_{IN} (Note)	-0.5 to Vcc+0.5	V
Input and Output Voltage	$V_{\text{I/O}}$ (Note)	-0.5 to Vcc+0.5	V
Allowable Power Dissipation	P_D	CXK58256P	1.0
		CXK58256M	0.7
Operating Temperature	T_{opr}	0 to +70	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering Temperature	T_{solder}	260.10	$^\circ\text{C}\cdot\text{sec}$

Note) During transitions, the inputs may undershoot to -3V for period less than 50ns.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not Selected	High Z	I_{SB1} , I_{SB2}
L	H	H	Output Disable	High Z	I_{CC1} , I_{CC2}
L	L	H	Read	D out	I_{CC1} , I_{CC2}
L	X	L	Write	D in	I_{CC1} , I_{CC2}

Note) X: "H" or "L"

DC Recommended Operating Conditions ($T_a=0$ to $+70^\circ\text{C}$, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	Vcc	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

Note) During transitions, the inputs may undershoot to -3V for period less than 50 ns.

DC and Operating Characteristics

(V_{CC}=5V±10%, GND=0V, T_a=0 to +70°C)

Item	Symbol	Test condition	CXK58256P/M -10/12/15			CXK58256P/M -10L/12L/15L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage Current	I _{LI}	V _{IN} =GND to V _{CC}	-1	-	1	-1	-	1	μA
Output Leakage Current	I _{LO}	V _{I/O} =GND to V _{CC} , $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$	-1	-	1	-1	-	1	μA
Operating Power Supply Current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	-	10	20	-	8	15	mA
		$\overline{CE}=0.2V$ V _{IN} =0.2V or V _{CC} -0.2V	-	5	10	-	3	7	mA
Average Operating Current	I _{CC2}	Cycle=Min, Duty=100% I _{OUT} =0mA	-	35	55	-	30	50	mA
Standby Current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	-	0.01	1	-	0.002	0.1	mA
	I _{SB2}	$\overline{CE}=V_{IH}$	-	0.4	3	-	0.2	2	mA
Output High Voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	-	-	0.4	V

Capacitance

(T_a=25°C, f=1 MHz)

Item	Test condition	Symbol	Min.	Max.	Unit
Input Capacitance	V _{IN} =0V	C _{IN}	-	8	pF
Input/Output Capacitance	V _{I/O} =0V	C _{I/O}	-	6	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC Test conditions** (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Condition
Input Pulse High Level	V _{IH} =2.2V
Input Pulse Low Level	V _{IL} =0.8V
Input Rise Time	t _R =5ns
Input Fall Time	t _F =5ns
Input and Output Reference Level	1.5V
Output Load	C _L *=100pF, 1TTL

* C_L includes scope and jig capacitances.

(1) Read Cycle

Item	Symbol	CXK58256P/M -10/10L		CXK58256P/M -12/12L		CXK58256P/M -15/15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	trc	100	—	120	—	150	—	ns
Address Access Time	tAA	—	100	—	120	—	150	ns
Chip Enable Access Time (\overline{CE})	tCO	—	100	—	120	—	150	ns
Output Enable to Output Valid	toE	—	50	—	60	—	70	ns
Output Hold from Address Change	toH	10	—	10	—	10	—	ns
Chip Enable to Output in Low Z (\overline{CE})	tlZ	10	—	10	—	10	—	ns
Output Enable to Output in Low Z (\overline{OE})	tolZ	5	—	5	—	5	—	ns
Chip Disable to Output in High Z (\overline{CE})	thZ	—	35	—	40	—	50	ns
Output Disable to Output in High Z (\overline{OE})	toHZ	—	35	—	40	—	50	ns

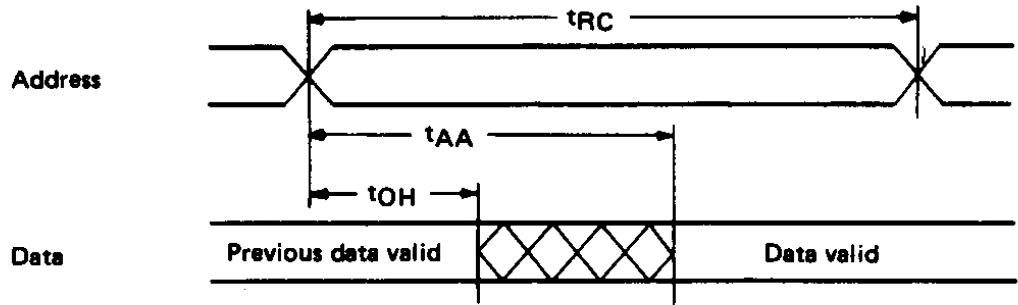
(2) Write Cycle

Item	Symbol	CXK58256P/M -10/10L		CXK58256P/M -12/12L		CXK58256P/M -15/15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	tWC	100	—	120	—	150	—	ns
Address Valid to End of Write	tAW	80	—	100	—	100	—	ns
Chip Enable to End of Write	tcW	80	—	100	—	100	—	ns
Data to Write Time Overlap	tdW	40	—	50	—	60	—	ns
Data Hold from Write Time	tdH	0	—	0	—	0	—	ns
Write Pulse Width	tWP	70	—	80	—	90	—	ns
Address Set up Time	tAS	0	—	0	—	0	—	ns
Write Recovery Time (\overline{WE})	tWR	0	—	0	—	0	—	ns
Write Recovery Time (\overline{CE})	tWR1	0	—	0	—	0	—	ns
Output Active from End of Write	tOW	10	—	10	—	10	—	ns
Write to Output in High Z	tWHZ	—	30	—	30	—	40	ns

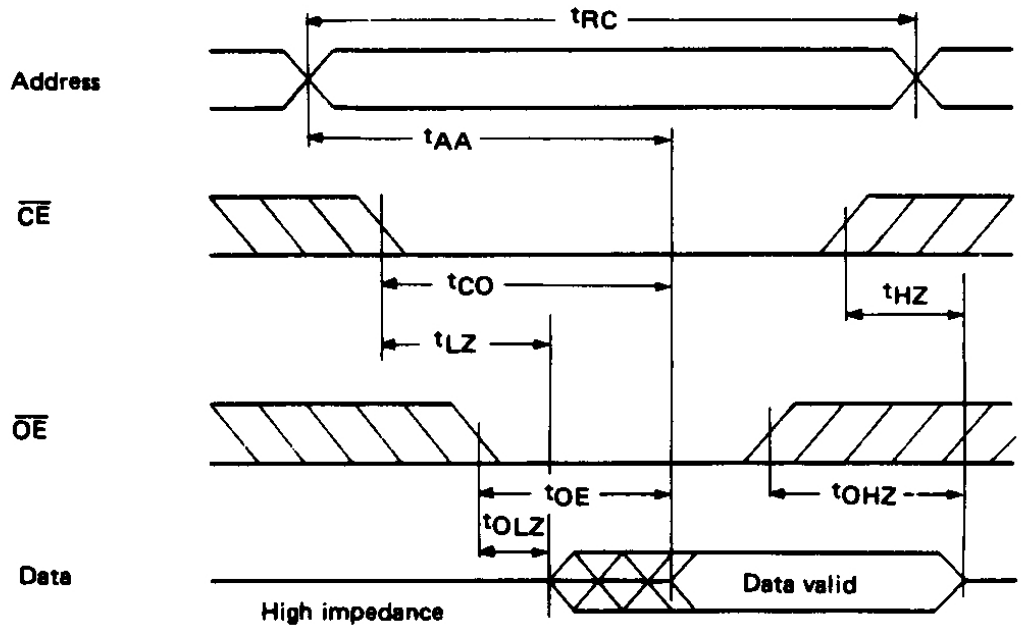
Timing Waveform

(1) Read Cycle

- Read cycle No. 1 [$\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$]

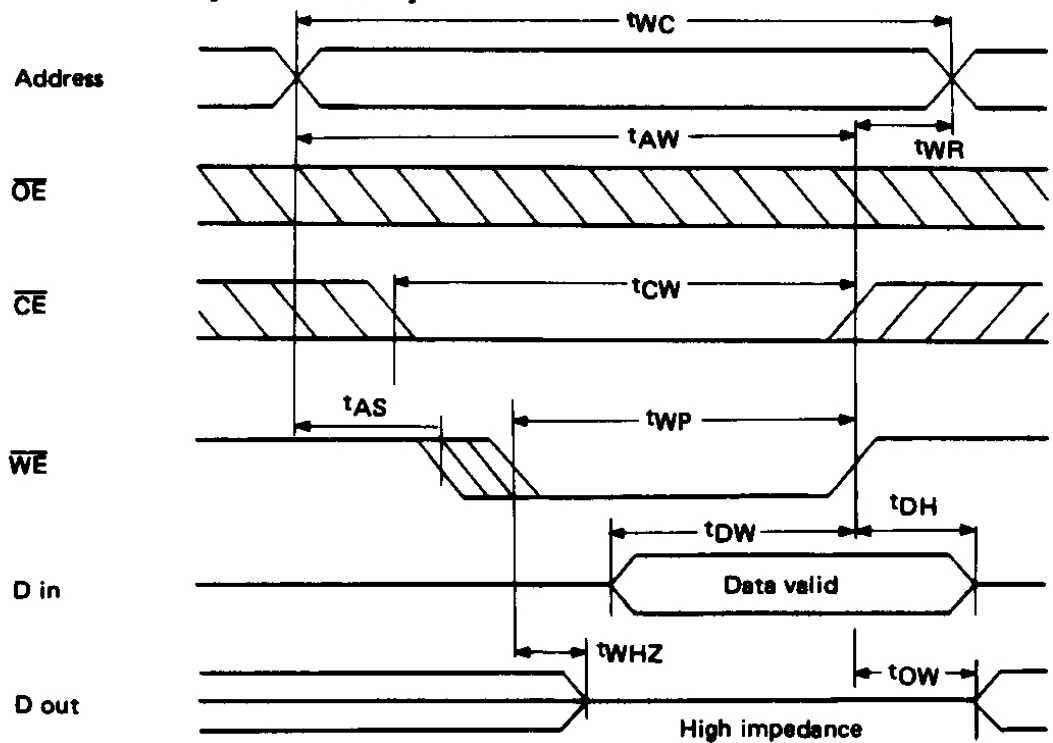


- Read cycle No. 2 [$\overline{WE}=V_{IH}$]

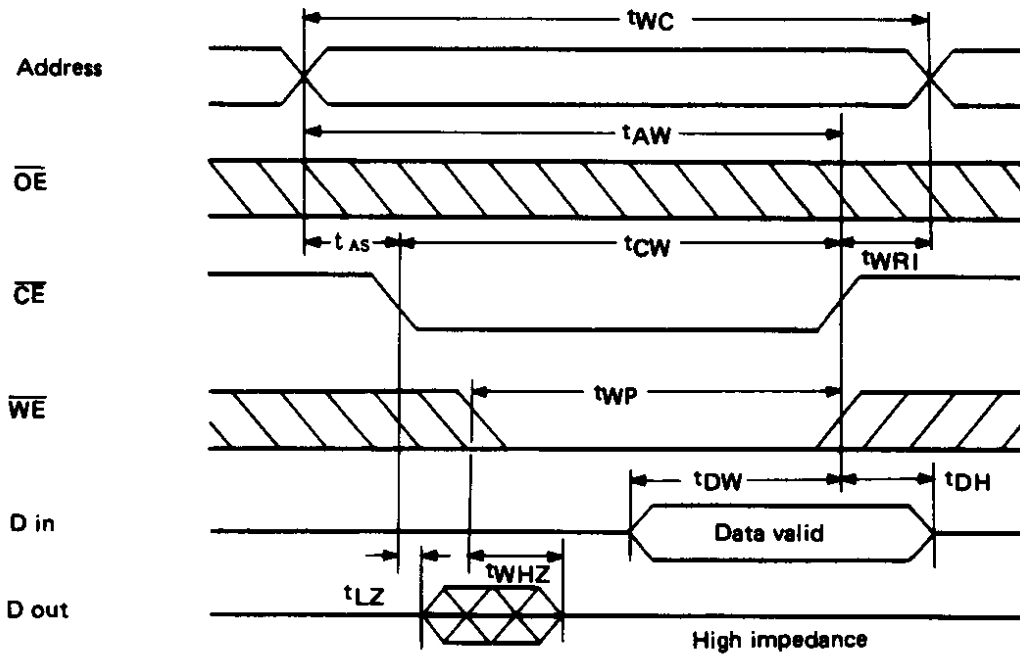


(2) Write Cycle

- Write cycle No. 1 [\overline{WE} control]



• Write cycle No. 2 [\overline{CE} control]



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

(Ta=0 to 70°C)

Item	Symbol	Test condition	CXK58256P/M -10/12/15			CXK58256P/M -10L/12L/15L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data Retention Voltage	V _{DR}	*1	2.0	5.0	5.5	2.0	5.0	5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} =3.0V *1	—	5	500	—	1	50	μA
	I _{CCDR2}	V _{CC} =2.0to5.5V *1	—	0.01	1.0	—	0.002	0.1	mA
Data Retention Set up Time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery Time	t _R		t _{RC} *2	—	—	t _{RC} *2	—	—	ns

*1 1) $\overline{CE} \geq V_{CC} - 0.2V$

*2 t_{RC} : Read Cycle Time

Data Retention Waveform

