Triple-port dynamic RAM fuels graphic displays

A novel video RAM from NEC helps designers come up with the next generation of fast displays. The main part of the μPD42232C/LA is an array of dynamic RAM cells organized as 32 kwords by 8 bits and an asynchronous 128-word-by-8-bit serial read/write buffer. Depending on the version, the random access port will access at either 100, 120, or 150 ns while the serial-access ports will handle data at 30, 40, or 60 ns per bit, respectively.

The central-memory array can transfer data in any of three ways to the display: through an 8-bit common I/O port; by means of a serial pixel-access port; or through a serial 128-word-by-8-bit I/O buffer. By combining common I/O and pixel-access ports, designers can effect a matrix-frame buffer architecture to access pixels and planes on alternate cycles. Both ports have two operating modes: the 8-bit common I/O port acts as a standard RAM port or as an 8-bit port for transferring data into the on-chip bit mask register. In one mode, data from the pixel-access port flows serially. In the other, Chip-Select mask data can be sent from an external source and loaded right into the Chip-Select mask register.

The third port, the serial I/O buffer, can be set up as a dual-buffer organization: two 64-by-8 serial-data registers. Each serial register can be loaded with data from the main memory array, either separately or at the same time as the other register.

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Graphics display controller simplifies programming

Offering the best of all worlds is a general-purpose display controller chip that's easy to use yet powerful enough to relieve a host processor of most graphics, text, and display chores. The μPD72120 advanced graphics-display controller, or AGDC, has a powerful instruction set that carries out graphics drawing, filling, copying, and controlling functions with one embedded command for each.

Unlike most other graphics processors, it doesn't need programming to perform each drawing function, nor does it need a development system. The drawing and display controls are on chip, saving valuable board space and reducing cost.

On top of that, the chip's hardware is flexible enough to arbitrate among a display-memory bus, a DMA-controller interface, and an 8- or 16-bit data bus for host-processor interfacing. It easily handles all external video, static, and dynamic RAMs. The controller can draw lines or fill areas at 500 ns/pixel.

To increase drawing speed, the controller relies on a pipelined preprocessor and separate drawing processor. While the drawing processor writes to or modifies the display memory, the preprocessor transforms the coordinates and prepares data. Also, the processing speed and the video timing are independent of each other, which is unusual for a graphics chip.

Separate clock inputs control the different operations. The SCLK pin drives the raster-scan timing generator; the CLK pin drives the preprocessor and drawing processor. The CLK frequency can run as high as 8 MHz, and SCLK can go as high as the CLK's frequency.

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μPD42232 Triple-port DRAM for graphics application & μPD72120 AGDC (Advanced Graphics Display Controller)