

NEC μ PD7220/72120 Related Public Documents

- [ISSCC](#) (International Solid-State Circuit Conference)
- [\$\mu\$ PD7220A User's Manual](#)
- Nikkei Electronics Magazine ([\$\mu\$ PD7220](#))
- Transistor Gijutsu (Technology) Magazine ([\$\mu\$ PD7220](#))
- Transistor Gijutsu (Technology) Magazine ([\$\mu\$ PD7220A](#))
- Nikkei Electronics Magazine ([\$\mu\$ PD72120](#))
- [\$\mu\$ PD72120 User's Manual](#)

Go to <https://www.oguchi-rd.com/LSI%20products.php> to get more detailed NEC μ PD7220/72120 related information such as;

"Logic Schematics", "Design Notes", "Evaluation Board Schematics", "Evaluation Software", "Silicon Die Photos", "Newspaper", "Magazine", and so forth.

Go to <https://www.oguchi-rd.com/patents.php> to get patent information including NEC μ PD7220/72120 related patents.

WEDNESDAY, THURSDAY AND FRIDAY / FEBRUARY 18-19-20, 1981

1981 IEEE INTERNATIONAL

Volume Twenty-Four



1981 DIGEST of TECHNICAL PAPERS

SOLID-STATE CIRCUITS CONFERENCE

SPONSORS: IEEE SOLID-STATE CIRCUITS COUNCIL / IEEE NEW YORK SECTION / UNIVERSITY OF PENNSYLVANIA

Feb. 19, 1981: 1:30 P.M.—5:00 P.M.

SESSION XIII: Advanced Circuit Applications

Ballroom E

THPM 13.1:	A Monolithic Power-Spectrum Centroid Detector L. Gerzberg, N.C.C. Lu and J.D. Meindl	164
THPM 13.2:	A Fully Integrated RF Actuated Battery Controller H.V. Allen and J.W. Knutti	166
THPM 13.3:	Biomedical Microprocessor with Analog I/O J.A. Berkman and J.W.L. Prak	168
THPM 13.4:	A Single-Chip Graphic Display Controller T. Oguchi, M. Higuchi, T. Uno, M. Kamaya and M. Suzuki	170
THPM 13.5:	A Single-Chip 20Mb Fiberoptic Receiver Circuit D.L. Rogers	172
THPM 13.6:	Self-Testing VLSI R.W. Heckelman and D.K. Bhavsar	174
THPM 13.7:	A Self-Testing ROM Device U. Theus and H. Leutiger	176

SESSION XIII: ADVANCED CIRCUIT APPLICATIONS

THPM 13.4: A Single-Chip Graphic Display Controller

Tetsuji Oguchi, Misao Higuchi, Takashi Uno, Michinori Kamaya and Munekazu Suzuki

Nippon Electric Co., Ltd.

Kawasaki, Japan

IN RECENT YEARS, implementations of systems that require a large capacity memory such as the graphic display terminal have been proliferating and becoming less expensive, helped by cost reduction and availability of greater size of semiconductor memories. Also, in the field of graphic display technology, the raster scan CRT is obtaining more popularity than the conventional storage tube or the direct scan CRT, due to its color capability, and ease of control with the digital computers. Along with such progress, there is a strong demand from terminal manufacturers for a powerful, intelligent and cost-effective graphic display controller device to handle a variety of complicated display control functions less expensively. To meet such growing demands, a single-chip Graphic Display Controller (GDC), with capability for both alphanumeric and graphic display has been developed for sophisticated raster-scan color CRT display terminals.

As a highly intelligent peripheral controller, with data manipulation algorithms, the GDC performs all of the complicated control and high-speed processing functions required for the sophisticated alphanumeric and graphic display terminals.

Major functions implemented include direct control and refresh of 256K word x 16b (or four planes of 1,024 x 1,024 dot) display memory, continuous dot address calculation, the drawing of graphics at a speed of 800ns/dot, display address control for flexible zooming/panning and scrolling, raster-scan synchronization, DMA control, etc., which are performed without CPU intervention.

The GDC directly and fully controls, by itself, the display memory address/data without CPU assistance. As the display memory can be placed separate from the main memory, different from the conventional so-called video RAM scheme, the GDC together with display memory and its control circuitry can simply be considered as an I/O mapped functional block in the system. This configuration provides system designers with a simple approach, in system design and expansion, to the inclusion of the display features. Other built-in GDC features, such as dynamic RAM refresh control and high-grade memory-to-memory DMA control, further simplify system design and enhance system functionality without additional hardware, as shown in Figure 1.

Functioning as both display and drawing processor, the GDC provides system simplification and performance improvement compared with that available with conventional approaches using standard microprocessors and sequential algorithms. The GDC also allows for flexible programming of display features to meet varied terminal design requirements.

Figure 2 shows the GDC die divided into functional blocks. Judging drawing direction and start/end points, and calculating dot/word address and displacement, the drawing control section performs dot-by-dot continuous drawing of graphics, such as line, rectangle, arc/circle and graphics text, at a speed of 800ns/dot

with 5MHz operation (or 4 clocks of one Read/Modify/Write cycle per dot).

This data manipulation and drawing speed improvement, more than 1,000 times faster for a circle and 10 times for a line than with the conventional approach, has been achieved by means of two techniques. One is the simple pre-manipulation of drawing parameters by the CPU, thereby eliminating time-consuming trigonometric calculations or multiplications from the GDC. The other is the use of unique algorithms that require only ten sets of adders/subtractors and two bit-shifters.

The total 256K word x 16b display memory can be directly controlled in the graphic mode, with 18 address lines and 16 bi-directional data lines used in a time-shared manner, allowing for Read/Modify/Write drawing operation. These lines are used differently in the character mode to allow for character generator addressing and cursor/attribute-blink control. An 8b refresh counter and logics are also contained on chip to perform memory refresh, stealing horizontal blanking periods.

The RAS signal provided from the GDC can be used for multi-timing controls such as address latch enable, generation of RAS and CAS signals for dynamic RAMs of the display memory, and load timing control of the parallel-serial shift register that generates the serial video signal. During zoomed display operation, the RAS signal and the display address output are automatically prolonged as long as specified with the zooming magnifier parameter.

The bidirectional FIFO stores up to 16bytes of command/parameter list from the CPU, and transfers display memory data and other information to the CPU, allowing for independent CPU interface and minimal CPU attention, while the GDC is devoted to drawing/display operations.

All of the GDC operations, including CRT synchronization and RAM refresh are flexibly programmable with 21 available commands. The commands also program various drawing/display and other operations such as zooming, panning, scrolling, screen partitioning, graphic pattern/text definition, pattern modification, slanting, cursor display, cursor and light pen position read, master-slave definition for multi-GDC operation, and cycle-stealing DMA between main memory and display memory at 4 clocks/byte maintaining refresh operation.

By defining the display memory plane wider than the CRT screen area in horizontal and/or vertical direction, smooth scrolling can be performed on the CRT with simple command operations without rewriting the display memory. A command is prepared to enable flexible scrolling such as dot-by-dot, line-by-line and all-direction scroll.

Flexible screen partitioning can also be performed by simply sending commands to the GDC. The CRT screen can be partitioned horizontally into two areas in graphic display mode and

up to four areas in character display mode.

For drawing of an 8-dot x 8-dot free graphic text pattern or a 16-dot free line pattern in the display memory, a text write command and an on-chip 8byte RAM are prepared. Using this feature and with continuous graphics text drawing, area fill drawing can be performed for a desired rectangular area previously specified by commands.

The display memory contents are rewritten by the GDC with Read/Modify/Write operation. For highly optional display memory modification, the data (dot pattern) read from the display memory can be selectively REPLACed, COMPLEMENTed, SET or RESET inside the GDC with the previously defined dot pattern and then written into the memory. Selective erasure of screen, one of convenient features with the raster scan CRT, is easily realized with the COMPLEMENT modification. With the on-chip MASK register that stores the dot pattern for modification, up to 16 dots can be modified at a time within 800ns of one Read/Modify/Write cycle. This flexible and high-speed modification enables, for example, rapid reset (clear) of the large display memory contents.

DMA is the most appropriate approach for data transfer, especially in graphic display systems. The DMA control logic installed in the GDC provides versatile DMA features designed for graphic systems. Maintaining dynamic RAM refresh for the display

memory, the GDC performs DMA between the main memory and the display memory at 4 clocks/byte in the burst mode, byte to/from double byte conversion in realtime for data transfer between the CPU and the display memory. Also, DMA into/from selective rectangular display memory area which enables prompt transfer or repetition of a specific graphics figure on the display memory plane, cycle-stealing DMA eliminating the effect of flashing from the screen, and flexible address calculation for such DMA operations are available.

The SYNC output pin for raster scan synchronization can be programmed to the SYNC input pin for synchronized multiple GDC operation. This vertical SYNC signal from the master GDC resets and synchronizes the slave GDC to the frame scanning start point. The SYNC input can also be used for varied applications such as synchronization of the GDC with a TV camera or a home TV.

The device has over 13,000 transistors on a die of approximately 7mm x 7mm, fabricated with the current standard N-channel MOS technology, and is housed in a 40-pin DIP.

Acknowledgments

The authors thank M. Endo and H. Aoyama for their helpful criticism, and S. Ikeda for his advice on the GDC functions.

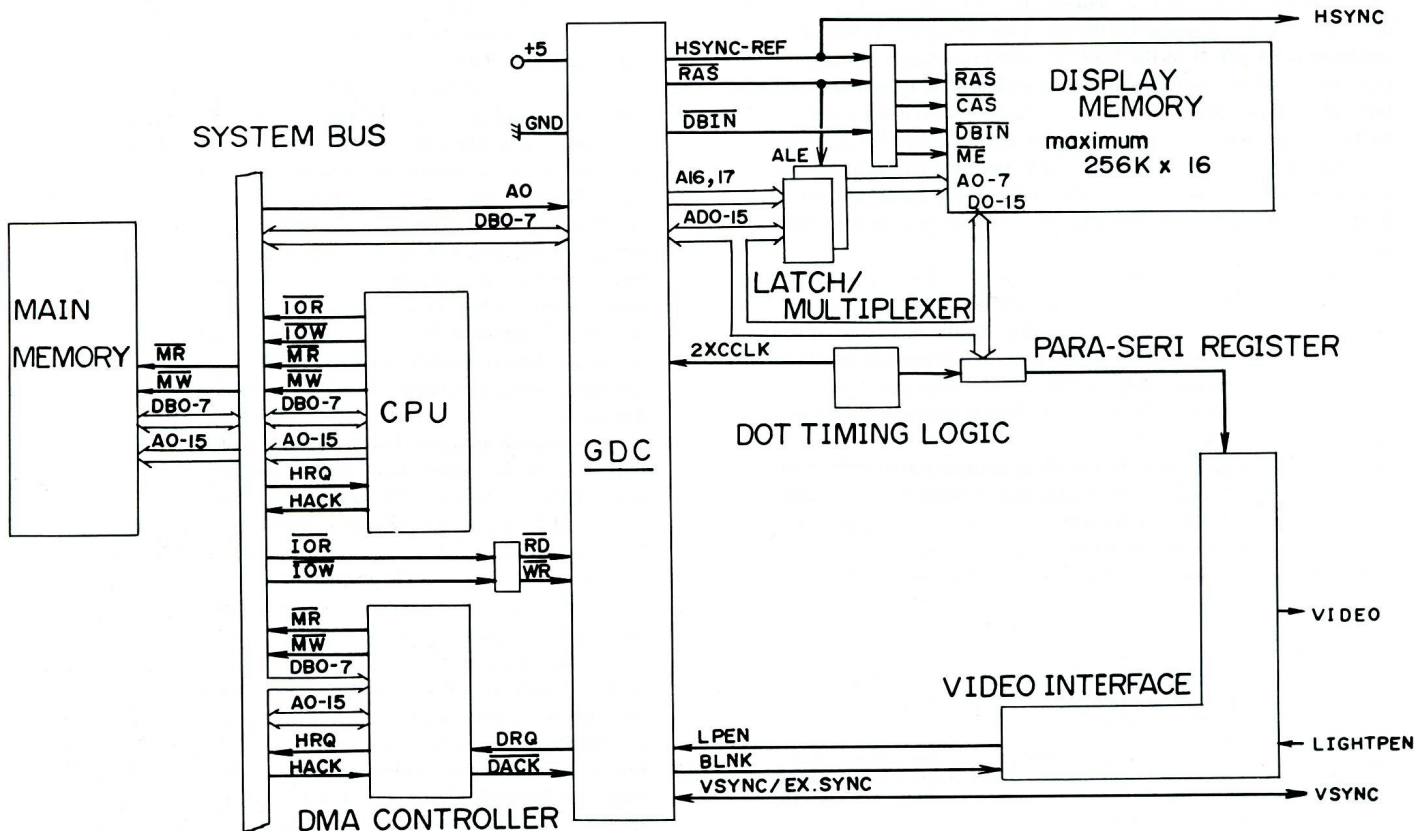


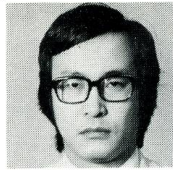
FIGURE 1—System block diagram; graphic display mode.

[See page 270 for Figure 2.]

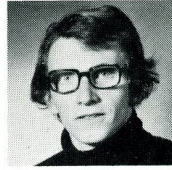
ISSCC 81 Speakers



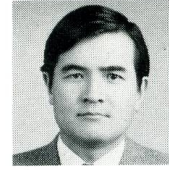
M. Nagata



M. Satou



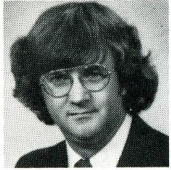
D. Des Camps



N. Horie



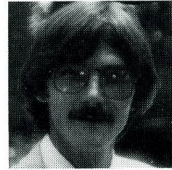
H. Kotecha



R. Webb



A. Kayanuma



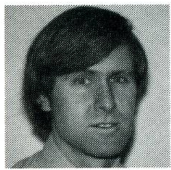
C. Palmer



G. Schaffer



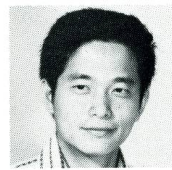
Z. Boyacigiller



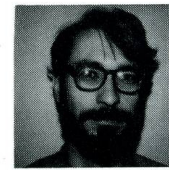
S. Eaton



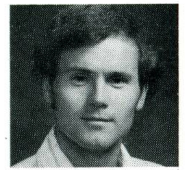
R. Plachno



C-L Jiang



E. Reese



J. Beyers



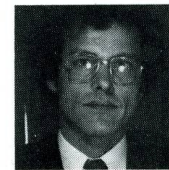
J. Bayliss



R. Schreiber



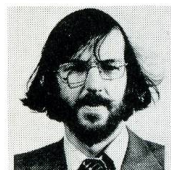
J. Mavor



H. Klar



K-C Hsieh



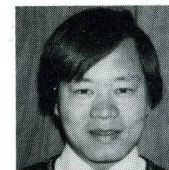
C. Suckling



A. Chu



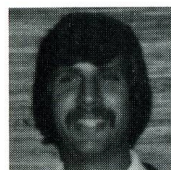
W. Owen



J. Wong



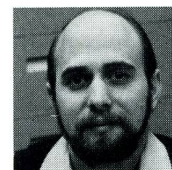
L. Terman



J. Berkman



T. Oguchi



D. Rogers



D. Bhavsar



U. Theus



T. Oguchi

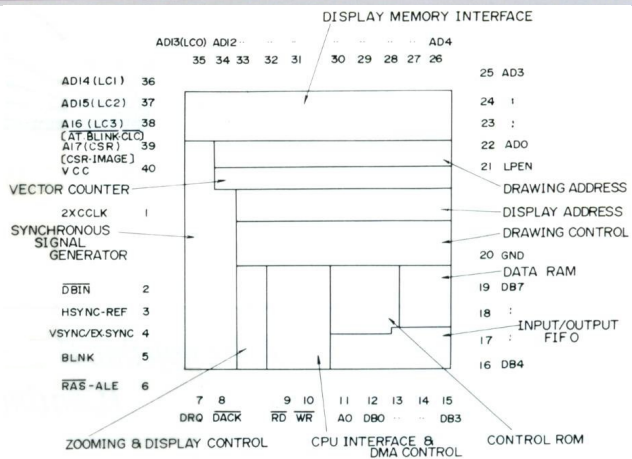
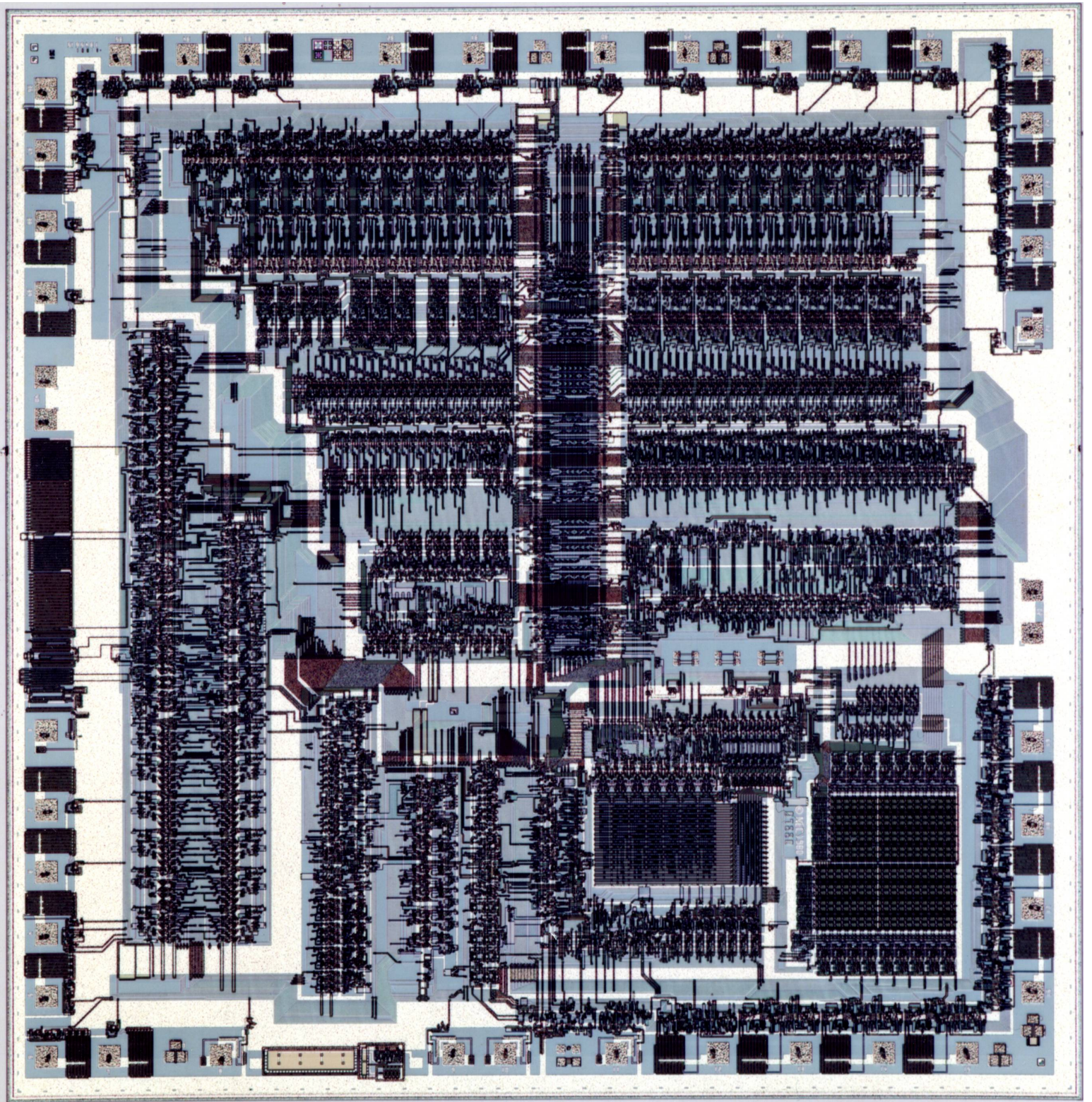


Figure 2-Microphotograph and diagram of μ PD7220