ISSCC (International Solid State Circuit Conference) Papers Co-authored by SanDisk & Toshiba

ISSCC 2002 (2/5/2002 – 2/9/2002)

SESSION 6 NON-VOLATILE MEMORIES AND SRAM

6.4 A 125mm^2 1Gb NAND Flash Memory with 10MB/s Program

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A 125mm^2 1Gb NAND flash uses 0.13μm CMOS. The cell is 0.077μm^2. Chip architecture is changed to reduce chip size and to realize 10.6MB/s throughput for program and 20MB/s for read. An on-chip page copy function provides 9.4MB/s throughput for garbage collection.

ISSCC 2005 (2/6/2005 – 2/10/2005)

SESSION 2 NON-VOLATILE MEMORY

2.1 A 146mm^2 8Gb NAND Flash Memory in 70nm CMOS

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A 146mm^2 8Gb NAND flash memory with 4-level programmed cells is fabricated in a 70nm CMOS technology. A single-sided pad architecture and extended block-addressing scheme without redundancy is adopted for die size reduction. The programming throughput is 6MB/s and is comparable to binary flash memories.

ISSCC 2006 (2/5/2006 – 2/9/2006)

SESSION 7 NONVOLATILE MEMORY

7.7 A 56nm CMOS 99mm^2 8Gb Multi-level NAND Flash Memory with 10MB/s Program Throughput

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Fabricated in 56nm CMOS technology, an 8Gb multi-level NAND Flash memory occupies 98.8mm^2, with a memory cell size of 0.0075μm^2/b. The 10MB/s programming and 93ms block copy are also realized by introducing 8kB page, noise-cancellation circuits, external page copy and the dual VDD scheme enabling efficient use of 1MB blocks.

SESSION 23 NON-VOLATILE MEMORY

23.1 A 34MB/s-Program-Throughput 16Gb MLC NAND with All-Bitline Architecture in 56nm

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A 16Gb MLC (4-state) NAND flash memory achieves a 34MB/s sustained program-throughput rate by using all memory cells available along a selected word-line and by using additional performance-enhancement techniques. The chip operating as an 8Gb binary device achieves a program throughput of over 60MB/s.

23.6 A 120mm^2 16Gb 4-MLC NAND Flash Memory with 43nm CMOS Technology

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A 120mm^2 16Gb MLC NAND flash memory is developed using 43nm CMOS. The area is reduced by more than 9% by applying a 66 NAND strings with a control-gate-driver circuit and power bus on memory cell array. Thus, a 16Gb chip capable of fitting into a microSD memory card.

SESSION 28 NON-VOLATILVE MEMORY & DIGITAL CLOCKING

28.1 A 16Gb 3b/Cell NAND Flash Memory in 56nm with 8MB/s Write Rate

Y. Li[1], *S. Lee[1], Y. Fong[1], F. Pan[1], T-C. Kuo[1], J. Park[1], T. Samaddar[1], H. Nguyen[1], M. Mui[1], K. Htoo[1], T. Kamei[1], M. Higashitani[1], E. Yero[1], G. Kwon[1], P. Kliza[1], J. Wan[1], T. Kaneko[2], H. Maejima[2], H. Shiga[2], M. Hamada[2], N. Fujita[2], K. Kanebako[2], E. Tam[1], A. Koh[1], I. Lu[1], C. Kuo[1], T. Pham[1], J. Huynh[1], Q. Nguyen[1], H. Chibvongodze[1], M. Watanabe[1], K. Oowada[1], G. Shah[1], B. Woo[1], R. Gao[1], J. Chan[1], J. Lan[1], P. Hong[1], L. Peng[1], D. Das[1], D. Ghosh[1], V. Kalluru[1], S. Kulkarni[1], R. Cernea[1], S. Huynh[1], D. Pantelakis[1], C-M. Wang[1], K. Quader[1]*

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A 16Gb 8-level NAND flash chip in 56nm CMOS is fabricated. 8MB/s write performance is achieved, comparable to previously published 4-level NAND performance. This chip provides a significant cost reduction compared to 4-level NAND flash in the same technology.

ISSCC 2009 (2/8/2009 – 2/12/2009)

SESSION 13 FLASH MEMORY

13.4 A 113mm2 32Gb 3b/cell NAND Flash Memory

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A 113mm2 32Gb 3b/cell (8-levels) NAND Flash memory using sub-35nm CMOS technology is developed. This 32Gb Flash die is sufficiently small to fit the microSD memory card format widely adopted in cell phones. This is achieved by a combination of 3b/cell technology and feature-size scaling.

13.6 A 5.6MB/s 64Gb 4b/cell NAND Flash Memory in 43nm CMOS

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A 64Gb 16-level (16LC) NAND flash memory in 43nm CMOS technology is developed. In addition to reducing cost per bit with 4b/cell and improving memory density, 5.6MB/s write performance is achieved using a three-step programming method, ABL sensing, and a sequential-sense concept for read and verify.

ISSCC 2011 (2/20/2011 – 2/24/2011)

SESSION 11 NON-VOLATILE MEMORY SOLUTIONS

11.1 A 151mm2 64Gb MLC NAND Flash Memory in 24nm CMOS Technology

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A 64Gb 2bit/cell NAND Flash memory capable of 14MB/s programming and 266MB/s data transfer is fabricated in 24nm CMOS technology. A 151mm2 die size is realized with a two-plane configuration enabled by low-resistance wordline material and a new bitline hook-up architecture. Program algorithms improve program throughput by 5% and operation current by 6%.

SESSION 1 PLENARY SESSION – INVITED PAPERS

1.1 Flash Memory — The Great Disruptor!

Eli Harari, *Co-Founder, Former CEO, and Chairman (retired)*

SanDisk , Milpitas, CA

Since its commercial introduction in 1988 Flash-memory chip density has advanced through 19 technology nodes, doubling the number of bits per chip with each successive node, with sub 20nm 128Gb Flash chips entering volume production in 2012. This incredible pace has been made possible by the use of the industry-workhorse floating-gate Fowler-Nordheim tunneling cell, first employed in EEPROM, then in NOR and NAND Flash EEPROM. The convergence of NAND Flash with System-Flash and Multi Level Cells (MLC) in the past decade transformed Flash from primarily a code-store memory to a highly-reliable low-cost data-store medium, bringing enormous price reductions and capacity growth to consumers.
Flash became an enabling technology to, as well as a prime beneficiary from, the digital consumer electronics revolution, the rise of the Internet, and the proliferation of wireless mobile devices (most recently, smartphones and tablets), fueling the rapid growth of Flash storage into a $25 billion industry today.
Over the past decade, Flash storage profoundly disrupted analog film, floppy disks, magnetic tapes, micro-drives, and optical CDs. Price elasticity drove rapid growth in consumer demand for Flash units and megabytes. Fierce competition among Flash suppliers ensured an ample supply, and created Flash-card format standards developed by Industry Associations, thereby open to all. Billions of units of SD, micro-SD, USB Flash-drive, and embedded Flash are sold by the industry each year, working seamlessly in literally tens of thousands of different host devices that are used in a broad spectrum of industries and applications.
I have been fortunate to have been involved with the semiconductor Non-Volatile-Memory industry over its 40-year history, first as a device physicist, then as an entrepreneur and businessman. In this presentation, I will provide my personal recollections of some of the past milestones of this industry, and commentary on the profound impact that Flash has had on Consumer Electronics and Mobile Computing. Looking forward, I will briefly discuss the substantial opportunities, as well as the considerable challenges for NAND Flash and post-NAND 3D Flash in the sub-20nm era ahead. I foresee that technology and manufacturing challenges will be overcome through device and architectural innovations, and that in the coming decade NAND and post-NAND 3D Flash will grow to eclipse all other storage media, whether semiconductor, magnetic, or optical, thereby completing a breathtaking odyssey spanning 50 years!

SESSION 25 NON-VOLATILE MEMORY SOLUTIONS

25.1 A 19nm 112.8mm^2 64Gb Multi-Level Flash Memory with 400Mb/s/pin 1.8V Toggle Mode Interface

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25.8 128Gb 3b/Cell NAND Flash Memory in 19nm Technology with 18MB/s Write Rate and 400Mb/s Toggle Mode

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V. Ramachandra[1], T. Kamei[1], M. Higashitani[1], T. Pham[1], M. Honma[2], Y. Watanabe[2], K. Ino[2], B. Le[1], B. Woo[1], K. Htoo[1], T-Y. Tseng[1], L. Pham[1], F. Tsai[1], K-H. Kim[1], Y-C. Chen[1], M. She[1], J. Yuh[1], A. Chu[1], C. Chen[1], R. Puri[1], H-S. Lin[1], Y-F. Chen[1], W. Mak[1], J. Huynh[1], J. Chan[1], M. Watanabe[1], D. Yang[1], G. Shah[1], P. Souriraj[1], D. Tadepalli[1], S. Tenugu[1], R. Gao[1], V. Popuri[1], B. Azarbayjani[1], R. Madpur[1], J. Lan[1], E. Yero[1], F. Pan[1], P. Hong[1], J. Kang[1], F. Moogat[1], Y. Fong[1], R. Cernea[1], S. Huynh[1], C. Trinh[1], M. Mofidi[1], R. Shrivastava[1], K. Quader[1]

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ISSCC 2013 (2/17/2013 – 2/21/2013)

SESSION 12 NONVOLATILE MEMORY SOLUTIONS

12.1 130.7mm[2] 2-Layer 32Gb ReRAM Memory Device in 24nm Technology

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A 64Gb 2bit/cell NAND Flash memory capable of 14MB/s programming and 266MB/s data transfer is fabricated in 24nm CMOS technology. A 151mm^2 die size is realized with a two-plane configuration enabled by low-resistance wordline material and a new bitline hook-up architecture. Program algorithms improve program throughput by 5% and operation current by 6%.

ISSCC 2015 (2/22/2015 – 2/26/2015)

SESSION 7 NON-VOLATILE MEMORY SOLUTIONS

7.1 A Low-Power 64Gb MLC NAND-Flash Memory in 15nm CMOS Technology

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