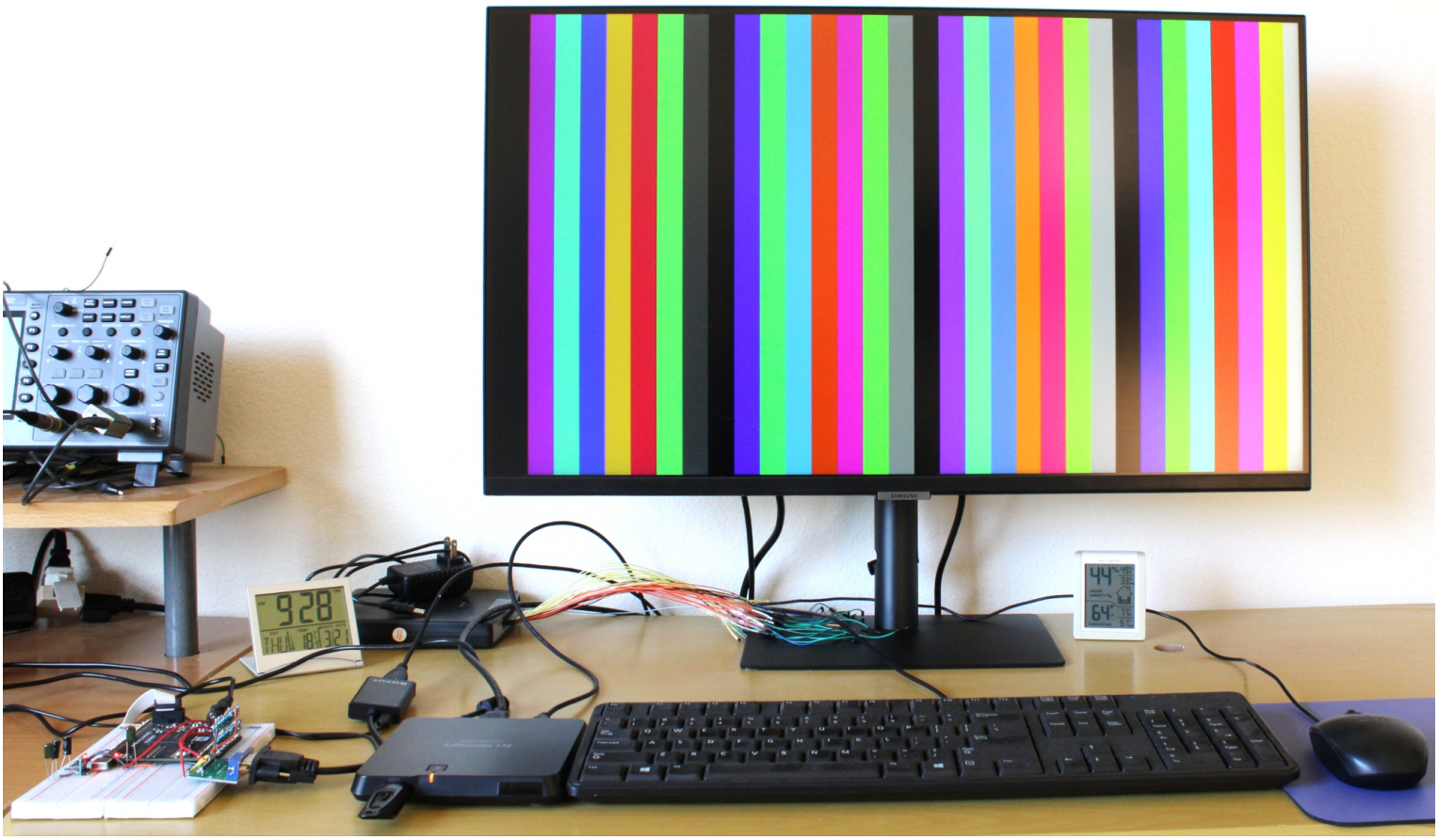
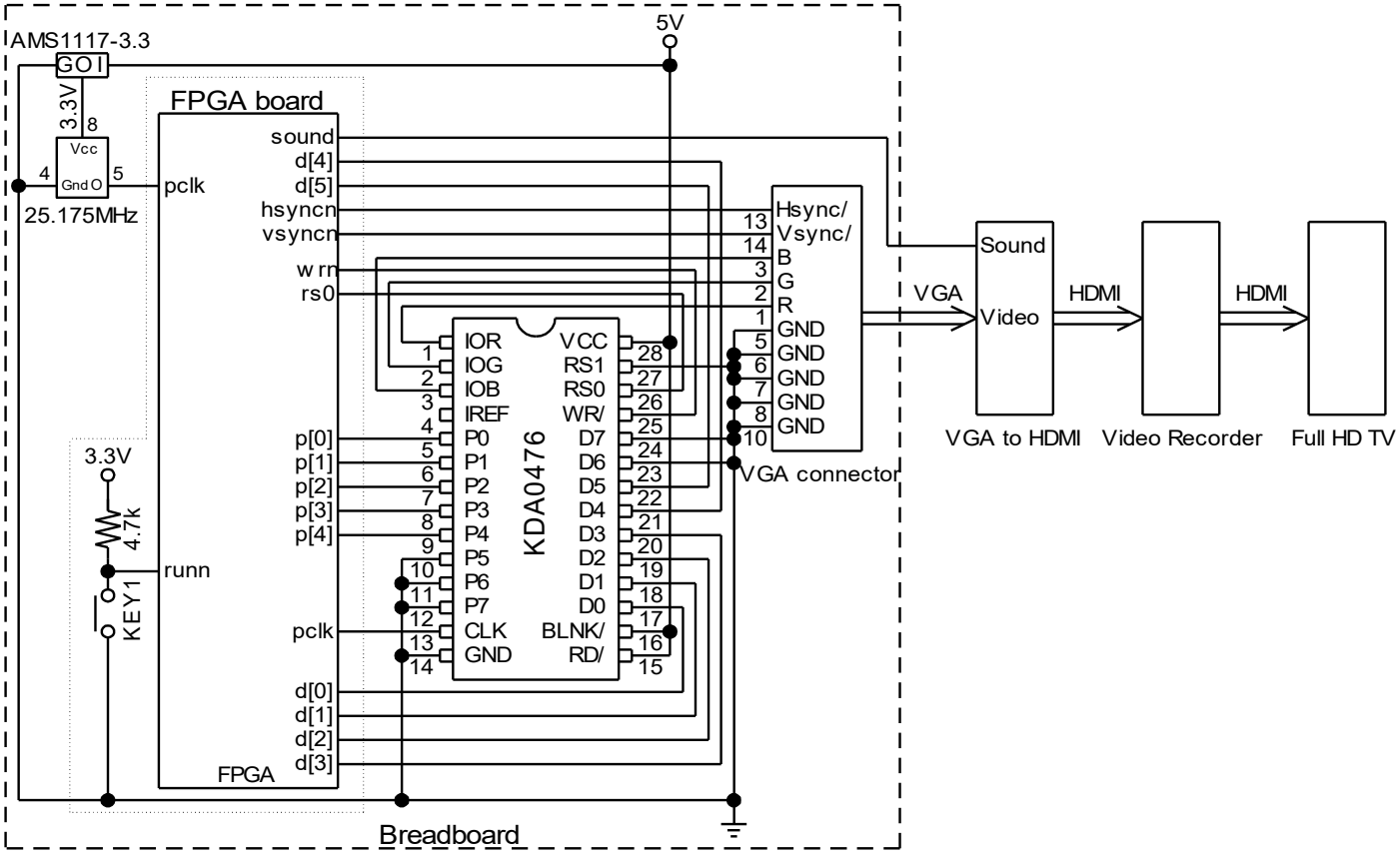
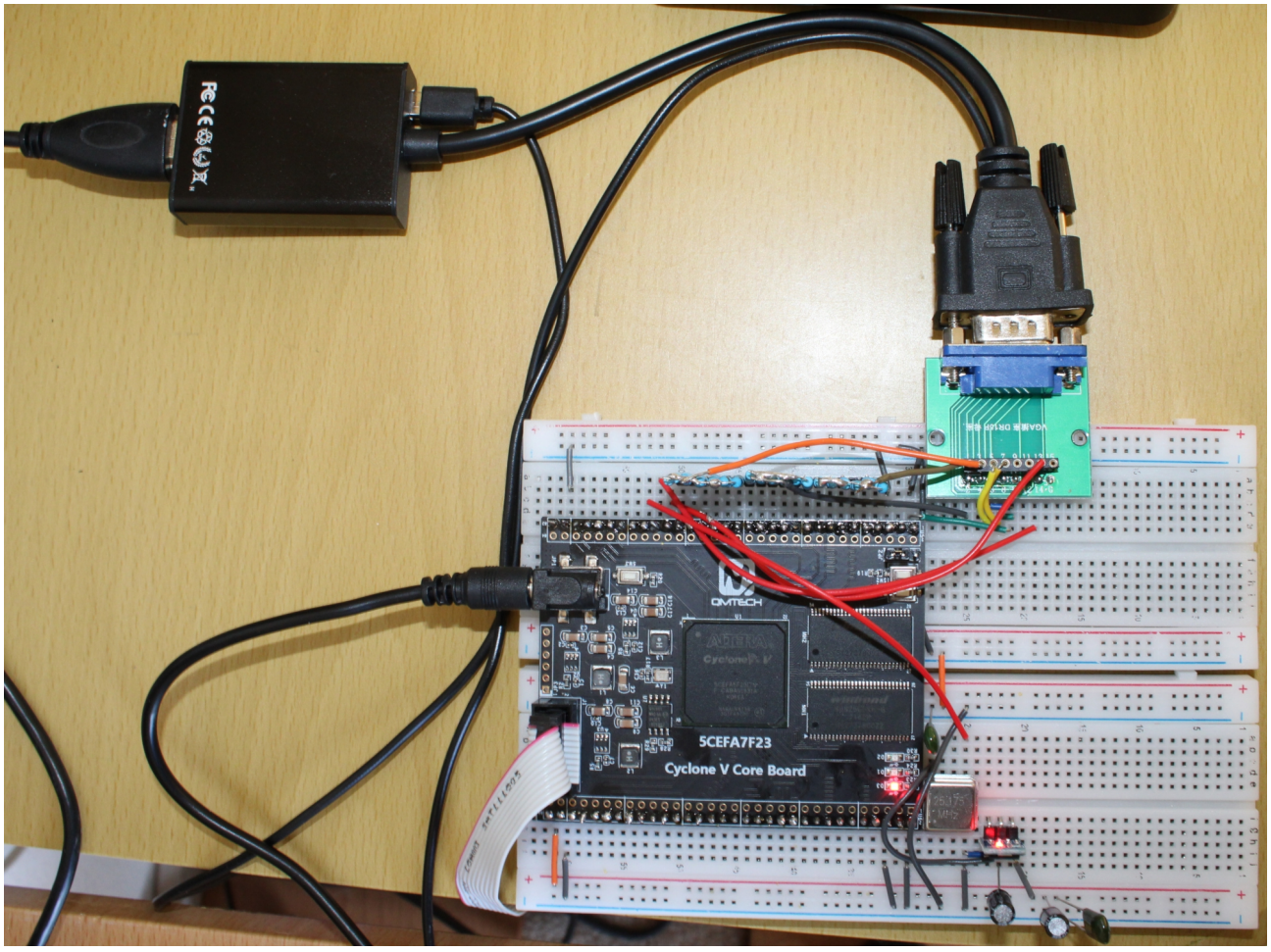
VGA Color Bars Display by FPGA



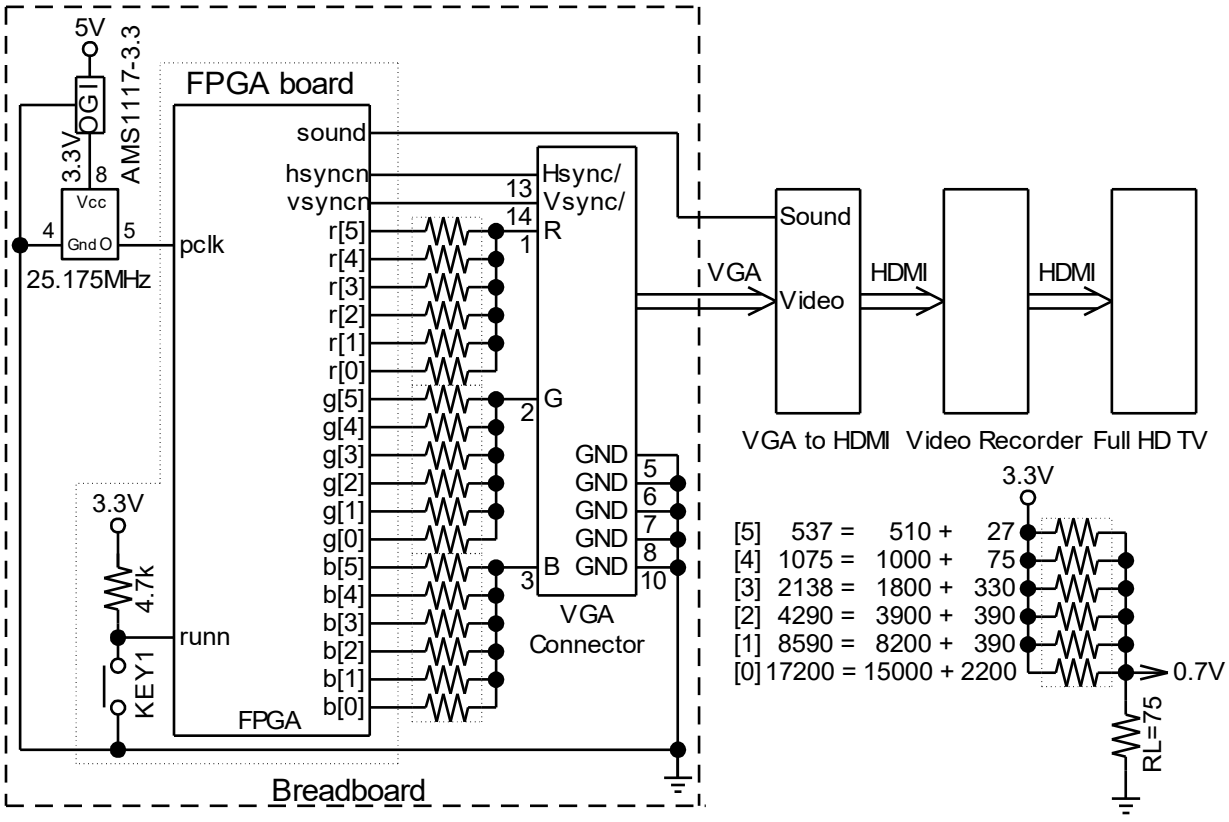
Whole aspect of system (displaying color bars Rev.1)



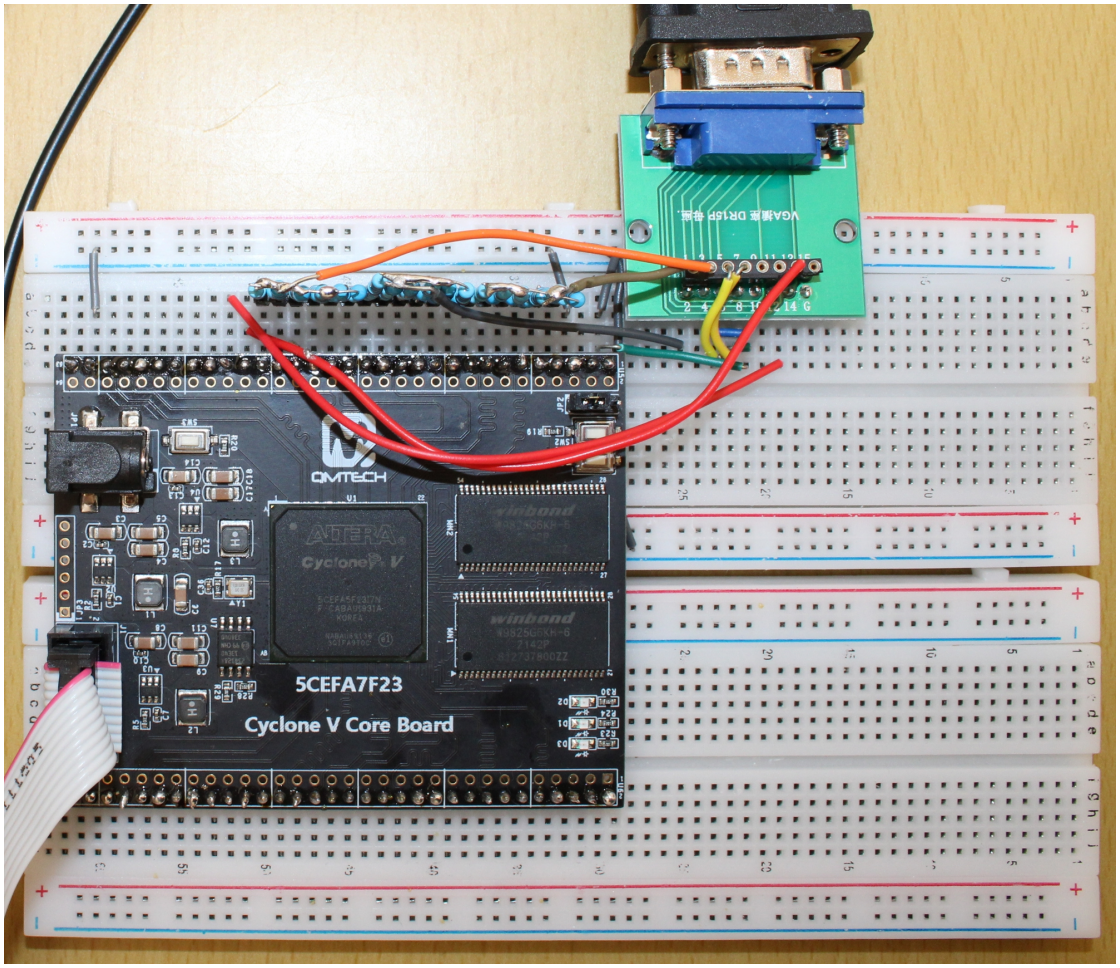
System Rev.1 (with on-board VGA RAMDAC and 25.175MHz crystal oscillator)



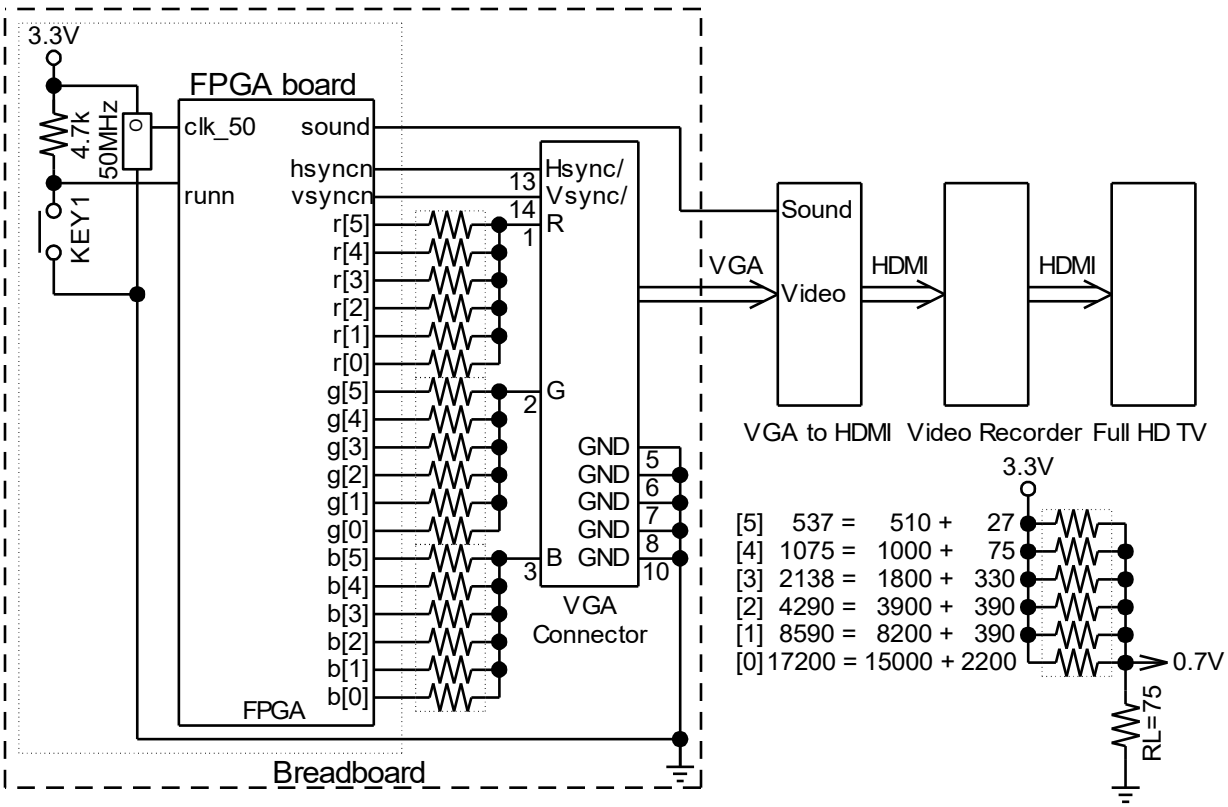
Breadboard Rev.2 (with on-board 25.175MHz crystal oscillator) & VGA to HDMI Converter



System Rev.2 (with on-board 25.175MHz crystal oscillator)



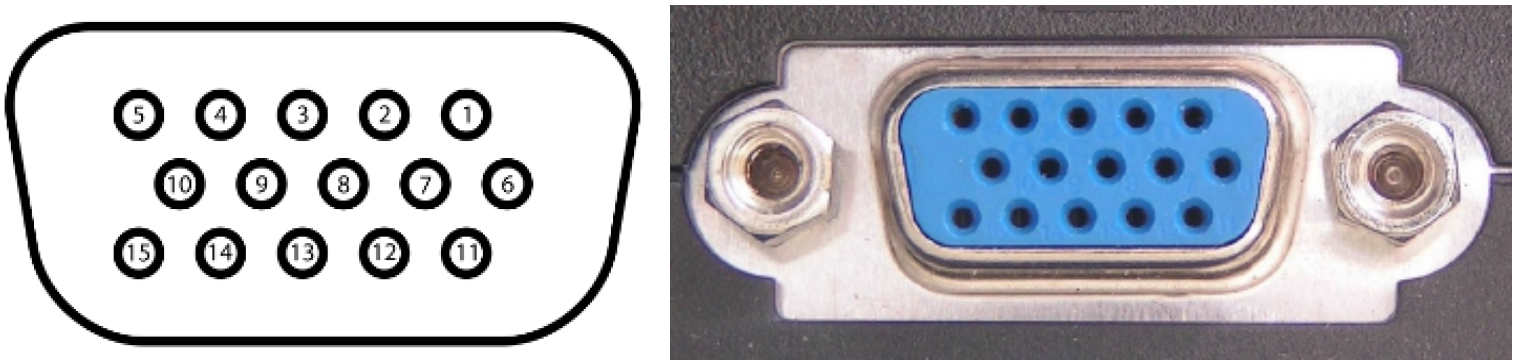
Breadboard Rev.3 (25.175MHz crystal oscillator removed)



System Rev.3 (25.175MHz crystal oscillator removed)

	Functions integrated in FPGA	Parts utilized on FPGA board	Parts implemented on Breadboard
Rev.1	- VGA sync generator - Color bars generator - RAMDAC controller	- Run key	- 25.175MHz crystal oscillator - RAMDAC
Rev.2	- VGA sync generator - Color bars generator - RAMDAC table memory	- Run key	- 25.175MHz crystal oscillator - Resister tree for DAC
Rev.3	- VGA sync generator - Color bars generator - RAMDAC table memory - 25.175MHz clock generator	- Run key - 50MHz crystal oscillator	- Resister tree for DAC

VGA Connector (15 pin High Density D-SUB connector)



Female connector view (Both PC and monitor device side)

Pin #	I/O	A/P/N	Description	Pin #	I/O	A/P/N	Description	Pin #	I/O	A/P/N	Description
1	O	A	Red video	**6**	--	--	Red GND	**11**	I	P	DDC ID0
2	O	A	Green video	**7**	--	--	Green GND	**12**	I	P	DDC ID1
3	O	A	Blue video	**8**	--	--	Blue GND	**13**	O	N	Horizontal Sync
4	I	P	DDC ID2	**9**	--	--	(+5V possible)	**14**	O	N	Vertical Sync
5	--	--	Hsync GND	**10**	--	--	Vsync/DDC GND	**15**	I	P	DDC ID3

A : Analog 0.7 Vpeak-to-peak when 75 ohm load impedance
P : Positive Digital 5V to GND
N : Negative Digital 5V to GND

In more details, refer to "Probing VGA_SVGA_XGA Video Signals.pdf".

Color Map (With Color Rotation)

RGB (1 bit each)	Attribute				Level (ffh - 00h)						Actual color
	Video		Chroma		Dec			Hex			
	Bright	Gray	Thick	Thin	R	G	B	R	G	B	
100	1	0	1	0	255	0	0	ff	00	00	
			0	1	255	128	0	ff	74	00	
	0	1	1	0	208	64	0	d5	41	00	
			0	1	208	192	0	d5	aa	00	
110	1	0	1	0	255	255	0	ff	ff	00	
			0	1	128	255	0	74	ff	00	
	0	1	1	0	192	208	0	aa	d5	00	
			0	1	64	208	0	41	d5	00	
010	1	0	1	0	0	255	0	00	ff	00	
			0	1	0	255	128	00	ff	74	
	0	1	1	0	0	208	64	00	d5	41	
			0	1	0	208	192	00	d5	aa	
011	1	0	1	0	0	255	255	00	ff	ff	
			0	1	0	128	255	00	74	ff	
	0	1	1	0	0	192	208	00	aa	d5	
			0	1	0	64	208	00	41	d5	
001	1	0	1	0	0	0	255	00	00	ff	
			0	1	128	0	255	74	00	ff	
	0	1	1	0	64	0	208	41	00	d5	
			0	1	192	0	208	aa	00	d5	
101	1	0	1	0	255	0	255	ff	00	ff	
			0	1	255	0	128	ff	00	74	
	0	1	1	0	208	0	192	d5	00	aa	
			0	1	208	0	64	d5	00	41	
111	1	0	1	0	255	255	255	ff	ff	ff	
			0	1	192	192	192	aa	aa	aa	
	0	1	1	0	128	128	128	74	74	74	
			0	1	64	64	64	41	41	41	
000	1	0	1	0	0	0	0	00	00	00	
			0	1	0	0	0	00	00	00	
	0	1	1	0	0	0	0	00	00	00	
			0	1	0	0	0	00	00	00	

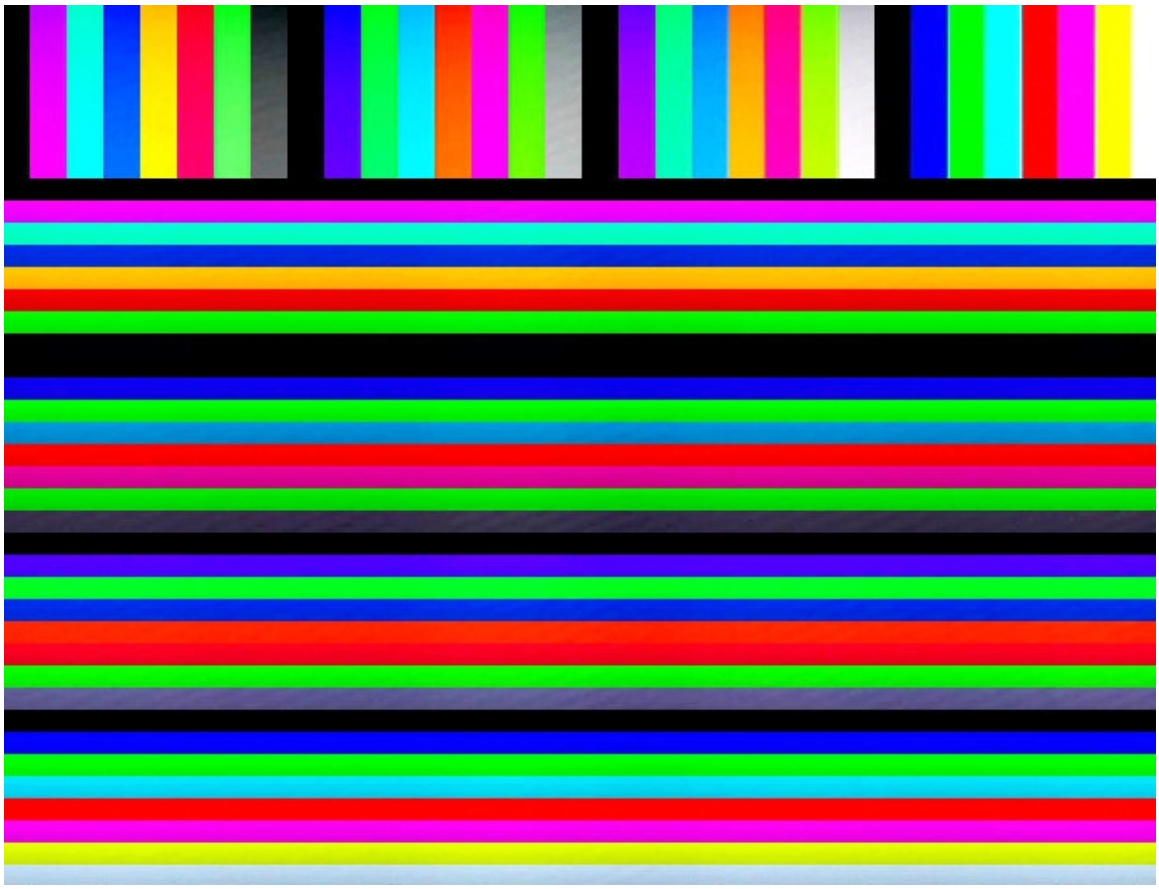
6 bit Digital to Analog Converter

5 bit color information to 6 bit RGB

Color signal level					Hex code						Color
Brightness	Hue	R	G	B	(8 bits)			(6 bits)			
P4	P3	P2	P1	P0	R	G	B	R	G	B	
0	0	0	0	0	00	00	00	00	00	00	
0	0	0	0	1	aa	00	d5	2a	00	35	
0	0	0	1	0	00	d5	aa	00	35	2a	
0	0	0	1	1	00	41	d5	00	10	35	
0	0	1	0	0	d5	aa	00	35	2a	00	
0	0	1	0	1	d5	00	41	35	00	10	
0	0	1	1	0	41	d5	00	10	35	00	
0	0	1	1	1	41	41	41	10	10	10	
0	1	0	0	0	00	00	00	00	00	00	
0	1	0	0	1	41	00	d5	10	00	35	
0	1	0	1	0	00	d5	41	00	35	10	
0	1	0	1	1	00	aa	d5	00	2a	35	
0	1	1	0	0	d5	41	00	35	10	00	
0	1	1	0	1	d5	00	aa	35	00	2a	
0	1	1	1	0	41	d5	00	10	35	00	
0	1	1	1	1	74	74	74	1d	1d	1d	
1	0	0	0	0	00	00	00	00	00	00	
1	0	0	0	1	74	00	ff	1d	00	3f	
1	0	0	1	0	00	ff	74	00	3f	1d	
1	0	0	1	1	00	74	ff	00	1d	3f	
1	0	1	0	0	ff	74	00	3f	1d	00	
1	0	1	0	1	ff	00	74	3f	00	1d	
1	0	1	1	0	74	ff	00	1d	3f	00	
1	0	1	1	1	aa	aa	aa	2a	2a	2a	
1	1	0	0	0	00	00	00	00	00	00	
1	1	0	0	1	00	00	ff	00	00	3f	
1	1	0	1	0	00	ff	00	00	3f	00	
1	1	0	1	1	00	ff	ff	00	3f	3f	
1	1	1	0	0	ff	00	00	3f	00	00	
1	1	1	0	1	ff	00	ff	3f	00	3f	
1	1	1	1	0	ff	ff	00	3f	3f	00	
1	1	1	1	1	ff	ff	ff	3f	3f	3f	

Color Bars Displayed on 640x480 VGA Screen

Color bars Rev.1 (Vertical bars only)



Color bars Rev.2 (Vertical and Horizontal bars)

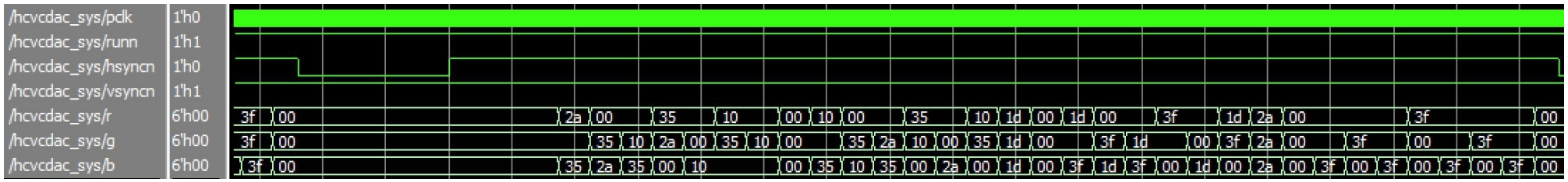
Timing design of Color bars Rev.2

P		0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh	10h	11h	12h	13h	14h	15h	16h	17h	18h	19h	1Ah	1Bh	1Ch	1Dh	1Eh	1Fh
	H\Clk	20	40	60	80	100	120	140	160	180	200	220	240	260	280	300	320	340	360	380	400	420	440	460	480	500	520	540	560	580	600	620	640
	1																																

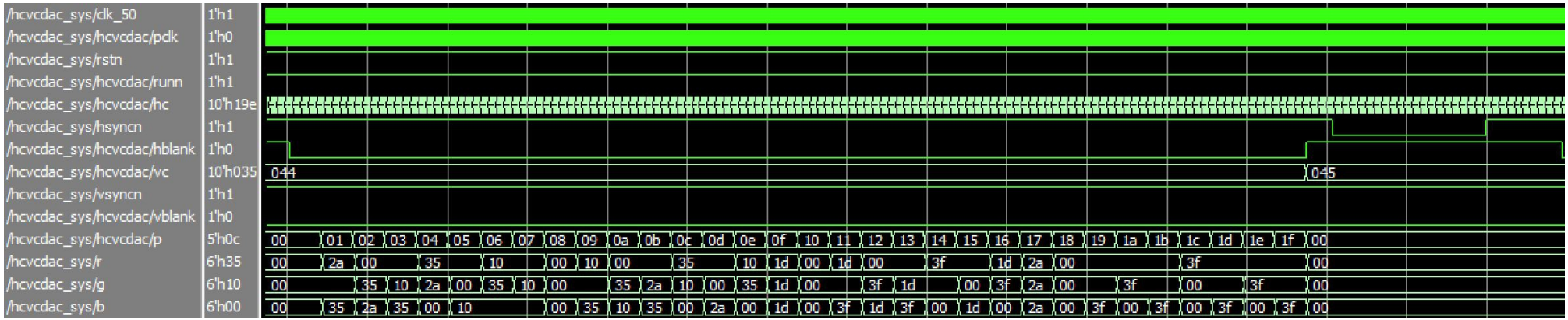
0h	96
1h	108
2h	120
3h	132
4h	144
5h	156
6h	168
7h	180
8h	192
9h	204
Ah	216
Bh	228
Ch	240
Dh	252
Eh	264
Fh	276
10h	288
11h	300
12h	312
13h	324
14h	336
15h	348
16h	360
17h	372
18h	384
19h	396
1Ah	408
1Bh	420
1Ch	432
1Dh	444
1Eh	456
1Fh	468

Verilog HDL Simulation Results

(A) Color Bars Rev.2

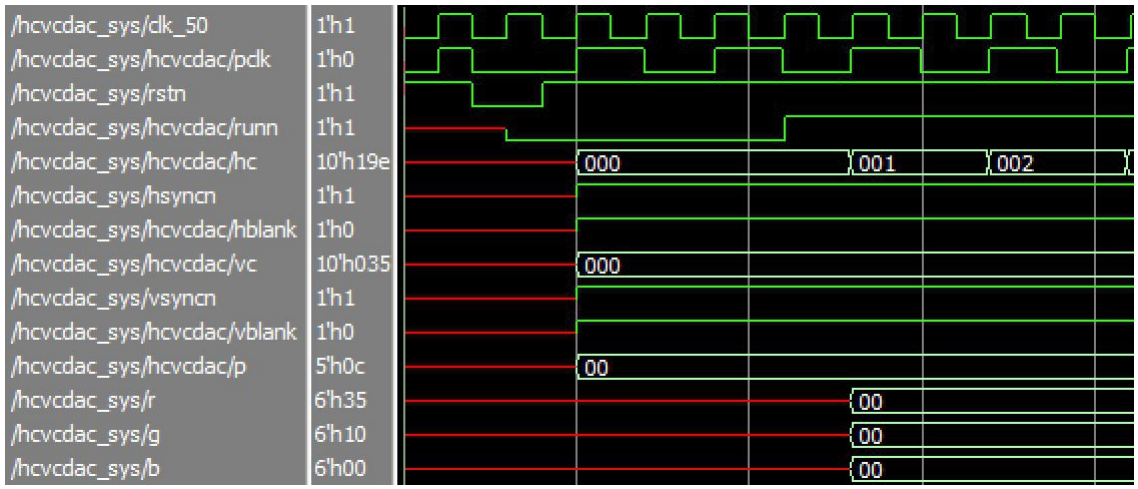


Vertical color bars (Total 32 vertical color bars changing color every 20 pclks at upper 96 lines)



Horizontal color bars (Total 32 horizontal color bars changing color every 12 lines at lower 384 lines)

(B) Reset timing of 25.175MHz clock generator and Logic implemented



First, reset “pclk” clock generator PLL by “rstn”. Then, reset FPGA sequential logic by “runn” made by combinational logic until “pclk” is stabled.

C++ software source code for DAC voltage level evaluation (“da_conv.cpp”)

```
/*****************************************************************************
Program name:   Digital to Analog Conversion Analysis
Module name:    da_conv.cpp
Description:    The program calculates analog RGB voltage level output through
                resistor trees.
                Output files :
                 "da_conv.log" RGB voltage calculation result text file
Usage:          da_conv <enter>
Version:        1.0
Date:           March 18, 2024
Programmer:     Tetsuji Oguchi
(C) Oguchi R&D  2024
*****************************************************************************/

#include   <stdio.h>
#include   <string.h>
#include   <process.h>

static char    outfile[] = "da_conv.log";
static int     rgb;
static double  r5, r4, r3, r2, r1, r0;  /* Resistor tree */
static double  rhigh, rlow, rload, vout;

FILE *logfp;

int main()
{
    printf("6 bit digital to analog VGA color conversion signal level calculation program\n");
    printf("                              (C) Oguchi R&D  2024\n\n");

    // Check & specify file I/O
    if (fopen_s(&logfp, outfile, "w"))
    {
      printf("Output file %s open error...\n", outfile);
      exit(0);
    }

    // Start calculation for DA converter
    r5    = 1/0.537;     /*  0.510 + 0.027 (0.537)    */
    r4    = 1/1.075;     /*  1.000 + 0.075 (1.074)    */
    r3    = 1/2.138;     /*  1.800 + 0.330 (2.148)    */
    r2    = 1/4.29;      /*  3.900 + 0.390 (4.296)    */
    r1    = 1/8.59;      /*  8.200 + 0.390 (8.592)    */
    r0    = 1/17.2;      /* 15.000 + 2.200 (17.184)   */
    rload = 1/0.075;     /* Load resistance = 75 ohms */
    for (rgb = 0x3f; rgb > -1; rgb--)
    {
      fprintf(logfp, "%02x  ", rgb);
      rhigh = 0;
      rlow  = 0;
      if (rgb & 0x20)  rhigh  = r5;
        else  rlow = r5;
      if (rgb & 0x10)  rhigh += r4;
        else  rlow += r4;
      if (rgb & 0x08)  rhigh += r3;
        else  rlow += r3;
      if (rgb & 0x04)  rhigh += r2;
        else  rlow += r2;
      if (rgb & 0x02)  rhigh += r1;
        else  rlow += r1;
```

```
      if (rgb & 0x01)  rhigh += r0;
        else  rlow += r0;
      rhigh = 1/rhigh;
      rlow  = 1/(rlow + rload);
      vout  = 3.3 * (rlow / (rhigh + rlow));
      fprintf(logfp, "%03f\n", vout);
    }

    // End calculation
    printf("Digtal Analog Converter resistor tree calculation completed\n");

    fclose(logfp);
}
```

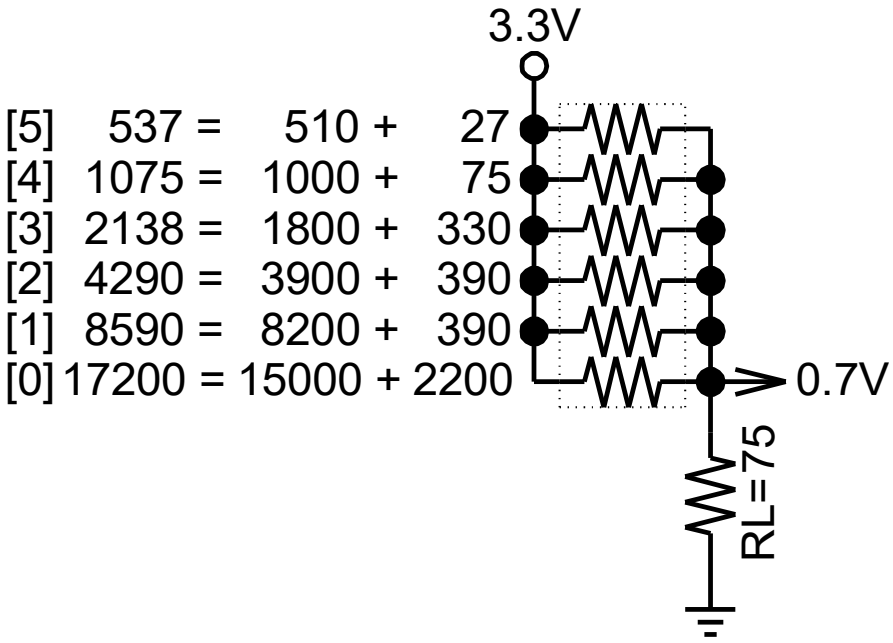
Log file (“da_conv.log”) result

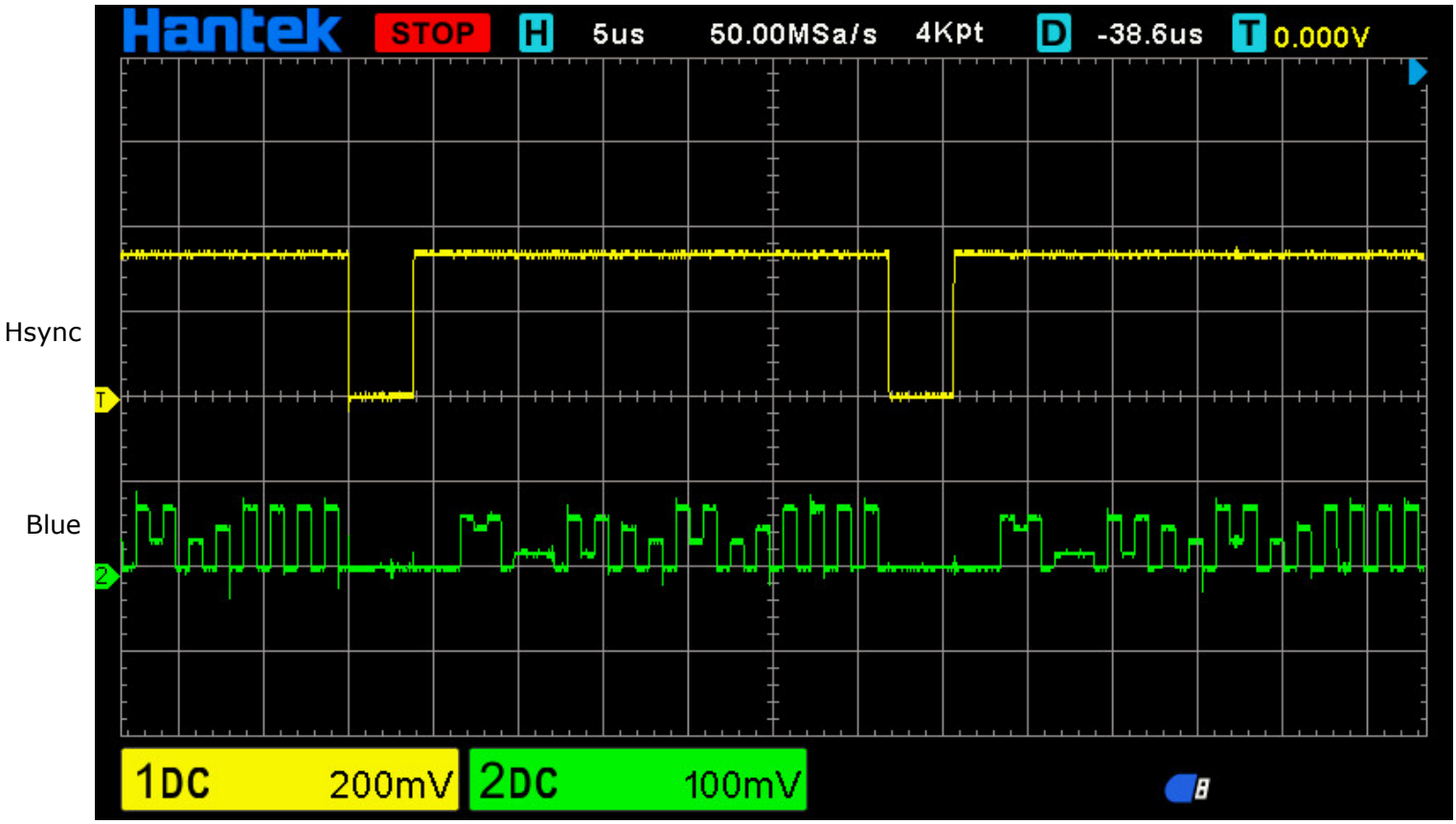
When 6 bit RGB level fully swings (3fh), 0.7V analog output appears between 75 ohm load resistor and ground.

6 bit R, G, B	Analog output (V)	6 bit R, G, B	Analog output (V)
3fh	0.711939	1fh	0.350478
3eh	0.700654	1eh	0.339193
3dh	0.689342	1dh	0.327881
3ch	0.678057	1ch	0.316596
3bh	0.666693	1bh	0.305232
3ah	0.655408	1ah	0.293947
39h	0.644097	19h	0.282635
38h	0.632811	18h	0.271350
37h	0.621151	17h	0.259690
36h	0.609866	16h	0.248405
35h	0.598554	15h	0.237093
34h	0.587269	14h	0.225808
33h	0.575905	13h	0.214444
32h	0.564620	12h	0.203159
31h	0.553309	11h	0.191848
30h	0.542023	10h	0.180562
2fh	0.531377	0fh	0.169915
2eh	0.520091	0eh	0.158630
2dh	0.508780	0dh	0.147319
2ch	0.497495	0ch	0.136034
2bh	0.486131	0bh	0.124670
2ah	0.474846	0ah	0.113384
29h	0.463534	09h	0.102073
28h	0.452249	08h	0.090788
27h	0.440589	07h	0.079128
26h	0.429303	06h	0.067842
25h	0.417992	05h	0.056531
24h	0.406707	04h	0.045246
23h	0.395343	03h	0.033882
22h	0.384058	02h	0.022597
21h	0.372746	01h	0.011285
20h	0.361461	00h	0.000000

Based upon this table, I calculated and made a VGA DAC register tree shown at next page.

VGA DAC Resistor Tree





Hsync vs. Digital to Analog Converter output (Blue) (maximum 0.7V peak-to-peak)