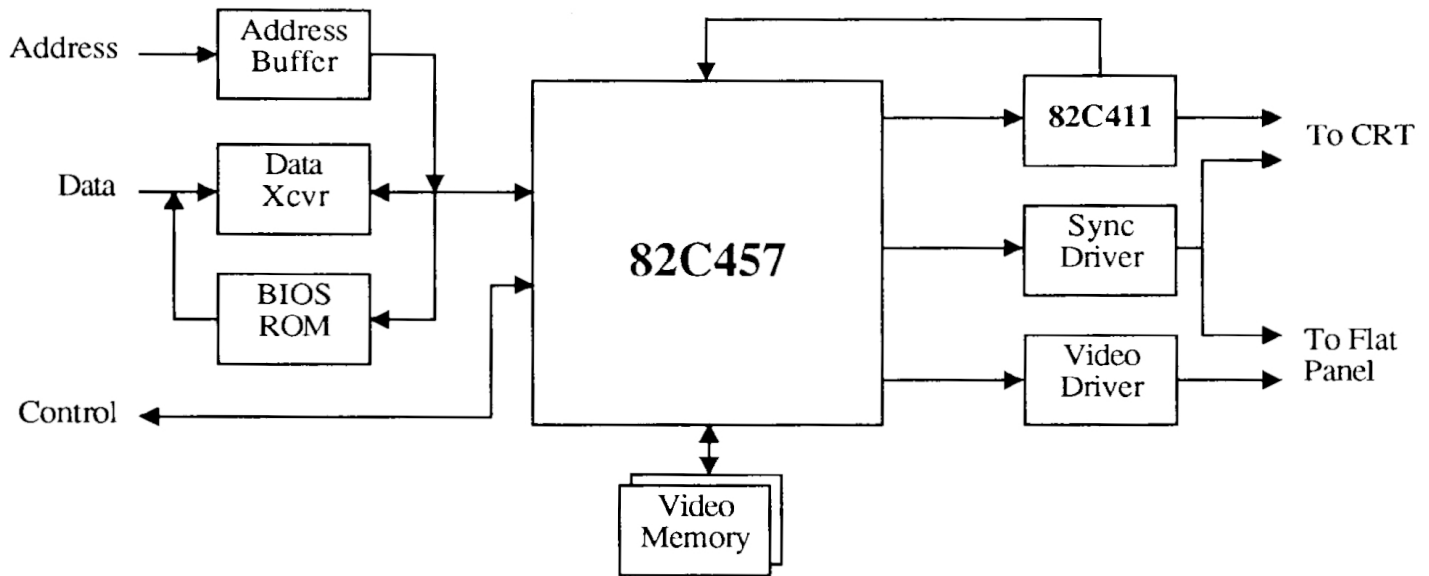


# 82C457 Enhanced Color Flat Panel/CRT VGA Controller

- Fully IBM VGA-compatible
- Supports TFT and STN Color LCD panels of varying resolutions and analog/digital CRT monitors
- Up to 227K colors on Color Flat Panels
- Integrates full support of STN, TFT and Plasma color panels
- Programmable vertical compensation techniques increase usable display area
- Advanced SLEEP mode minimizes power consumption
- Full backwards compatibility with IBM EGA, CGA, MDA and Hercules graphics standards
- Proven DOS and OS/2™ compatibility



82C457 System Block Diagram

# Introduction

The 82C457 Enhanced Color Flat Panel/CRT VGA Controller, combined with the 82C411 Flat Panel Color Palette / DAC, provides a complete solution for a VGA, EGA, CGA, MDA, or Hercules compatible display system. The 82C457 supports a wide variety of color flat panel displays and CRT monitors.

By providing a high level of integration, the 82C457 minimizes the total chip count for a VGA display subsystem. The 82C457 power-down features reduce power consumption of the display subsystem and extend battery life in portable applications. The 82C457 provides a variety of programmable features, such as Vertical Compensation and Alternate Registers to enhance the flat panel display; as well as Frame Rate Control to increase the number of displayable colors.

## FLAT PANEL DISPLAYS

There is currently no standard interface for flat panel displays. Interface signals and timing requirements vary between panel technologies and manufacturers. The 82C457 provides register programmable features to allow interfacing to the widest possible range of flat panel display units. The 82C457 is optimized to interface directly to color panels. For most panel applications, no additional interface circuitry is required.

The 82C411 Flat Panel Color Palette / DAC and a proprietary Frame Rate Control (FRC) algorithm in the 82C457's hardware generate up to 64 shades for each color (RGB) output. The FRC algorithm simulates intensity levels on panels by turning the pixels on and off over several frames. This technique allows up to 226,981 color to be displayed on color STN LCD panels. For flat panels that support multiple levels per color (more than one bit per color per pixel), the 82C457 supports up to 4096 colors directly. By combining internally generated colors with FRC up to 4096 colors may be supported on TFT panels. For an analog CRT display, the 82C411 provides all the functions of a standard RAMDAC and LM339 comparator.

The 82C457 supports all color liquid crystal display (LCD) technologies, including thin film transistor (TFT). Interfaces are provided for single panel-single drive (SS) and dual panel-single drive (DS) configurations. A single panel sequences data similar to a CRT. In contrast, a dual panel requires

video data from separate locations in memory. The 82C457 handles the display data sequencing transparent to the application software, providing full compatibility on both CRT and flat panel displays.

The 82C457 can support the popular panel resolutions of 640x200, 640x350, 640x400 and 640x480. For non-standard applications additional resolutions are supported. The 82C457 provides a direct interface to panels from vendors such as Sharp, Sanyo, Hitachi and Epson.

## CRT MONITOR

The 82C457 supports both fixed and variable frequency analog monitors, including IBM PS/2™ and Multisync™ or Multi-Scan monitors. The 82C457 supports digital TTL monitors for the EGA, CGA, and MDA standards with no extra circuitry if a clock synthesizer (such as the 82C401/A) is used. If a clock synthesizer is not used, a single CMOS PAL and the required oscillators must be added for digital monitor support. High resolution support is provided on both fixed and variable frequency monitors. When booting a system, the BIOS determines the monitor type and whether to boot on the CRT or flat panel.

## COMPATIBILITY

The 82C457 is fully compatible with the IBM VGA standard. The 82C457 also provides compatibility with IBM's EGA, CGA and MDA standards and the Hercules graphics adapter. The 82C457 includes a variety of features to provide compatibility on flat panel displays. Internal compensation techniques ensure that industry-standard software designed for different displays can be executed on the single flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software.

## EXTENSION REGISTERS

The 82C457 employs an "Extension" Register set to control its enhanced features. These Extension Registers provide control of the flat panel interface, flat panel timing, vertical compensation and Backwards Compatibility.

### Flat Panel Interface Registers

The Flat Panel Interface characteristics are controlled by a subset of the Extension Registers. These

Registers select the panel type, data formatting, panel configuration, panel size, clock selection and video polarity. Since the 82C457 is designed to support a wide range of panel types and sizes, control of these features is fully programmable.

### **Flat Panel Timing Registers**

Flat panel displays usually require sync signal timing that is different from a CRT. To provide full compatibility with the IBM VGA standard, alternate timing registers are used to allow independent timing of the sync signals for flat panel displays. Unlike the values programmed into the standard CRT timing registers, the value programmed into the alternate timing registers is dependent on the panel type used and is independent of the display mode.

### **VERTICAL COMPENSATION**

Vertical Compensation is a programmable feature that increases the usable display area when running lower resolution software on a higher resolution panel. Unlike CRT monitors, flat panels have a fixed number of scan lines (e.g., 200, 350, 400 or 480 lines). Lower resolution software run on a higher resolution panel only partially fills the usable display area. For instance, 350-line EGA software displayed on a 480-line panel would leave 130 blank lines at the bottom of the display. The 82C457 offers the following three Vertical Compensation techniques to increase the usable screen area:

First, border insertion (referred to as "centering") adjusts the Display Start and Display End addresses to center the display, leaving a border of unused area at the top and bottom of the panel. Border insertion can be used in text and graphics modes.

Second, line replication (referred to as "stretching") duplicates every Nth display line (where N is programmable), thus stretching text characters and graphic images an adjustable amount. The display can be stretched to completely fill the flat panel area. Double scanning, a form of line replication where every line is replicated, is useful for running 200 line software on a 400 line panel. Line replication can be used in text and graphics modes

Third, blank line insertion, inserts N blank lines (where N is programmable) between each line of text characters. Thus text can be evenly spaced to fill the entire panel display area without altering the height and shape of the text characters. Blank line insertion can be used in text mode only.

Each of these Vertical Compensation techniques can be controlled by programming the 82C457's Extension Registers. A combination of centering and stretching or blank line insertion may also be used.

### **VIDEO BIOS**

In typical applications, the 82C457 is placed on the CPU board and the video BIOS is integrated with the system BIOS. A signal (ROMCS/) is provided for implementing a separate 8-bit ROM Video BIOS. CHIPS supplies a video BIOS that is optimized for the 82C457 hardware. The BIOS supports the extended functions of the 82C457, such as switching between the flat panel and the CRT, and setting the Vertical Compensation values. The BIOS Modification Program (BMP) enables OEMs to tailor their feature set by programming the extended functions. CHIPS also provides several BMS files as part of the 82C457 utility package. Those files contain all configuration information for a variety of color panels. Working in conjunction with the BMP, the BMS files will load automatically the BIOS information. CHIPS offers the BIOS as a standard production version, a customized version or as source code.

### **POWER REDUCTION**

The 82C457 Power-Saving feature reduces power consumption and extends battery-based operation. When the PWRDN pin goes high, the 82C457 enters 'retire' power-down mode.

While in retire mode the 82C457 is invisible to the system. The display is blanked, the display timing signals are halted and the flat panel should be turned off. The CPU cannot access any internal registers or display memory. During retire mode, the 82C457 continues to refresh the DRAMs at a programmable rate, to conserve power in display memory while preventing data loss. This mode is useful when system operation is suspended.

### **BUS INTERFACE**

The 82C457 directly interfaces to 8-bit PC and PC/XT and 16-bit PC/AT buses. All operations necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations, and generation of the necessary control signals.

### **DISPLAY MEMORY**

The 82C457 supports a total of 256 Kbytes of display memory. The 82C457 serves as a DRAM controller for the system's display memory. It handles DRAM refresh, fetches data from display memory as required to refresh the screen, interfaces the CPU to display memory and supplies all necessary DRAM control signals. The display memory is arranged as four planes of 64 Kbytes

each. Each plane is eight bits wide for a total of 32 bits. Planes 0 and 1 share a common address bus, as do Planes 2 and 3. Each pair of planes has a common RAS signal. CAS and write enable are either shared or separate, depending on the memory device chosen. Supported DRAMs include two 64Kx16 (with either separate CAS or write enable signals), four 64Kx8 or eight 64Kx4. 120ns DRAMs are required for clock inputs up to 30 MHz. Pseudo-Static and SRAMs can be supported with external address latches.

## **82C457 ARCHITECTURE**

The 82C457 integrates four major internal modules:

### **Graphics Controller**

The Graphics Controller interfaces the 8 or 16-bit CPU data bus to the 32-bit data bus used by the four planes (Maps) of display memory. It also latches and supplies display memory data to the Attribute Controller for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller also performs any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

### **Sequencer**

The Sequencer generates all CPU and display memory timing signals. It controls CPU access of display memory by inserting cycles dedicated to CPU access. It also contains mask registers which can prevent writes to individual display memory planes.

### **Attribute Controller**

The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and 16 color graphic modes the 4-bit pixel data acts as an index into a set of internal color look-up registers which generate a 6-bit stream. Two additional bits of color data are added to provide an 8-bit address to the external color palette. In 256 color modes, two 4-bit values are passed through the color look-up registers and assembled into an 8-bit value. Text and cursor blink, underline and horizontal scrolling are also the responsibility of the Attribute Controller.

### **CRT Controller**

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

### **82C411**

The 82C411 is used to provide the required color information to the 82C457 as well as the functions of an industry standard RAMDAC in a single package. It stores all 18-bits of color video data (i.e., 6-bit Red, 6-bit Green and 6-bit Blue data) in internal RAM. During display, the data is provided to triple 6-bit DACs for display on the CRT or to digital outputs for conversion to flat panel output.

## MODES OF OPERATION

The 82C457 addresses the specific requirements of laptop design by providing different modes of operation to optimize power usage. The table at the bottom of the page summarizes these modes and display memory access in each.

### Reset mode

When this mode is activated by pulling the RESET pin high, the 82C457 is forced to VGA-compatible mode and the CRT is selected as the active display. In addition, the 82C457 is disabled; it must be enabled after deactivating the RESET pin by writing to the Global Enable Register (102h in Setup Mode). Access to all Extension Registers is also disabled. They must be explicitly enabled via the Extension Enable Register (103h in Setup Mode) following a reset. The RESET pin must be active for at least 64 clock cycles.

### Setup Mode

In this mode, only the configuration registers are accessible (these include the Global Enable, Extension Enable and Global ID).

Setup mode is entered by writing a 1 to bit-4 of port 46E8h. This port is incorporated in the 82C457. While in Setup mode, the video output is active if it was active prior to entering Setup mode and inactive if it was inactive prior to entering Setup mode.

### Normal Operating Mode

In this mode all functions of the 82C457 are enabled except that the configuration registers (102h and 103h) are not accessible.

### Retire Mode

The 82C457 supports a power-down mode to reduce power consumption and extend battery-based operation. While the 82C457 is in retire mode, the display is blanked, the display timing signals are halted and the flat panel should be turned off. The CPU cannot access any internal registers or display memory. During Retire, the 82C457 continues to refresh the DRAMs at a programmable rate to conserve power in the display memory while preventing data loss. Extension register 5Fh (XR5F) defines the frequency of the memory refresh cycles during the retire mode. The lower the refresh frequency is, the greater the power savings. The 82C457 provides for very low refresh frequencies, thereby extending battery life.

Mode of Operation	RESET Pin	PWRDN Pin	Display Memory Access	Video Output
Reset	High	xxx	----	----
Setup	----	----	No	Yes
Normal	Low	Low	Yes	Yes
Retire	Low	High	No	No

**Note:** Combinations of pin levels not shown in the table above are illegal and should not be used.

## GENERAL PURPOSE OUTPUTS

The 82C457 provides two general purpose output pins. This feature relies on redefinition of the TRAP/ and ERMEN/ pins with the General Purpose Output Registers (XR08 and XR09). These pins can be defined to serve their normal function or can be individually 3-stated, forced low, or forced high. In most applications, the TRAP/ pin is used as a CRT / LCD control signal.

## SCREEN BLANKING

The 82C457 permits blanking of the display by writing to bit 5 of the Sequencer Clocking Mode Register (SR01). With the screen blanked, all memory cycles are available to the CPU except those used for display memory refresh. In addition, the video output can be forced to a predefined color (the default video) whenever the BLANK/ pin is asserted. This color is written to the Default Video Register (XR2B).

## INTERNAL AND EXTERNAL PALETTES

The 82C457 contains 16 color look-up registers (in the Attribute Controller), each of which is 6 bits wide. These are used in 16 color modes to select 16 active colors from a palette of 64.

The 82C457 also supports an external flat panel color palette / DAC (such as the Chips 82C411). CPU access to this device is controlled by the 82C457, which decodes CPU accesses and generates the PALRD/ and PALWR/ signals for the external palette. I/O addresses 3C6-3C9h are valid external palette addresses.

## LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter are saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space at indices 10h and 11h. This allows simulation of a light pen hit in CGA and Hercules modes.

## SYSTEM TRAPS

The 82C457 supports generation of traps (NMIs) on one or more conditions. The Trap Enable and Trap Status Registers (XR16 and XR17) are utilized to implement this feature. Note that the use of traps with OS/2™ and other operating environments may not be useful.

## FRAME INTERRUPTS

The 82C457 supports frame interrupts. For compatibility with the IBM VGA adapter in the PC bus, frame interrupts may also be disabled through the Emulation Mode register (XR14).

## DIP SWITCH INPUTS

The 82C457 supports up to 7 DIP switch inputs. These can be read through the Dip Switch Register (XR01). To implement this feature, the A16, A17, A18, BHE/, ADDHI, MIO/ (AEN) and VGAENAB (RFSH/) pins are connected to the 7 DIP switches through a multiplexer. These inputs can be used to define initialization conditions. Note: the standard CHIPS BIOS does not require that any DIP switches be connected to these inputs.

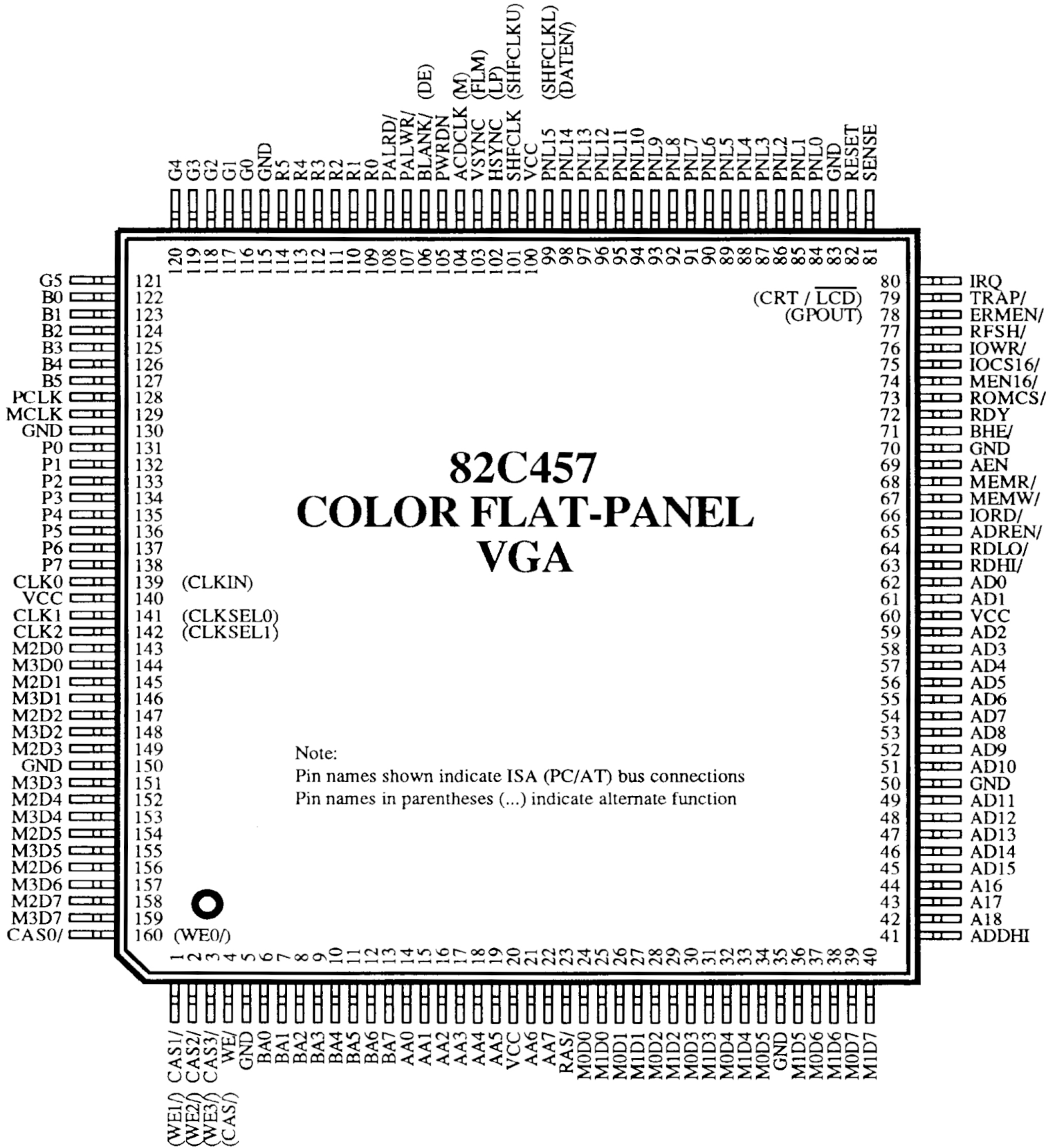
## CONTEXT SWITCHING

For support of multi-tasking, windowing and context switching, the entire state of the 82C457 (all internal registers) is readable and writeable. This feature is fully compatible with IBM's VGA. Additional registers are provided to allow read back of internal latches not readable in the IBM VGA.

## WRITE PROTECTION

A Feature of the 82C457 is the ability to write protect most of the standard VGA registers. This feature is used to provide backwards compatibility with software written for older generation display types. The write protection is grouped into register sets and controlled by the Write Protect Register (XR15).

# 82C457 Pin Diagram



## 82C457 Pin List

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
A16	44	ERMEN/ (GPOUT)	78	MEMW/	67
A17	43	G0	116	MEN16/	74
A18	42	G1	117	P0	131
AA0	14	G2	118	P1	132
AA1	15	G3	119	P2	133
AA2	16	G4	120	P3	134
AA3	17	G5	121	P4	135
AA4	18	GND	5	P5	136
AA5	19	GND	35	P6	137
AA6	21	GND	50	P7	138
AA7	22	GND	70	PALRD/	108
ACDCLK (M)	104	GND	83	PALWR/	107
AD0	62	GND	115	PCLK	128
AD1	61	GND	130	PNL0	84
AD2	59	GND	150	PNL1	85
AD3	58	HSYNC (LP)	102	PNL2	86
AD4	57	IOCS16/	75	PNL3	87
AD5	56	IORD/	66	PNL4	88
AD6	55	IOWR/	76	PNL5	89
AD7	54	IRQ	80	PNL6	90
AD8	53	M0D0	24	PNL7	91
AD9	52	M0D1	26	PNL8	92
AD10	51	M0D2	28	PNL9	93
AD11	49	M0D3	30	PNL10	94
AD12	48	M0D4	32	PNL11	95
AD13	47	M0D5	34	PNL12	96
AD14	46	M0D6	37	PNL13	97
AD15	45	M0D7	39	PNL14 (DATEN/)	98
ADDHI	41	M1D0	25	PNL15 (SHFCLKL)	99
ADREN/	65	M1D1	27	PWRDN	105
AEN	69	M1D2	29	R0	109
B0	122	M1D3	31	R1	110
B1	123	M1D4	33	R2	111
B2	124	M1D5	36	R3	112
B3	125	M1D6	38	R4	113
B4	126	M1D7	40	R5	114
B5	127	M2D0	143	RAS/	23
BA0	6	M2D1	145	RDHI/	63
BA1	7	M2D2	147	RDLO/	64
BA2	8	M2D3	149	RDY	72
BA3	9	M2D4	152	RESET	82
BA4	10	M2D5	154	RFSH/	77
BA5	11	M2D6	156	ROMCS/	73
BA6	12	M2D7	158	SENSE	81
BA7	13	M3D0	144	SHFCLK (SHFCLKU)	101
BHE/	71	M3D1	146	TRAP/ (CRT / LCD)	79
BLANK/ (DE)	106	M3D2	148	VCC	20
CAS0/ (WE0/)	160	M3D3	151	VCC	60
CAS1/ (WE1/)	1	M3D4	153	VCC	100
CAS2/ (WE2/)	2	M3D5	155	VCC	140
CAS3/ (WE3/)	3	M3D6	157	VSYNC (FLM)	103
CLK0 (CLKIN)	139	M3D7	159	WE/ (CAS/)	4
CLK1 (CLKSEL0)	141	MCLK	129		
CLK2 (CLKSEL1)	142	MEMR/	68		



Pin #	Pin Name	Type	Active	Description
69	AEN	In	High	ADDRESS ENABLE and AUXILIARY DATA BIT-5. When low, it indicates a valid I/O address. The AEN signal is latched internally. This pin also serves as an auxiliary data bit input. It is read into bit-5 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.
67	MEMW/	In	Low	MEMORY WRITE. This input must be low for CPU writes to display memory.
68	MEMR/	In	Low	MEMORY READ. This input must be low to permit the CPU to read display memory.
76	IOWR/	In	Low	I/O WRITE. This input must be low to permit the CPU to write to an 82C457 I/O register.
66	IORD/	In	Low	I/O READ. This input must be low to permit the CPU to read an I/O register.
77	RFSH/	In	Low	REFRESH and AUXILIARY DATA BIT-6. RFSH/high indicates a valid memory cycle. This pin also serves as an auxiliary data bit input which is read into bit 6 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.
75	IOCS16/	Out	Low	I/O SELECT 16. This active low signal indicates a valid 16 bit I/O cycle. IOCS16/ is driven when the VGA is accessed and 3-stated when the VGA is inactive.
72	RDY	Out	High	VGA READY. When low, this output indicates that the current CPU read/write cycle must be extended with wait states. RDY is driven when the VGA is accessed; it is 3-stated when the VGA is inactive.
74	MEN16/	Out	Low	MEMORY ENABLE 16. This active low signal indicates 16-bit memory cycle transfers are enabled. This signal should be used by external logic to enable decode of high order addresses and generation of MEMCS16/ for the PC-AT bus.
73	ROMCS/	Out	Low	ROM CHIP Select. This active low signal indicates a valid memory read in the range C0000h-C7FFFh. It is used to generate the enable for 8-bit BIOS ROMs.
71	BHE/	In	Low	BYTE HIGH ENABLE and AUXILIARY DATA BIT 3. BHE/ low indicates that the high order byte at the current word address is being accessed. If active, BHE/ must be valid when ADREN/ is low. This pin is also an auxiliary data input which is read into bit 3 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This data bit is latched internally on the falling edge of IORD/.

Pin #	Pin Name	Type	Active	Description												
80	IRQ	Out	High	VGA INTERRUPT. An interrupt can be generated whenever the vertical sync signal goes active. This pin may be logically disconnected (3-stated) through the Emulation Mode register (XR14 Bit-7) independent of whether interrupts are enabled or disabled. Clearing XR14 Bit-7 emulates the function of the IBM PC-Bus VGA board interrupt output.  <table border="1"> <thead> <tr> <th>Interrupt State</th> <th>XR14 Bit-7=0</th> <th>XR14 Bit-7=1</th> </tr> </thead> <tbody> <tr> <td>Disabled</td> <td>3-state</td> <td>3-state</td> </tr> <tr> <td>Enabled &amp; Inactive</td> <td>3-state</td> <td>Low</td> </tr> <tr> <td>Enabled &amp; Active</td> <td>3-state</td> <td>High</td> </tr> </tbody> </table>	Interrupt State	XR14 Bit-7=0	XR14 Bit-7=1	Disabled	3-state	3-state	Enabled & Inactive	3-state	Low	Enabled & Active	3-state	High
Interrupt State	XR14 Bit-7=0	XR14 Bit-7=1														
Disabled	3-state	3-state														
Enabled & Inactive	3-state	Low														
Enabled & Active	3-state	High														
82	RESET	In	High	RESET. An active high input which resets the 82C457.												
105	PWRDN	In	High	POWER DOWN. The Power Down input pin selects the Retire mode of operation when high												
139 141 142	CLK0 CLK1 CLK2	(CLKIN) (CLKSEL0) (CLKSEL1)	In In In	Both Both Both	CLK0, CLK1, and CLK2 are 3 clock inputs. One of the three is selected as the dot-clock. Alternately, CLK1/CLKSEL0 and CLK2/CLKSEL1 can be made outputs and CLK0 becomes the clock input. CLKSEL0 and CLKSEL1 can be used to select one of four clocks via an external mux for input to the chip on CLKIN.											
129	MCLK	In	Both	Memory Clock. Used to generate internal and I/O cycle timing. Contrary to its name, it is <b>not</b> used to generate any memory timing.												
108	PALRD/	Out	Low	PALETTE READ. This output is active low during I/O reads from addresses in the range 3C6h or 3C8-3C9h (I/O reads from 3C7h are handled directly by the 82C457). This output is normally connected to the Read input of the 82C411 Palette / DAC.												
107	PALWR/	Out	Low	PALETTE WRITE. This output is active low during I/O writes to addresses in the range 3C6-3C9h and is normally connected to the Write input of the 82C411 Palette / DAC).												
65	ADREN/	Out	Low	ADDRESS ENABLE. The ADREN/ output controls external multiplexing of the system address/data bus. ADREN/ low selects address and ADREN/ high selects data. ADREN/ is low when MEMR/, MEMW/, IORD/, and IOWR/ are all high. ADREN/ is high when any one of MEMR/, MEMW/, IORD/ or IOWR/ is low. The inverse of this pin, DATEN/ may be made available on PNL14.												

Pin #	Pin Name	Type	Active	Description
64	RDLO/	Out	Low	READ LOW. This output controls the direction of the external data transceivers on the low order byte (Bits 0-7) of the address / data bus. It is low when data is read from the 82C457 and high when data is written to the 82C457. This pin is 3-stated during RESET.
63	RDHI/	Out	Low	READ HIGH. This output operates identically to the RDLO/ output except that it controls the direction for the high order byte (Bits 8-15) of the address/data bus. RDHI/ is low when data is read from the 82C457 and high when data is written to the 82C457. This pin is 3-stated during RESET.
62	AD0	I/O	Both	SYSTEM ADDRESS and DATA BITS 0-15. These bits are used to address display memory and the I/O mapped 82C457 internal registers. They also transfer data between the CPU bus and the 82C457 registers and display memory. Addresses must be valid when output signal ADREN/ is low and data must be held while ADREN/ is high. Addresses are latched internally.
61	AD1	I/O	Both	
59	AD2	I/O	Both	
58	AD3	I/O	Both	
57	AD4	I/O	Both	
56	AD5	I/O	Both	
55	AD6	I/O	Both	
54	AD7	I/O	Both	
53	AD8	I/O	Both	
52	AD9	I/O	Both	
51	AD10	I/O	Both	
49	AD11	I/O	Both	
48	AD12	I/O	Both	
47	AD13	I/O	Both	
46	AD14	I/O	Both	
45	AD15	I/O	Both	
44	A16	In	Both	SYSTEM ADDRESS BITS 16-18 and AUXILIARY DATA BITS 0-2. These bits transfer a high-order address when ADREN/ is low. The auxiliary data bits on pins A16, A17, and A18 are read into bits 0-2, respectively, of the DIP Switch register when that register is accessed by the CPU. The address bits are latched internally and are ignored for I/O cycles.
43	A17	In	Both	
42	A18	In	Both	
41	ADDHI	In	High	ADDRESS HI and AUXILIARY DATA BIT 4. This high order memory address enable input is generated external to the 82C457 by decoding system addresses A19-A23. As an address, it must be valid when ADREN/ is low. It is latched internally and specifies that the current memory address is valid for the 82C457. This pin is an auxiliary data bit read into bit 4 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This input pin is ignored during I/O cycles.

Pin #	Pin Name	Type	Active	Description
24	M0D0	I/O	Both	MEMORY 0 DATA. Display memory data bus for Plane 0 (Map 0).
26	M0D1	I/O	Both	
28	M0D2	I/O	Both	
30	M0D3	I/O	Both	
32	M0D4	I/O	Both	
34	M0D5	I/O	Both	
37	M0D6	I/O	Both	
39	M0D7	I/O	Both	
25	M1D0	I/O	Both	MEMORY 1 DATA. Display memory data bus for Plane 1 (Map 1).
27	M1D1	I/O	Both	
29	M1D2	I/O	Both	
31	M1D3	I/O	Both	
33	M1D4	I/O	Both	
36	M1D5	I/O	Both	
38	M1D6	I/O	Both	
40	M1D7	I/O	Both	
143	M2D0	I/O	Both	MEMORY 2 DATA. Display memory data bus for Plane 2 (Map 2).
145	M2D1	I/O	Both	
147	M2D2	I/O	Both	
149	M2D3	I/O	Both	
152	M2D4	I/O	Both	
154	M2D5	I/O	Both	
156	M2D6	I/O	Both	
158	M2D7	I/O	Both	
144	M3D0	I/O	Both	MEMORY 3 DATA. Display memory data bus for Plane 3 (Map 3).
146	M3D1	I/O	Both	
148	M3D2	I/O	Both	
151	M3D3	I/O	Both	
153	M3D4	I/O	Both	
155	M3D5	I/O	Both	
157	M3D6	I/O	Both	
159	M3D7	I/O	Both	

Pin #	Pin Name	Type	Active	Description	
14	AA0	Out	Both	ADDRESS PLANES 1,0. Display memory address bus for DRAM planes 0 and 1.	
15	AA1	Out	Both		
16	AA2	Out	Both		
17	AA3	Out	Both		
18	AA4	Out	Both		
19	AA5	Out	Both		
21	AA6	Out	Both		
22	AA7	Out	Both		
6	BA0	Out	Both	ADDRESS PLANES 3,2. Display memory address bus for DRAM Planes 2 and 3.	
7	BA1	Out	Both		
8	BA2	Out	Both		
9	BA3	Out	Both		
10	BA4	Out	Both		
11	BA5	Out	Both		
12	BA6	Out	Both		
13	BA7	Out	Both		
23	RAS/	Out	Low	ROW ADDRESS STROBE. Row address strobe for all DRAM memory banks.	
160	CAS0/	(WE0/)	Out	Column address strobes for memory planes 0-3 in the 64Kx4 (64Kx8) memory configuration. Write enables for planes 0-3 in the 64Kx16 memory configuration.	
1	CAS1/	(WE1/)	Out		
2	CAS2/	(WE2/)	Out		
3	CAS3/	(WE3/)	Out		
4	WE/	(CAS/)	Out	Low	Write enable for all memory banks/planes in the 64Kx4 (64Kx8) memory configuration. Column address strobe for all memory banks/planes in the 64Kx16 memory configuration.

Pin #	Pin Name	Type	Active	Description																								
102	HSYNC (LP)	Out	Either	HORIZONTAL SYNC OUTPUT. HSYNC is active high if the horizontal polarity bit (in the MSR @ 3C2, D6) is low. It is active low if the horizontal polarity bit is high. In flat panel mode this polarity is controlled by the Alt. Misc. Reg (XR54).																								
103	VSYNC (FLM)	Out	Either	VERTICAL SYNC OUTPUT. VSYNC is active high if the vertical polarity bit (in the MSR @ 3C2, D7) is low. It is active low if the vertical polarity bit is high. In flat panel mode this polarity is controlled by the Alt. Misc. Reg (XR54).																								
106	BLANK/ (DE)	Out	Either	BLANK or DISPLAY ENABLE. BLANK/ is a programmable output for blanking the display which is normally connected to the RAMDAC. For CRTs, it can be redefined as a Display Enable signal in systems where a RAMDAC is not required. For Flat Panels, the Display Enable signal is output on this pin.																								
131	P0	Out	Both	VIDEO PIXEL DATA 0-7. Eight outputs to drive color or monochrome CRTs. These pins are connected to the inputs to the 82C411 color palette. Color values for digital CRT interface are assigned as follows:																								
132	P1	Out	Both																									
133	P2	Out	Both																									
134	P3	Out	Both																									
135	P4	Out	Both																									
136	P5	Out	Both																									
137	P6	Out	Both																									
138	P7	Out	Both																									
				<table> <tr> <td>P0</td> <td>B</td> <td>Blue</td> </tr> <tr> <td>P1</td> <td>G</td> <td>Green</td> </tr> <tr> <td>P2</td> <td>R</td> <td>Red</td> </tr> <tr> <td>P3</td> <td>BS/V</td> <td>Secondary Blue / Monochrome</td> </tr> <tr> <td>P4</td> <td>GS/I</td> <td>Secondary Green / Intensity</td> </tr> <tr> <td>P5</td> <td>RS</td> <td>Secondary Red</td> </tr> <tr> <td>P6</td> <td></td> <td>User Defined</td> </tr> <tr> <td>P7</td> <td></td> <td>User Defined</td> </tr> </table>	P0	B	Blue	P1	G	Green	P2	R	Red	P3	BS/V	Secondary Blue / Monochrome	P4	GS/I	Secondary Green / Intensity	P5	RS	Secondary Red	P6		User Defined	P7		User Defined
P0	B	Blue																										
P1	G	Green																										
P2	R	Red																										
P3	BS/V	Secondary Blue / Monochrome																										
P4	GS/I	Secondary Green / Intensity																										
P5	RS	Secondary Red																										
P6		User Defined																										
P7		User Defined																										
128	PCLK	Out	Both	PIXEL CLOCK. Output pixel clock to which CRT Video output data and Flat Panel Video input data is synchronized. This pin is 3-stated during RESET.																								
101	SHFCLK (SHFCLKU)	Out	Both	SHIFT CLOCK. Output pixel clock to which panel output data is synchronized. When a double clock is used (Extended 4-bit Packed Data), this pin outputs the upper shift clock.																								
104	ACDCLK (M)	Out	Both	LCD CLOCK. A 50% duty cycle square-wave with programmable period. Used to time the back bias switching in LCD panels.																								

Pin #	Pin Name	Type	Active	Description			
109	R0	In	Both	FLAT PANEL RED VIDEO DATA 0-5. These six pins are used to input the Red video data from the external digital color palette. The input data is synchronized to the PCLK. They are usually connected to R[5:0] on the 82C411.			
110	R1	In	Both				
111	R2	In	Both				
112	R3	In	Both				
113	R4	In	Both				
114	R5	In	Both				
116	G0	In	Both	FLAT PANEL GREEN VIDEO DATA 0-5. These six pins are used to input the green video data from the external digital color palette. The input data is synchronized to the PCLK. They are usually connected to G[5:0] on the 82C411.			
117	G1	In	Both				
118	G2	In	Both				
119	G3	In	Both				
120	G4	In	Both				
121	G5	In	Both				
122	B0	In	Both	FLAT PANEL BLUE VIDEO DATA 0-5. These six pins are used to input the blue video data from the external digital color palette. The input data is synchronized to the PCLK. They are usually connected to B[5:0] on the 82C411.			
123	B1	In	Both				
124	B2	In	Both				
125	B3	In	Both				
126	B4	In	Both				
127	B5	In	Both				
84	PNL0	Out	Both	FLAT PANEL DATA 0-15. Sixteen outputs to drive the flat panel data signals. The data output order depends on the panel type being driven. Typical outputs for clock divide of one are as follows:			
85	PNL1	Out	Both				
86	PNL2	Out	Both				
87	PNL3	Out	Both				
88	PNL4	Out	Both				
89	PNL5	Out	Both				
90	PNL6	Out	Both				
91	PNL7	Out	Both				
92	PNL8	Out	Both				
93	PNL9	Out	Both				
94	PNL10	Out	Both				
95	PNL11	Out	Both				
96	PNL12	Out	Both				
97	PNL13	Out	Both				
98	PNL14	(DATEN/)	Out		Both		
99	PNL15	(SHFCLKL)	Out		Both		
				Output	PWM	3-bit FRC	4-bit Pack
				PNL0	B0	B	Rn
				PNL1	B1	G	Gn
				PNL2	B2	R	Bn
				PNL3	B3	–	Rn+1
				PNL4	G0	–	–
				PNL5	G1	–	–
				PNL6	G2	–	–
				PNL7	G3	–	–
				PNL8	R0	–	–
				PNL9	R1	–	–
				PNL10	R2	–	–
				PNL11	R3	–	–
				PNL12	–	–	–
				PNL13	–	–	–
				PNL14	–	–	–
				PNL15	–	–	–

For Clock divide of 2 or 4, additional pixels are output on the unused output pins in the same order shown in the examples. For Extended 4-bit Packed data, PNL15 is the second shift clock, SHFCLKL. For additional output sequencing detail, see the panel interface section.

Pin #	Pin Name	Type	Active	Description
81	SENSE	In	Both	SENSE. The state of this input pin can be read at Input Status Register 0, Bit 4.
78	ERMEN/ (GPOUT)	Out	Low	EARLY MEMORY INDICATOR. This output indicates whether display memory is being accessed by the CPU or by the 82C457 to refresh the display. High indicates display access and low indicates CPU access. This pin can be redefined as a general purpose output.
79	TRAP/ (CRT / $\overline{\text{LCD}}$ )	Out	Low	TRAP. This active low output indicates a TRAP condition requiring special CPU assistance. This pin is open collector when used as a trap pin. It can be redefined as a general purpose output pin. The Chips BIOS redefines this as a CRT / $\overline{\text{LCD}}$ output. If this pin is high, the BIOS has programmed the part for CRT displays; if low, the BIOS has programmed the part for LCD displays.
20 60 100 140	VCC VCC VCC VCC	In	N/A	POWER
5 35 50 70 83 115 130 150	GND GND GND GND GND GND GND GND	In	N/A	GROUND



## 82C457 REGISTER SUMMARY - CGA, MDA, AND HERCULES MODES

<u>Register</u>	<u>Register Name</u>	<u>Bits</u>	<u>Access</u>	<u>I/O Port - MDA/Herc</u>	<u>I/O Port - CGA</u>	<u>Comment</u>
STAT	Display Status	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	-	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	-	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
MODE	CGA/MDA/Hercules Mode Control	7	RW	3B8	3D8	
COLOR	CGA Color Select	6	RW	n/a	3D9	
CONFIG	Hercules Configuration	2	W	3BF	n/a	
			R	3B6-3B7 index 14	n/a	XR14
RX, R0-11	'6845' Registers	--8	RW	3B4-3B5	3D4-3D5	
XRX, XR0-7F	Extension Registers	--8	RW	3B6-3B7	3D6-3D7	if port 103 bit-7=1

## 82C457 REGISTER SUMMARY - VGA MODE

<u>Register</u>	<u>Register Name</u>	<u>Bits</u>	<u>Access</u>	<u>I/O Port - Mono</u>	<u>I/O Port - Color</u>	<u>Reg Type</u>	<u>Comment</u>
POSIDL	POS ID LSB	8	R	100 (Setup Only)	100 (Setup Only)	Motherboard	ref only
POSIDH	POS ID MSB	8	R	101 (Setup Only)	101 (Setup Only)	Motherboard	ref only
SLEEP	Video Subsystem Sleep Control	1	RW	102 (Setup Only)	102 (Setup Only)	VGA	full decode
XENA	Extended Enable	7	RW	103 (Setup Only)	103 (Setup Only)	VGA	full decode
GLOBID	Global ID (0A5h)	8	R	104 (Setup Only)	104 (Setup Only)	VGA	full decode
MISC	Miscellaneous Output	7	W	3C2	3C2	VGA	
			R	3CC	3CC	VGA	
FC	Feature Control	3	W	3BA	3DA	VGA	
			R	3CA	3CA	VGA	
FEAT	Feature Read (Input Status -)	4	R	3C2	3C2	VGA	
STAT	Display Status (Input Status 1)	6	R	3BA	3DA	VGA	
CLPEN	Clear Light Pen Flip Flop	-	W(n/a)	3BB (ignored)	3DB (ignored)	n/a	no lpen
SLPEN	Set Light Pen Flip Flop	-	W(n/a)	3BC (ignored)	3DC (ignored)	n/a	no lpen
VSE	Video Subsystem Enable	1	RW	3C3 if MCA	3C3 if MCA	Motherboard	
46E8	Setup / Disable Control	2	W	46E8 if ISA	46E8 if ISA	VGA	
DACMASK	Color Palette Pixel Mask	8	RW	3C6, 83C6	3C6, 83C6	DAC	
DACSTATE	Color Palette State	2	R	3C7, 83C7	3C7, 83C7	VGA	
DACRX	Color Palette Read-Mode Index	8	W	3C7, 83C7	3C7, 83C7	DAC	
DACWX	Color Palette Write-Mode Index	8	RW	3C8, 83C8	3C8, 83C8	DAC	
DACDATA	Color Palette Registers --FF	3x6 or 3x8	RW	3C9, 83C9	3C9, 83C9	DAC	
SRX, SR0-7	Sequencer	--8	RW	3C4-3C5	3C4-3C5	VGA	
CRX, CR0-3F	CRT Controller	--8	RW	3B4-3B5	3D4-3D5	VGA	
GRX, GR0-8	Graphics Controller	--8	RW	3CE-3CF	3CE-3CF	VGA	
ARX, AR0-14	Attributes Controller	--8	RW	3C0-3C1	3C0-3C1	VGA	
XRX, XR0-7F	Extension Registers	--8	RW	3B6-3B7	3D6-3D7	VGA	103 bit7=1

## 82C457 REGISTER SUMMARY - INDEXED REGISTERS (VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	RW	RW	3C4
SR0	Reset	2	VGA/EGA	RW	RW	3C5
SR1	Clocking Mode	6	VGA/EGA	RW	RW	3C5
SR2	Plane Mask	4	VGA/EGA	RW	RW	3C5
SR3	Character Map Select	6	VGA/EGA	RW	RW	3C5
SR4	Memory Mode	3	VGA/EGA	RW	RW	3C5
SR7	Reset Horizontal Character Counter	-	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	RW	RW	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR7	Overflow	5	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latch	1	VGA	R	n/a	3B5 Mono, 3D5 Color
CR3x	Clear Vertical Display Enable FF	-	VGA	W	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	RW	RW	3CE
GR0	Set/Reset	4	VGA/EGA	RW	RW	3CF
GR1	Enable Set/Reset	4	VGA/EGA	RW	RW	3CF
GR2	Color Compare	4	VGA/EGA	RW	RW	3CF
GR3	Data Rotate	5	VGA/EGA	RW	RW	3CF
GR4	Read Map Select	2	VGA/EGA	RW	RW	3CF
GR5	Mode	6	VGA/EGA	RW	RW	3CF
GR6	Miscellaneous	4	VGA/EGA	RW	RW	3CF
GR7	Color Don't Care	4	VGA/EGA	RW	RW	3CF
GR8	Bit Mask	8	VGA/EGA	RW	RW	3CF
ARX	Attribute Controller Index	6	VGA/EGA	RW	RW	3C0 (3C1)
AR0-F	Internal Palette Regs --15	6	VGA/EGA	RW	RW	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	RW	RW	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	RW	RW	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	RW	RW	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	RW	RW	3C0 (3C1)
AR14	Color Select	4	VGA	RW	n/a	3C0 (3C1)

**82C457 EXTENSION REGISTER SUMMARY: 00-2F**

**Chips' 45x Product Family**

Reg	Register Name	Bits	Access	Port	Reset	450	451	452	453	455	456	457
XRX	Extension Index Register	7	R/W	3B6/3D6	- x x x x x x x	✓	✓	✓	✓	✓	✓	✓
XR00	Chip Version	8	R/O	3B7/3D7	0 1 1 0 0 0 0 0	✓	✓	✓	✓	✓	✓	
XR01	DIP Switch	7	R/O	3B7/3D7	- d d d d d d d	✓	✓	✓	✓	✓	✓	✓
XR02	CPU Interface	6	R/W	3B7/3D7	-- 0 0 0 0 0 0	✓	✓	✓	✓	✓	✓	✓
XR03	ROM Interface	1	R/W	3B7/3D7	- - - - - 0	.	✓	✓	✓	.	.	✓
XR04	Memory Mapping	4	R/W	3B7/3D7	- - - - 0 0 0 0	✓	✓	✓	.	✓	✓	✓
XR05	Sequencer Control	1	R/W	3B7/3D7	- - - - - 0 - -	.	.	✓	✓	.	.	✓
XR06	(DRAM Interface)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.
XR07	-reserved-	-	-	3B7/3D7	.	.	.	.	.	.	.	.
XR08	General Purpose Output Select B	3	R/W	3B7/3D7	- - - - - 0 0 0	.	✓	✓	.	✓	✓	✓
XR09	General Purpose Output Select A	2	R/W	3B7/3D7	- - - - - 0 0	.	✓	✓	.	✓	✓	✓
XR0A	(Cursor Address Top)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.
XR0B	CPU Paging	3	R/W	3B7/3D7	- - - - - 0 0 0	✓	.	✓	✓	✓	✓	✓
XR0C	(Start Address Top)	-	-	3B7/3D7	✓	.	✓	✓	.	.	.	.
XR0D	Auxiliary Offset	2	R/W	3B7/3D7	- - - - - 0 0	✓	✓	✓	✓	✓	✓	✓
XR0E	(Text Mode)	-	-	3B7/3D7	✓	.	✓	.	.	.	.	.
XR0F	-reserved-	-	-	3B7/3D7	.	.	.	.	.	.	.	.
XR10	(Single/Low Map Register)	-	-	3B7/3D7	✓	.	✓	✓	.	.	.	.
XR11	(High Map Register)	-	-	3B7/3D7	✓	.	✓	✓	.	.	.	.
XR12	-reserved-	-	-	3B7/3D7	.	.	.	.	.	.	.	.
XR13	-reserved-	-	-	3B7/3D7	.	.	.	.	.	.	.	.
XR14	Emulation Mode	8	R/W	3B7/3D7	0 0 0 0 h h 0 0	✓	✓	✓	✓	✓	✓	✓
XR15	Write Protect	7	R/W	3B7/3D7	- 0 0 0 0 0 0 0	✓	✓	✓	✓	✓	✓	
XR16	Trap Enable	6	R/W	3B7/3D7	- - 0 0 0 0 0 0	.	✓	✓	✓	✓	✓	✓
XR17	Trap Status	6	R/W	3B7/3D7	- - 0 0 0 0 0 0	.	✓	✓	✓	✓	✓	✓
XR18	Alternate H Display End	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓
XR19	Alt H Retr Start/Half-line Comp	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓
XR1A	Alternate H Retrace End	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓
XR1B	Alternate H Total	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓
XR1C	Alternate H Blank Start	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓
XR1D	Alternate H Blank End	8	R/W	3B7/3D7	0 x x x x x x x	✓	✓	✓	✓	✓	✓	✓
XR1E	Alternate Offset	8	R/W	3B7/3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓
XR1F	(Virtual EGA Switch Register)	-	-	3B7/3D7	✓	.	.	✓	.	.	.	.
XR20	(Sliding Unit Delay)/(453 Interface)	-	-	3B7/3D7	.	.	✓	✓	.	.	.	.
XR21	(Sliding Hold A)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.
XR22	(Sliding Hold B)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.
XR23	(Sliding Hold C)/(Wr Bit Mask Ctrl)	-	-	3B7/3D7	.	.	✓	✓	.	.	.	.
XR24	(Sliding Hold D)/(Wr Bit Mask Pattern)	-	-	3B7/3D7	.	.	✓	✓	.	.	.	.
XR25	(453 Pin Definition)	-	-	3B7/3D7	.	.	.	✓	.	.	.	.
XR26	(453 Configuration)	-	-	3B7/3D7	.	.	.	✓	.	.	.	.
XR27	-reserved-	-	-	3B7/3D7	.	.	.	.	.	.	.	.
XR28	Video Interface	4	R/W	3B7/3D7	- - - - 0 0 1 0	✓	✓	✓	✓	✓	✓	✓
XR29	(Function Control)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.
XR2A	(Frame Interrupt Count)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.
XR2B	Default Video	8	R/W	3B7/3D7	0 0 0 0 0 0 0 0	✓	✓	✓	.	✓	✓	
XR2C	(Force Horizontal High)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.
XR2D	(Force Horizontal Low)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.
XR2E	(Force Vertical High)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.
XR2F	(Force Vertical Low)	-	-	3B7/3D7	.	.	✓	.	.	.	.	.

Reset Codes: x = Not changed by RESET (indeterminate on power-up)      - = Not implemented (always reads 0)  
d = Set from the corresponding data bus pin on falling edge of RESET      r = Chip revision # (starting from 0000)  
h = Read-only Hercules Configuration Register Readback bits      0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column  
Note: 451 = Integrated VGA, 452 = Super VGA, 455, 456 & 457 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

## 82C457 EXTENSION REGISTER SUMMARY: 30-5F

Reg	Register Name	Bits	Access	Port	Reset	Chips' 45x Product Family						
						450	451	452	453	455	456	457
XR30	(Graphics Cursor Start Address High)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR31	(Graphics Cursor Start Address Low)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR32	(Graphics Cursor End Address)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR33	(Graphics Cursor X Position High)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR34	(Graphics Cursor X Position Low)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR35	(Graphics Cursor Y Position High)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR36	(Graphics Cursor Y Position Low)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR37	(Graphics Cursor Mode)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR38	(Graphics Cursor Mask)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR39	(Graphics Cursor Color -)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR3A	(Graphics Cursor Color 1)	--	--	3B7/3D7		.	.	✓	.	.	.	.
XR3B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR3C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR3D	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR3E	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR3F	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR40	(I/O Flag)	--	--	3B7/3D7		.	.	.	✓	.	.	.
XR41	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR42	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR43	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR44	(Scratch Register -)	--	--	3B7/3D7		.	.	.	✓	.	.	.
XR45	(Scratch Register 1 / FG Color)	--	--	3B7/3D7		.	.	.	✓	.	.	.
XR46	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR47	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR48	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR49	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4A	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4D	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4E	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR4F	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR50	Panel Format	8	R/W	3B7/3D7	x 0 x x x x x x	.	.	.	.	✓	✓	✓
XR51	Display Type	7	R/W	3B7/3D7	0 0 x x 0 1 0 -	.	.	.	.	✓	✓	✓
XR52	Panel Size	6	R/W	3B7/3D7	- x x x x - x x	.	.	.	.	✓	✓	✓
XR53	Line Graphics Override	2	R/W	3B7/3D7	- - - - - x x	.	.	.	.	✓	✓	✓
XR54	Alternate Misc Output	5	R/W	3B7/3D7	x x - - 1 0 - 0	.	.	.	.	✓	✓	✓
XR55	Text Mode 350_A Compensation	5	R/W	3B7/3D7	- - - 1 x x x x	.	.	.	.	✓	✓	✓
XR56	Text Mode 350_B Compensation	5	R/W	3B7/3D7	- - - 1 x x x x	.	.	.	.	✓	✓	✓
XR57	Text Mode 400 Compensation	5	R/W	3B7/3D7	- - - 1 x x x x	.	.	.	.	✓	✓	✓
XR58	Graphics Mode 350 Compensation	7	R/W	3B7/3D7	- x x 0 x x x x	.	.	.	.	✓	✓	✓
XR59	Graphics Mode 400 Compensation	7	R/W	3B7/3D7	- x x 0 x x x x	.	.	.	.	✓	✓	✓
XR5A	Flat Panel Vertical Display Start 400	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓
XR5B	Flat Panel Vertical Display End 400	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓
XR5C	(Weight Control Clock A)	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR5D	(Weight Control Clock B)	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR5E	ACDCLK Control	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓
XR5F	Power Down Mode Refresh	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)      - = Not implemented (always reads -)  
d = Set from the corresponding data bus pin on falling edge of RESET      r = Chip revision # (starting from 0000)  
h = Read-only Hercules Configuration Register Readback bits      0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column  
Note: 451 = Integrated VGA, 452 = Super VGA, 455, 456 & 457 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

**82C457 EXTENSION REGISTER SUMMARY: 60-7F**

Chips' 45x Product Family

Reg	Register Name	Bits	Access	Port	Reset	450	451	452	453	455	456	457
XR60	Blink Rate Control	8	R/W	3B7/3D7	1 0 0 0 0 0 1 1	.	.	.	.	✓	✓	✓
XR61	<i>(Text Color Mapping Control)</i>	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR62	<i>(Text Color Shift Parameter)</i>	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR63	<i>(Graphics Color Mapping Control)</i>	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR64	Alternate Vertical Total	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓
XR65	Alternate Overflow	6	R/W	3B7/3D7	x x x - - x x x	.	.	.	.	✓	✓	✓
XR66	Alternate Vertical Sync Start	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓
XR67	Alternate Vertical Sync End	4	R/W	3B7/3D7	- - - - x x x x	.	.	.	.	✓	✓	✓
XR68	Alternate Vertical Display Enable End	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓
XR69	Flat Panel Vertical Display Start 350	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓
XR6A	Flat Panel Vertical Display End 350	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓
XR6B	Flat Panel Vertical Overflow 2	8	R/W	3B7/3D7	x x x x x x x x	.	.	.	.	✓	✓	✓
XR6C	<i>(Weight Control Clock C)</i>	--	--	3B7/3D7		.	.	.	.	✓	✓	.
XR6D	FRC & External Palette Control	8	R/W	3B7/3D7	0 1 0 0 0 0 1 1	.	.	.	.	.	✓	✓
XR6E	Polynomial FRC Control	8	R/W	3B7/3D7	1 0 1 1 1 1 0 1	.	.	.	.	.	.	✓
XR6F	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR70	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR71	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR72	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR73	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR74	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR75	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR76	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR77	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR78	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR79	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7A	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7B	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7C	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7D	-reserved-	--	--	3B7/3D7		.	.	.	.	.	.	.
XR7E	CGA/Hercules Color Select	6	R/O	3B7/3D7	- - x x x x x x	✓	✓	✓	✓	✓	✓	✓
XR7F	Dagnostic	6	R/W	3B7/3D7	- - 0 0 0 0 0 0	✓	✓	✓	.	✓	✓	✓

# 82C457 Registers

## GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register is used to enable or disable the VGA. It is also used to place the VGA in normal or setup mode.

The Global and Extension Enable Registers are accessible only during Setup mode. The Global ID Register contains the ID number that identifies the 82C457 as a Chips & Technologies product.

**Warning:** In setup mode, the Global Setup Registers actually occupy the *entire I/O space*. Only the lower 3 bits are used to decode and select these registers. To avoid bus conflicts with other peripherals, reads should only be performed at 10xh port addresses. This decode is compatible with the IBM VGA.

## GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE pin, pending CRT interrupt, display enable/Hsync output, and vertical retrace/video output. The Feature Control Register selects the Vsync function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video RAM, memory page, and video sync polarity.

## CGA / HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

## SEQUENCER REGISTERS

The Sequencer Index Register is a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4/16/32K Bytes, Odd/Even addresses (planes) and writing of data to display memory.

## CRT CONTROLLER REGISTERS

The CRT Controller Index Register is a 6-bit index to the CRT Controller Register. Twenty eight registers perform all display functions for modes: horizontal and vertical blank and sync, panning and scrolling, cursor size and location, light pen, and underline.

## GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register is a 4-bit index to the Graphics Controller Register. The Set/Reset Register controls the formatting of CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

## ATTRIBUTE CONTROLLER AND EXTERNAL COLOR PALETTE REGISTERS

The Attribute Controller Index Register is a 5-bit index to the Attribute Controller Register. A 6th bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen. External color palette registers handle CPU reads and writes to I/O address range 3C6h-3C9h. Some of the registers are located external to 82C457 in the external color palette. Inmos IMS-G176 compatible registers are documented in this manual. The 82C411 provides an IMS-G176 compatible color palette and interface, advanced power reduction features and the digital color data required for the flat panel.

## EXTENSION REGISTERS

The 82C457 defines a set of extension registers which are addressed with the 7-bit Extension Register Index. The I/O Port Address (3D6/3D7h) and Read/Write access to the extension registers is controlled by the Extension Enable Register (103h).

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

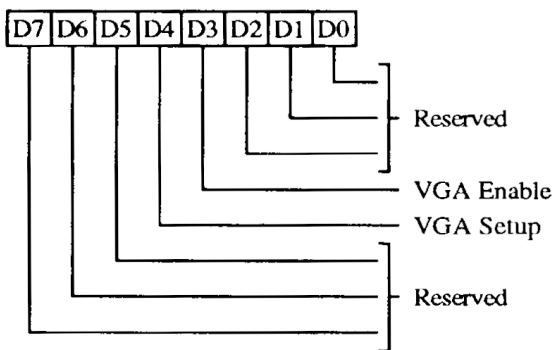
1. Miscellaneous Registers include the 82C457 Version number, Dip Switch CPU interface and paging control, memory mode control, power down / refresh control, blink rate and diagnostic functions.
2. General Purpose Registers allow the CPU to individually switch two outputs (ERMEN/ and TRAP/). They also handle video blanking interface and the video default color.
3. Backwards Compatibility Registers control Hercules, MDA, and CGA emulation modes. Trap Enable and Trap Status as well as Write Protect functions are provided to increase flexibility in providing backwards compatibility.
4. Alternate Horizontal and Vertical Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for both flat panels and backwards compatibility.
5. Panel Control Registers operate only in flat panel mode. The Panel Control Registers determine panel and video interface format, display type and size, line drawing character function, and grayscale selection and weighting, flat panel bias clocks and Frame Rate Control generation.
6. Compensation Registers provide vertical centering, blank line insertion, and graphics stretching features. For 350 and 400 line display modes, registers are provided to control display start and end locations, blank line insertion in text modes and stretching in both graphics and text modes.

# 82C457 Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
—	Setup Control	—	W	46E8h (PC-Bus only)	—	29
—	Global Enable	—	RW	102h & Setup mode	—	29
—	Extension Enable	—	RW	103h & Setup mode	—	30
—	Global ID	—	R	104h & Setup mode	—	30

## SETUP CONTROL REGISTER

Write only at I/O Address 46E8h

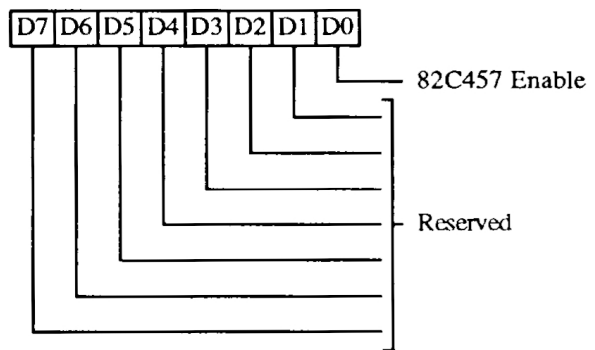


This register is cleared by RESET.

- 2-0 Reserved (0)
- 3 VGA Enable
  - 0 VGA is disabled
  - 1 VGA is enabled
- 4 Setup Mode
  - 0 VGA is in Normal Mode
  - 1 VGA is in Setup Mode
- 7-5 Reserved (0)

## GLOBAL ENABLE REGISTER

Read/Write at I/O Address 102h



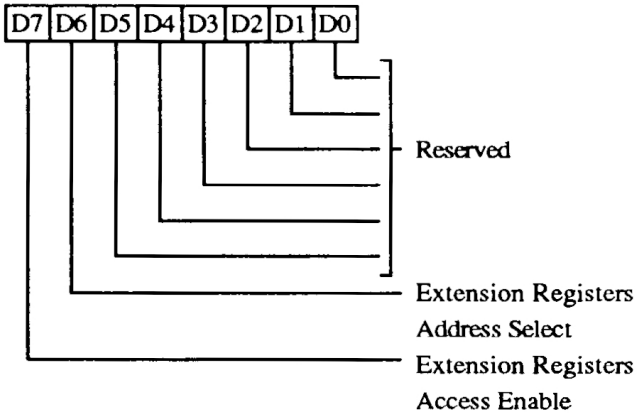
This register is only accessible in Setup Mode. It is cleared by RESET.

- 0 VGA Enable
  - 0 VGA is disabled
  - 1 VGA is enabled
- 7-1 Reserved (0)



## EXTENSION ENABLE REGISTER

Read/Write at I/O Address 103h

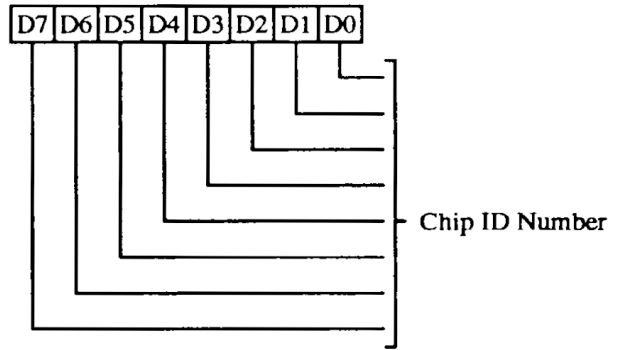


This register is only accessible in Setup Mode. It is cleared by RESET.

- 3-0 Reserved (0)
- 4 Reserved (0) This bit must be set to zero for proper operation of the 82C457.
- 5 Reserved (0)
- 6 Address for Extension Registers
  - 0 Extension registers at I/O Address 3D6/3D7h
  - 1 Extension registers at I/O Address 3B6/3B7h
- 7 Extension Registers Access Enable
  - 0 Disable Access
  - 1 Enable Access

## GLOBAL ID REGISTER

Read only at I/O Address 104h



This register is only accessible in Setup Mode.

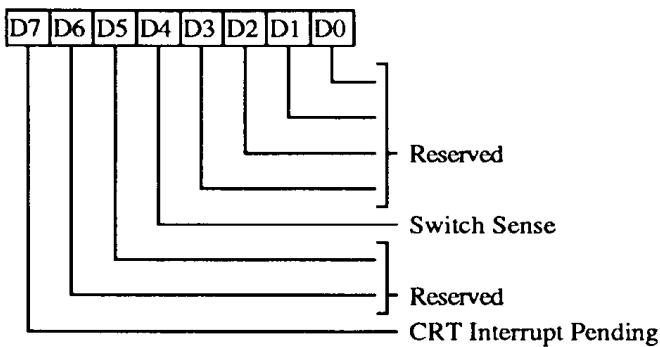
- 7-0 These bits contain the ID number (A5h). This identifies the chip as a Chips and Technologies product.

# 82C457 General Control & Status Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	-	R	3C2h	-	31
ST01	Input Status 1	-	R	3BAh/3DAh	-	31
FCR	Feature Control	-	W	3BAh/3DAh	5	32
MSR	Miscellaneous Output	-	R	3CAh	5	32
			W	3C2h		
			R	3CCh		

## INPUT STATUS REGISTER 0 (ST00)

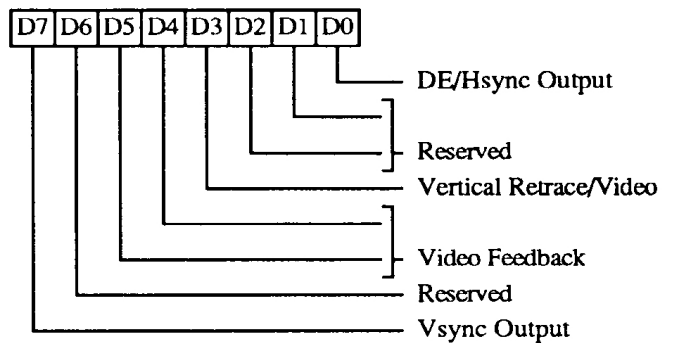
Read only at I/O Address at 3C2h



- 3-0 Reserved (0)
- 4 Switch Sense. This bit returns the Status of the SENSE pin.
- 6-5 Reserved. These bits read back 00.
- 7 CRT Interrupt Pending
  - 0 Indicates no CRT interrupt is pending
  - 1 Indicates a CRT interrupt is waiting to be serviced

## INPUT STATUS REGISTER 1 (ST01)

Read only at I/O Address 3BAh/3DAh



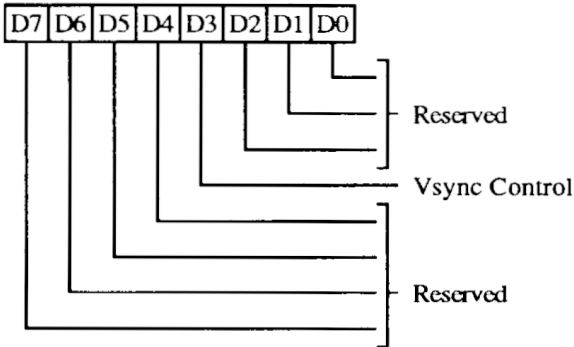
- 0 Display Enable/HSYNC Output. The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-4).
  - 0 Indicates DE or HSYNC inactive
  - 1 Indicates DE or HSYNC active
- 2-1 Reserved (0)
- 3 Vertical Retrace/Video. The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-5).
  - 0 Indicates VSYNC or video inactive
  - 1 Indicates VSYNC or video active
- 5-4 Video Feedback 1, 0. These are diagnostic video bits which are selected via the Color Plane Enable Register.
- 6 Reserved (0)
- 7 Vsync Output. The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-6). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

## FEATURE CONTROL REGISTER (FCR)

Write at I/O Address 3BAh/3DAh

Read at I/O Address 3CAh

Group 5 Protection



This register is cleared by RESET.

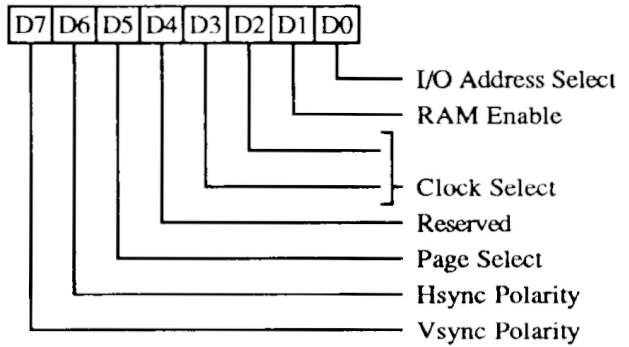
- 2-0 Reserved (0)
- 3 Vsync Control
  - 0 Vsync output on the VSYNC pin
  - 1 Logical 'OR' of Vsync and Display Enable output on the VSYNC pin
- 7-4 Reserved (0)

## MISCELLANEOUS OUTPUT REGISTER (MSR)

Write at I/O Address 3C2h

Read at I/O Address 3CCh

Group 5 Protection



Bits 2, 3, 6 and 7 of this register are effective in CRT Interface mode only. For flat panel mode, the Alternate Miscellaneous Output register is used. This register is cleared by RESET.

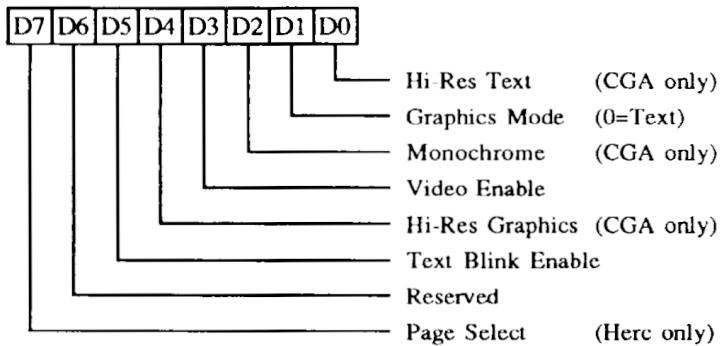
- 0 I/O Address Select. This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).
    - 0 Select 3Bxh I/O address (default)
    - 1 Select 3Dxh I/O address
  - 1 Enable RAM.
    - 0 Prevent CPU access to display memory;
    - 1 Allow CPU access to display memory.
  - 3-2 Clock Select. These bits select the dot clock source for CRT interface:
    - 00 = Select CLK0
    - 01 = Select CLK1
    - 10 = Select CLK2
    - 11 = Reserved
  - 4 Reserved (0)
  - 5 Page Select. In Odd/Even Memory Map Mode 1 (GR06), this bit selects the upper or lower 64K byte page in display memory for CPU access: 1=select lower page; 0=select upper page.
  - 6 CRT Hsync Polarity: 0=pos, 1=neg
  - 7 CRT Vsync Polarity: 0=pos, 1=neg
- (Blank pin polarity can be controlled via the Video Interface Register)

# 82C457 CGA / Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	RW	3D8h	–	33
COLOR	CGA Color Select	–	RW	3D9h	–	34
HCFG	Hercules Configuration	–	RW	3BFh	–	35

## CGA / HERCULES MODE CONTROL REGISTER (MODE)

Read/Write at I/O Address 3B8h/3D8h



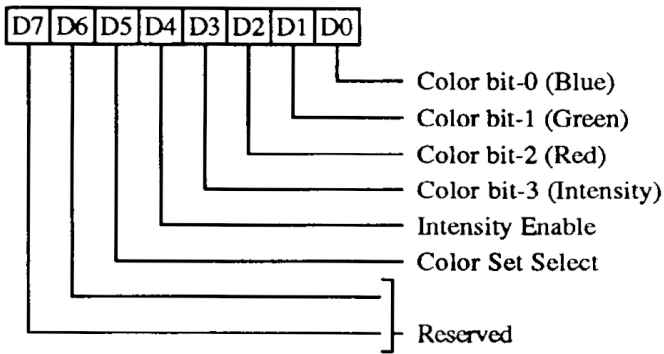
This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

- 0** CGA 80/40 Column Text Mode
  - 0 Select 40 column CGA text mode
  - 1 Select 80 column CGA text mode
- 1** CGA/Hercules Graphics/Text Mode
  - 0 Select text mode
  - 1 Select graphics mode

- 2** CGA Mono/Color Mode
  - 0 Select CGA color mode
  - 1 Select CGA monochrome mode
- 3** CGA/Hercules Video Enable
  - 0 Blank the screen
  - 1 Enable video output
- 4** CGA High Resolution Mode
  - 0 Select 320x200 graphics mode
  - 1 Select 640x200 graphics mode
- 5** CGA/Hercules Text Blink Enable
  - 0 Disable character blink attribute (blink attribute bit-7 used to control background intensity)
  - 1 Enable character blink attribute
- 6** Reserved (0)
- 7** Hercules Page Select
  - 0 Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode
  - 1 Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

## CGA COLOR SELECT REGISTER

Read/Write at I/O Address 3D9h



This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by RESET.

### 3-0 Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color: Foreground Color (color when the pixel value is 1)

The background color (color when the pixel value is 0) is black.

### 4 Intensity Enable

Text Mode: Enables intensified background colors

320x200 4-color: Enables intensified colors 0-3

640x200 2-color: Don't care

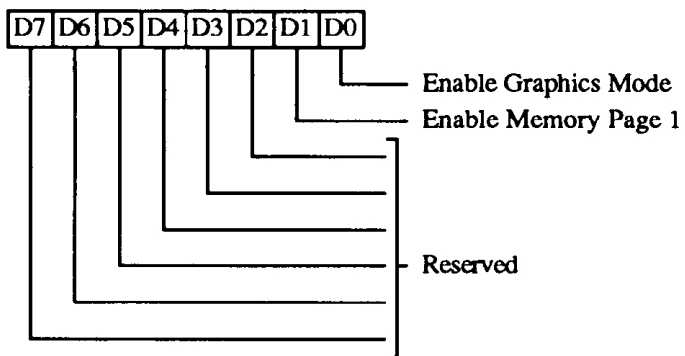
### 5 Color Set Select. This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:

Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

### 7-6 Reserved (0)

## HERCULES CONFIGURATION REGISTER (HCFG)

Write only at I/O Address 3BFh



This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14bits3&2. It is cleared by RESET.

### 0 Enable Graphics Mode

0 Lock the 82C457 in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh.

1 Permit entry to Hercules Graphics mode.

### 1 Enable Memory Page 1

0 Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.

1 The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.

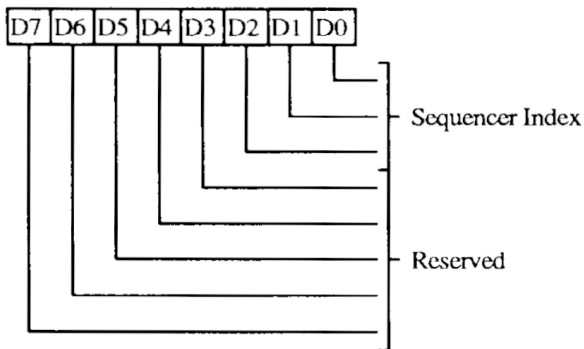
### 7-2 Reserved (0)

# 82C457 Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	RW	3C4h	1	37
SR00	Reset	00h	RW	3C5h	1	37
SR01	Clocking Mode	01h	RW	3C5h	1	38
SR02	Plane/Map Mask	02h	RW	3C5h	1	38
SR03	Character Font	03h	RW	3C5h	1	39
SR04	Memory Mode	04h	RW	3C5h	1	40
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	40

## SEQUENCER INDEX REGISTER (SRX)

Read/Write at I/O Address 3C4h



This register is cleared by RESET.

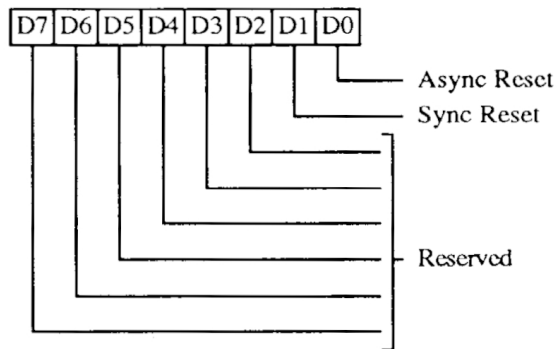
- 2-0** These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.
- 7-3** Reserved (0)

## SEQUENCER RESET REGISTER (SR00)

Read/Write at I/O Address 3C5h

Index 00h

Group 1 Protection



- 0** Asynchronous Reset
  - 0 Force asynchronous reset
  - 1 Normal operation
- 1** Synchronous Reset
  - 0 Force synchronous reset
  - 1 Normal operation

Display memory data will be corrupted if this bit is set to zero.

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tens of microseconds).

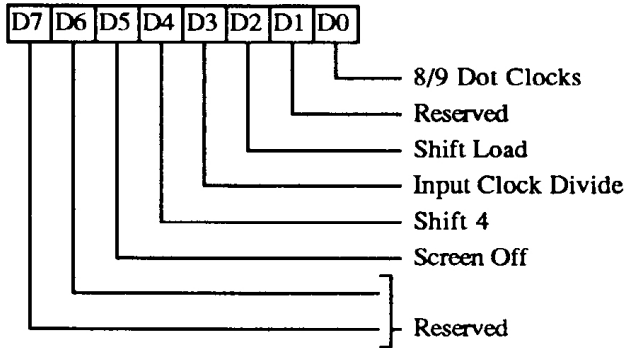
- 7-2** Reserved (0)

**SEQUENCER CLOCKING MODE REGISTER (SR01)**

*Read/Write at I/O Address 3C5h*

*Index 01h*

*Group 1 Protection*



**0** 8/9 Dot Clocks. This bit determines whether a character clock is 8 or 9 dot clocks long.

- 0 Select 9 dots/character clock
- 1 Select 8 dots/character clock

**1** Reserved (0)

**2** Shift Load

- 0 Load video data shift registers every character clock
- 1 Load video data shift registers every other character clock

Bit-4 of this register must be 0 for this bit to be effective.

**3** Input Clock Divide

- 0 Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
- 1 Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

**4** Shift 4

- 0 Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register)
- 1 Load shift registers every 4th character clock.

**5** Screen Off

- 0 Normal Operation
- 1 Disable video output and assign all display memory bandwidth for CPU accesses

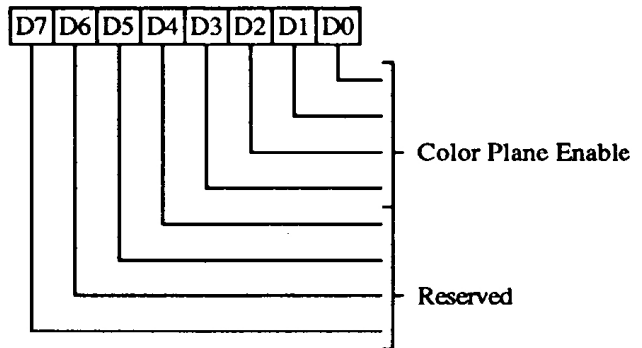
**7-6** Reserved (0)

**SEQUENCER PLANE/MAP MASK REGISTER (SR02)**

*Read/Write at I/O Address 3C5h*

*Index 02h*

*Group 1 Protection*



**3-0** Color Plane Enable

- 0 Write protect corresponding color plane
- 1 Allow write to corresponding color plane.

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.

**7-4** Reserved (0)

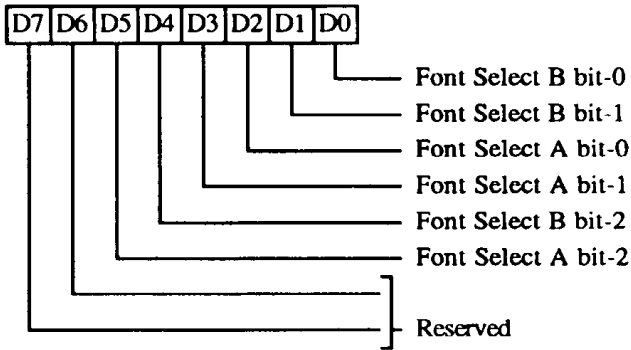


## CHARACTER FONT SELECT REGISTER (SR03)

Read/Write at I/O Address 3C5h

Index 03h

Group 1 Protection



In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04D1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

- 1-0 Lower bits of Character Generator Select B
- 3-2 Lower bits of Character Generator Select A
- 4 High bit of Character Generator Select B
- 5 High bit of Character Generator Select A
- 7-6 Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

Code	Character Generator Table Location
0	First 8K of Plane 2
1	Third 8K of Plane 2
2	Fifth 8K of Plane 2
3	Seventh 8K of Plane 2
4	Second 8K of Plane 2
5	Fourth 8K of Plane 2
6	Sixth 8K of Plane 2
7	Eighth 8K of Plane 2

where 'code' is:

Character Generator Select A (bits 5, 3, 2) when bit-3 of the the attribute byte is one.

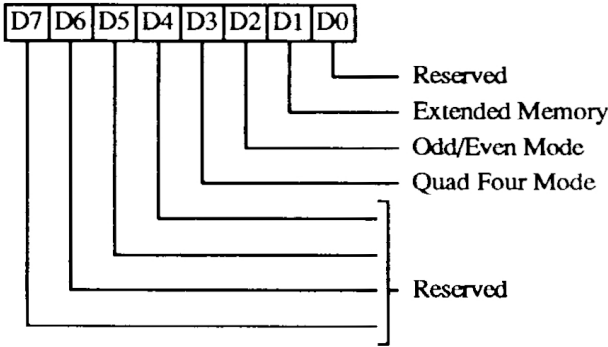
Character Generator Select B (bits 4, 1, 0) when bit-3 of the attribute byte is zero.

**SEQUENCER MEMORY MODE REGISTER (SR04)**

*Read/Write at I/O Address 3C5h*

*Index 04h*

*Group 1 Protection*



- 0** Reserved (0)
- 1** Extended Memory
  - 0 Restrict CPU access to 4/16/32 Kbytes
  - 1 Allow complete access to memory

This bit should normally be 1.
- 2** Odd/Even Mode
  - 0 CPU accesses to Odd/Even addresses are directed to corresponding odd/even planes
  - 1 All planes are accessed simultaneously (IRGB color)

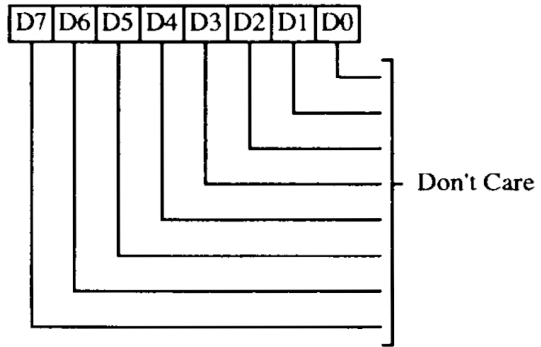
Bit-3 of this register must be 0 for this bit to be effective. This bit affects only CPU write accesses to display memory.
- 3** Quad Four Mode
  - 0 CPU addresses are mapped to display memory as defined by bit-2 of this register
  - 1 CPU addresses are mapped to display memory modulo 4. The two low order CPU address bits select the display memory plane.

This bit affects both CPU reads and writes to display memory.
- 7-4** Reserved (0)

**SEQUENCER HORIZONTAL CHARACTER COUNTER RESET REGISTER (SR07)**

*Read/Write at I/O Address 3C5h*

*Index 07h*



Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal and vertical counters will both be set to zero. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

*This is a standard VGA register which was not documented by IBM.*

## 82C457 CRT Controller Registers

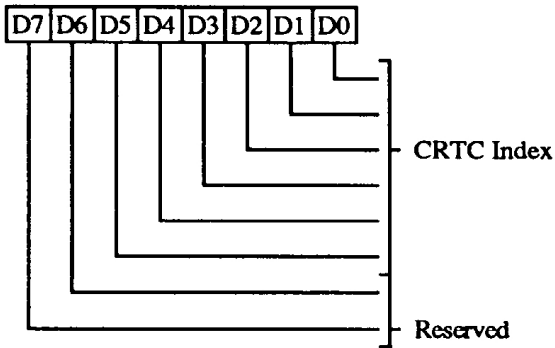
Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	RW	3B4h/3D4h	–	42
CR00	Horizontal Total	00h	RW	3B5h/3D5h	0	42
CR01	Horizontal Display Enable End	01h	RW	3B5h/3D5h	0	42
CR02	Horizontal Blank Start	02h	RW	3B5h/3D5h	0	43
CR03	Horizontal Blank End	03h	RW	3B5h/3D5h	0	43
CR04	Horizontal Sync Start	04h	RW	3B5h/3D5h	0	44
CR05	Horizontal Sync End	05h	RW	3B5h/3D5h	0	44
CR06	Vertical Total	06h	RW	3B5h/3D5h	0	45
CR07	Overflow	07h	RW	3B5h/3D5h	0/3	45
CR08	Preset Row Scan	08h	RW	3B5h/3D5h	3	46
CR09	Maximum Scan Line	09h	RW	3B5h/3D5h	2/4	46
CR0A	Cursor Start Scan Line	0Ah	RW	3B5h/3D5h	2	47
CR0B	Cursor End Scan Line	0Bh	RW	3B5h/3D5h	2	47
CR0C	Start Address High	0Ch	RW	3B5h/3D5h	–	48
CR0D	Start Address Low	0Dh	RW	3B5h/3D5h	–	48
CR0E	Cursor Location High	0Eh	RW	3B5h/3D5h	–	48
CR0F	Cursor Location Low	0Fh	RW	3B5h/3D5h	–	48
CR10	Vertical Sync Start (See Note 2)	10h	W or RW	3B5h/3D5h	4	49
CR11	Vertical Sync End (See Note 2)	11h	W or RW	3B5h/3D5h	3/4	49
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	49
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	49
CR12	Vertical Display Enable End	12h	RW	3B5h/3D5h	4	50
CR13	Offset	13h	RW	3B5h/3D5h	3	50
CR14	Underline Row	14h	RW	3B5h/3D5h	3	50
CR15	Vertical Blank Start	15h	RW	3B5h/3D5h	4	51
CR16	Vertical Blank End	16h	RW	3B5h/3D5h	4	51
CR17	CRT Mode Control	17h	RW	3B5h/3D5h	3/4	52
CR18	Line Compare	18h	RW	3B5h/3D5h	3	53
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	54
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	54
CR3x	Clear Vertical Display Enable	3xh	W	3B5h/3D5h	–	54

**Note 1:** The emulation mode affects the I/O address of the CRTC. When MDA or Hercules emulation is enabled, the CRTC I/O is 3D0h-3D7h. This overrides the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh). In this case, the index appears at the even addresses and the data at the odd addresses.

**Note 2:** In the EGA, all CRTC registers except the cursor (CR0C-CR0F) and light pen (CR10 and CR11) registers are write-only (i.e., no read back). In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03bit7) of whether the vertical sync or light pen registers are readable at indices 10-11.

### CRTC INDEX REGISTER (CRX)

Read/Write at I/O Address 3B4h/3D4h



5-0 CRTC data register index

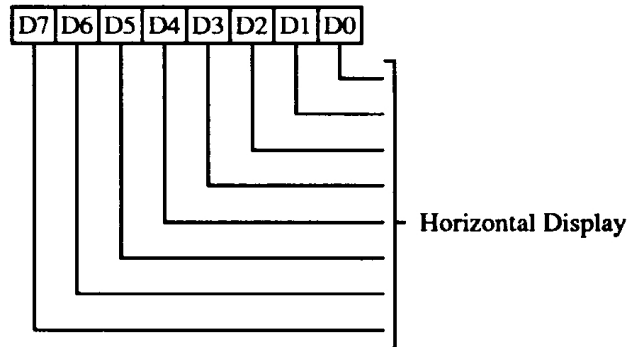
7-6 Reserved (0)

### HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)

Read/Write at I/O Address 3B5h/3D5h

Index 01h

Group 0 Protection



This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

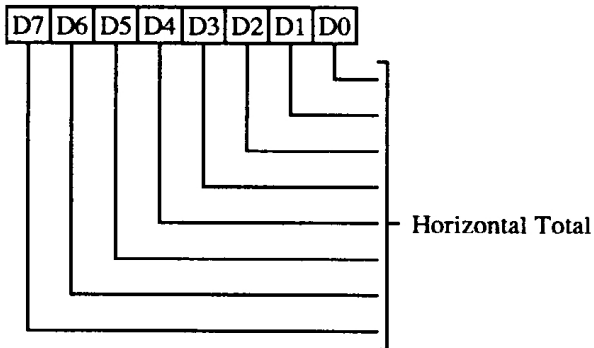
7-0 Number of Characters displayed per scan line - 1.

### HORIZONTAL TOTAL REGISTER (CR00)

Read/Write at I/O Address 3B5h/3D5h

Index 00h

Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

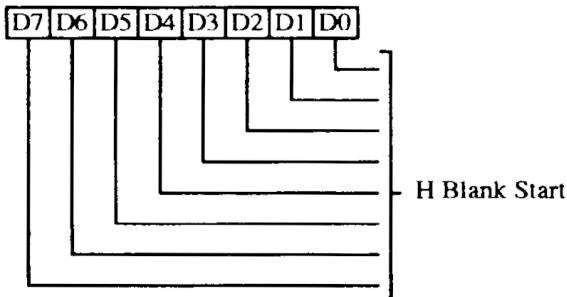
7-0 Horizontal Total. Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

## HORIZONTAL BLANK START REGISTER (CR02)

Read/Write at I/O Address 3B5h/3D5h

Index 02h

Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

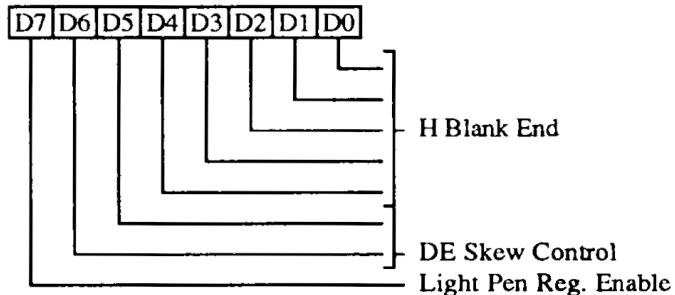
- 7-0** These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

## HORIZONTAL BLANK END REGISTER (CR03)

Read/Write at I/O Address 3B5h/3D5h

Index 03h

Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

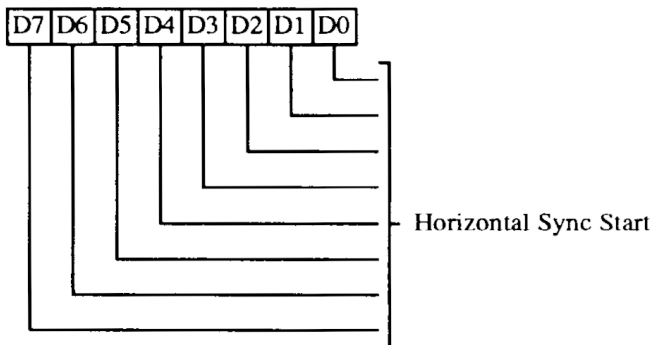
- 4-0** These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. If the horizontal blank width desired is  $W$  clocks, the 5-bit value programmed in this register =  $[\text{contents of CR02} + W] \text{ AND } 1Fh$ . The most significant bit is programmed in CR05 bit-7. This bit =  $[(\text{CR02} + W) \text{ AND } 20h] / 20h$ .
- 6-5** Display Enable Skew Control: Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.
- 7** Light Pen Reg. Enable: Must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.

## HORIZONTAL SYNC START REGISTER (CR04)

Read/Write at I/O Address 3B5h/3D5h

Index 04h

Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

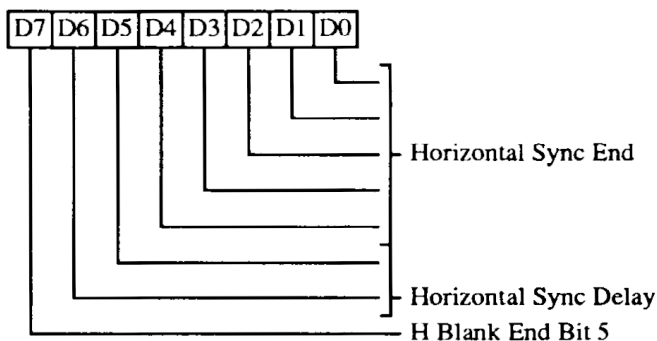
- 7-0 These bits specify the beginning of Hsync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

## HORIZONTAL SYNC END REGISTER (CR05)

Read/Write at I/O Address 3B5h/3D5h

Index 05h

Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

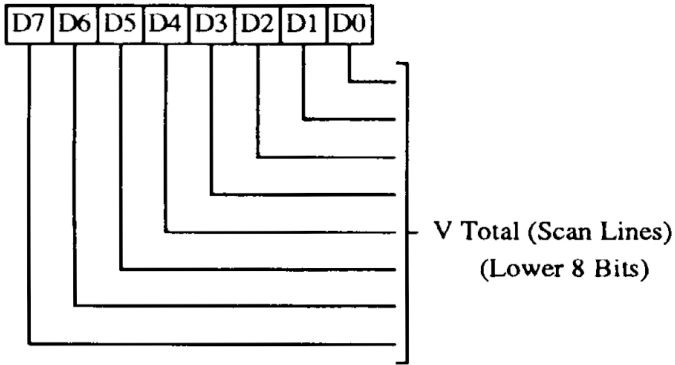
- 4-0 Hsync End. Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. If the horizontal sync width desired is N clocks, then these bits =  $(N + \text{contents of CR04}) \text{ AND } 1Fh$ .
- 6-5 Horizontal Sync Delay. These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.
- 7 Horizontal Blank End Bit 5. Sixth bit of the Horizontal Blank End Register (CR03).

### VERTICAL TOTAL REGISTER (CR06)

Read/Write at I/O Address 3B5h/3D5h

Index 06h

Group 0 Protection



This register is used in all modes.

**7-0** These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count - 2

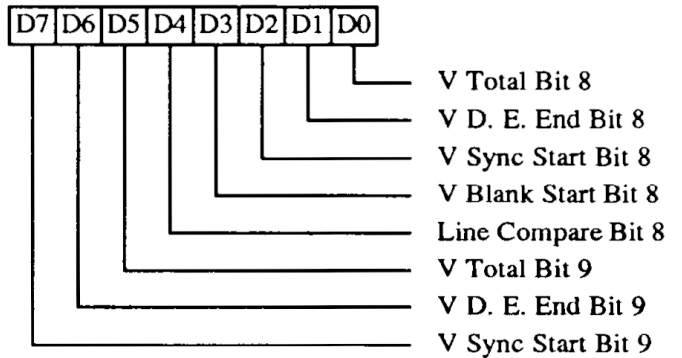
### OVERFLOW REGISTER (CR07)

Read/Write at I/O Address 3B5h/3D5h

Index 07h

Group 0 Protection on bits 0-3 and bits 5-7

Group 3 Protection on bit 4



This register is used in all modes.

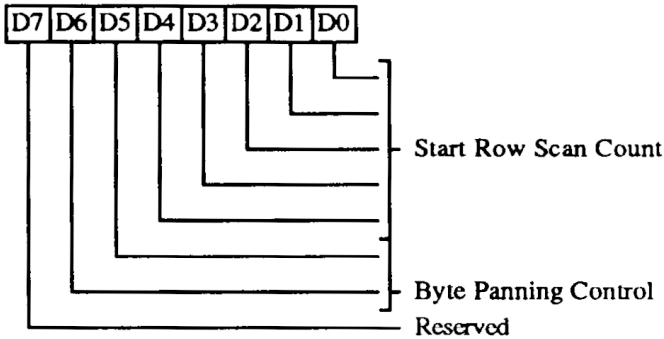
**0** Vertical Total Bit 8  
**1** Vertical Display Enable End Bit 8  
**2** Vertical Sync Start Bit 8  
**3** Vertical Blank Start Bit 8  
**4** Line Compare Bit 8  
**5** Vertical Total Bit 9  
**6** Vertical Display Enable End Bit 9  
**7** Vertical Sync Start Bit 9

### PRESET ROW SCAN REGISTER (CR08)

Read/Write at I/O Address 3B5h/3D5h

Index 08h

Group 3 Protection



- 4-0 These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.
- 6-5 Byte Panning Control. These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.
- 7 Reserved (0)

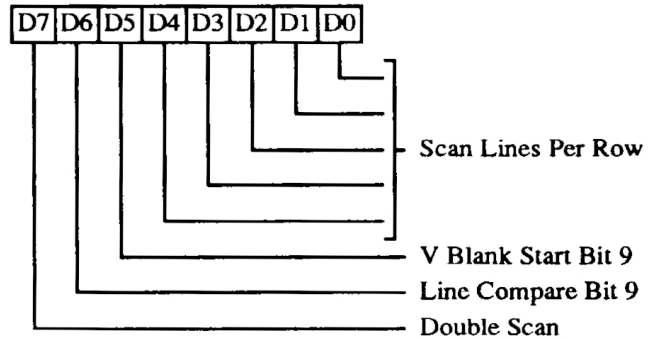
### MAXIMUM SCAN LINE REGISTER (CR09)

Read/Write at I/O Address 3B5h/3D5h

Index 09h

Group 2 Protection on bits 0-4

Group 4 Protection on bit 5-7



- 4-0 These bits specify the number of scan lines in a row: Number of scan lines per row = value + 1.
- 5 Bit 9 of the Vertical Blank Start register
- 6 Bit 9 of the Line Compare register
- 7 Double Scan
  - 0 Normal Operation
  - 1 Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRT row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.



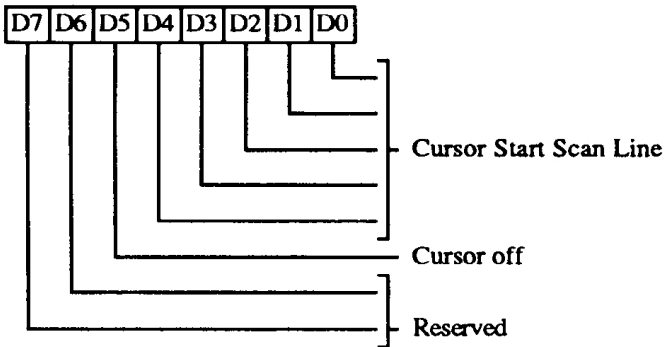
### CURSOR START SCAN LINE

#### REGISTER (CR0A)

Read/Write at I/O Address 3B5h/3D5h

Index 0Ah

Group 2 Protection



**4-0** These bits specify the scan line of the character row where the cursor display begins.

**5** Cursor Off

0 Text Cursor On

1 Text Cursor Off

**7-6** Reserved (0)

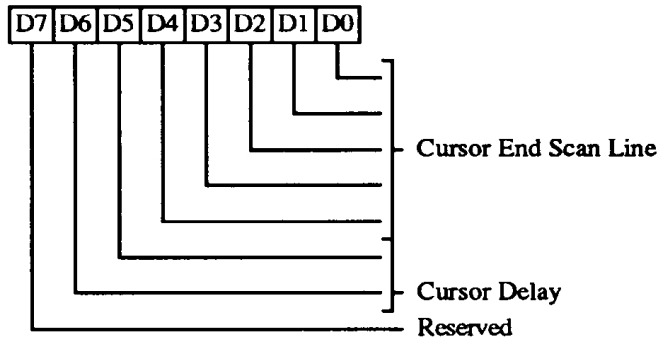
### CURSOR END SCAN LINE

#### REGISTER (CR0B)

Read/Write at I/O Address 3B5h/3D5h

Index 0Bh

Group 2 Protection



**4-0** These bits specify the scan line of a character row where the cursor display ends: Last scan line for the block cursor = Value + 1.

**6-5** These bits define the number of character clocks that the cursor is delayed to compensate for internal pipeline delay.

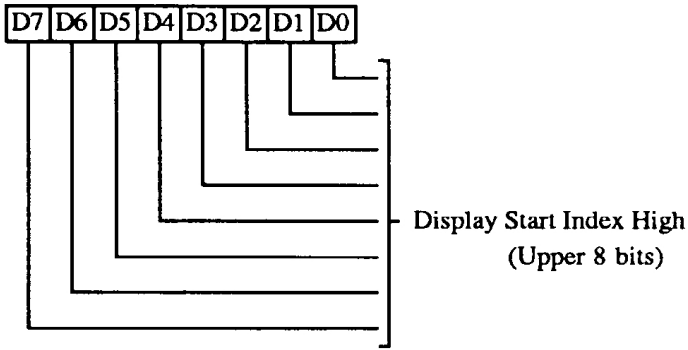
**7** Reserved (0)

**Note:** If the Cursor Start Line is greater than the Cursor End Line, then no cursor is generated.

### START INDEX HIGH REGISTER (CR0C)

Read/Write at I/O Address 3B5h/3D5h

Index 0Ch

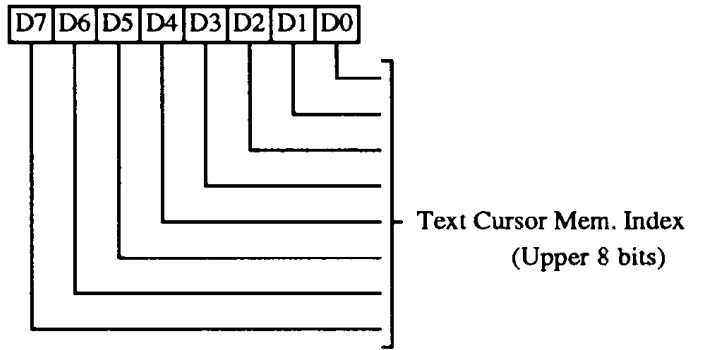


- 7-0 Upper 8 bits of display start address. In CGA/MDA/Hercules modes, this register wraps around at the 16, 32, and 64 Kbyte boundaries respectively.

### CURSOR LOCATION HIGH REGISTER (CR0E)

Read/Write at I/O Address 3B5h/3D5h

Index 0Eh

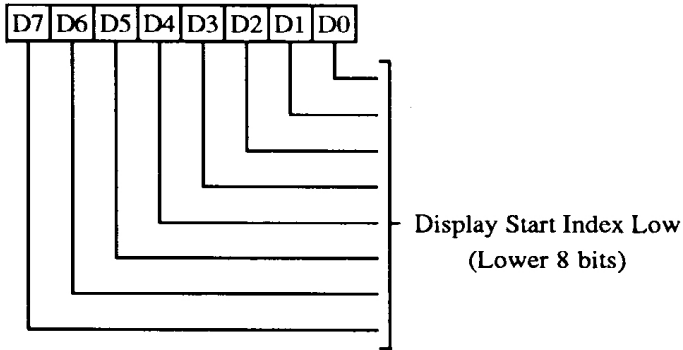


- 7-0 Upper 8 bits of the memory address where the text cursor is active. In CGA/MDA/Hercules modes, this register wraps around at 16, 32, and 64 Kbyte boundaries respectively.

### START INDEX LOW REGISTER (CR0D)

Read/Write at I/O Address 3B5h/3D5h

Index 0Dh

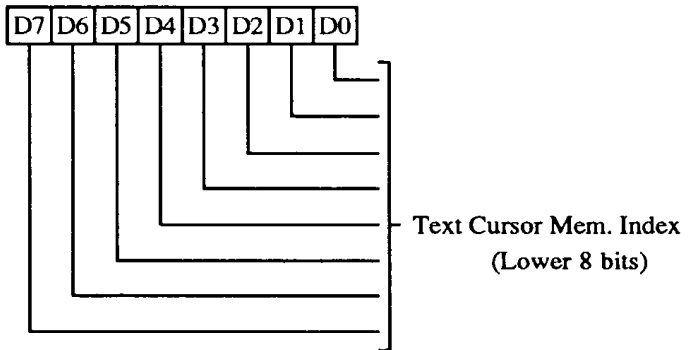


- 7-0 Lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

### CURSOR LOCATION LOW REGISTER (CR0F)

Read/Write at I/O Address 3B5h/3D5h

Index 0Fh



- 7-0 Lower 8 bits of the memory address where the text cursor is active. In CGA/MDA/Hercules modes, this register wraps around at 16, 32, and 64 Kbyte boundaries respectively.

### LIGHTPEN HIGH REGISTER (CR10)

Read only at I/O Address 3B5h/3D5h

Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

### LIGHTPEN LOW REGISTER (CR11)

Read only at I/O Address 3B5h/3D5h

Index 11h

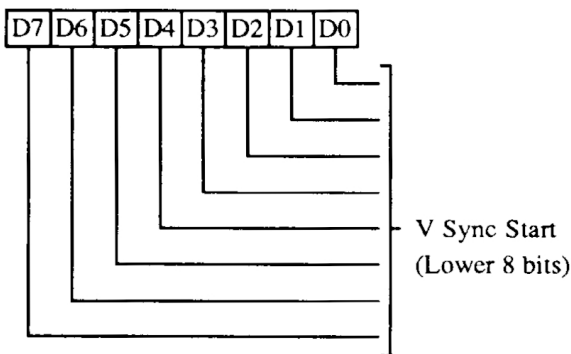
Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

### VERTICAL SYNC START REGISTER (CR10)

Read/Write at I/O Address 3B5h/3D5h

Index 10h

Group 4 Protection



This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03 bit-7=1.

- 7-0 The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

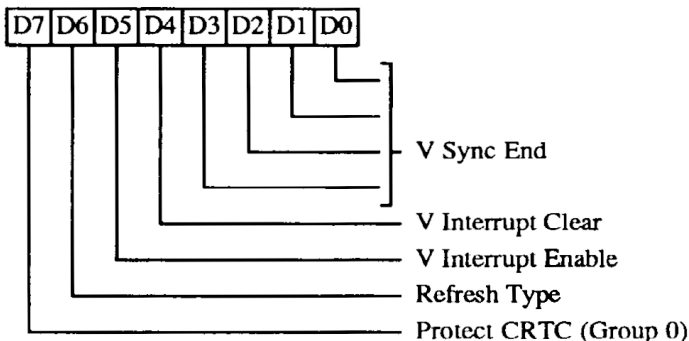
### VERTICAL SYNC END REGISTER (CR11)

Read/Write at I/O Address 3B5h/3D5h

Index 11h

Group 3 Protection for bits 4 and 5

Group 4 Protection for bits 0-3, 6 and 7



This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03 bit-7=1.

- 3-0 Vertical Sync End. Lower 4 bits of the scan line count that defines the end of vertical sync. If the vertical sync width desired is N lines, then bits 3-0 of this register = (CR10 + N) AND 0Fh.
- 4 Vertical Interrupt Clear
  - 0 Clear vertical interrupt generated on the IRQ output
  - 1 Normal operation. This bit is cleared by RESET.
- 5 Vertical Interrupt Enable
  - 0 Enable vertical interrupt
  - 1 Disable vertical interrupt. This bit is cleared by RESET.
- 6 Select Refresh Type
  - 0 3 refresh cycles per scan line
  - 1 5 refresh cycles per scan line
- 7 Group Protect 0. This bit is logically ORed with XR15 bit-6 to determine the protection for group 0 registers. This bit is cleared by RESET.
  - 0 Enable writes to CR00-CR07
  - 1 Disable writes to CR00-CR07

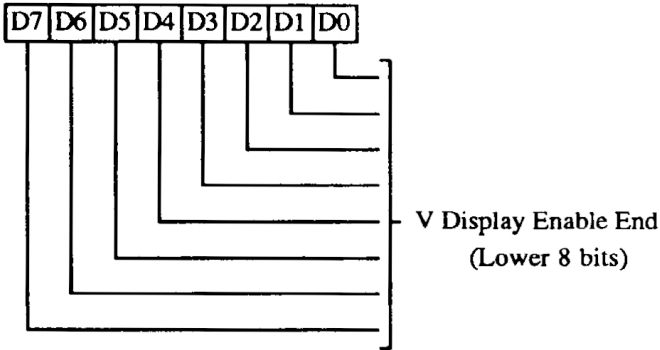
CR07 bit-4 (Line Compare bit-9) is not affected by this bit.

### VERTICAL DISPLAY ENABLE END REGISTER (CR12)

Read/Write at I/O Address 3B5h/3D5h

Index 12h

Group 4 Protection



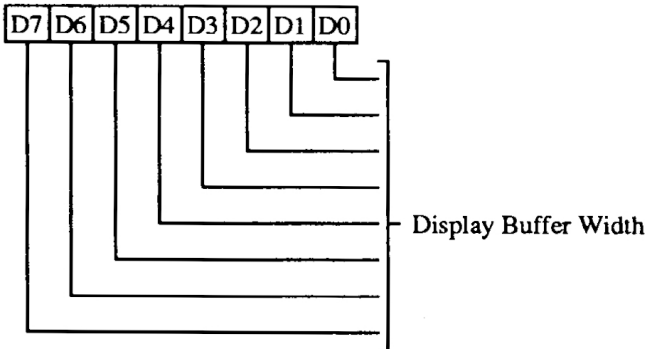
- 7-0 These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The Actual count = Contents of this register + 1.

### OFFSET REGISTER (CR13)

Read/Write at I/O Address 3B5h/3D5h

Index 13h

Group 3 Protection



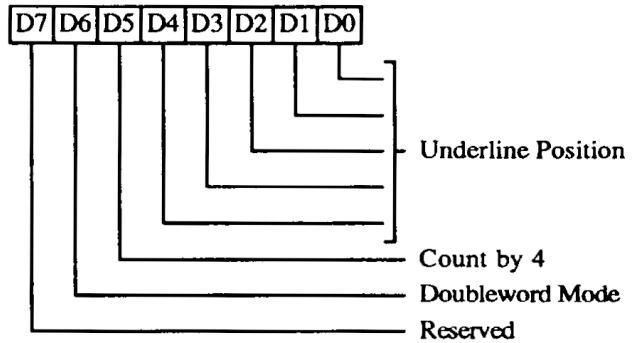
- 7-0 Display Buffer Width. The byte starting address of the next display row = Byte Start Address for current row +  $K * (CR13 + Z/2)$ , where  $Z$  = bit defined in XR0D and  $K=2$  in byte mode,  $K=4$  in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

### UNDERLINE LOCATION REGISTER (CR14)

Read/Write at I/O Address 3B5h/3D5h

Index 14h

Group 3 Protection



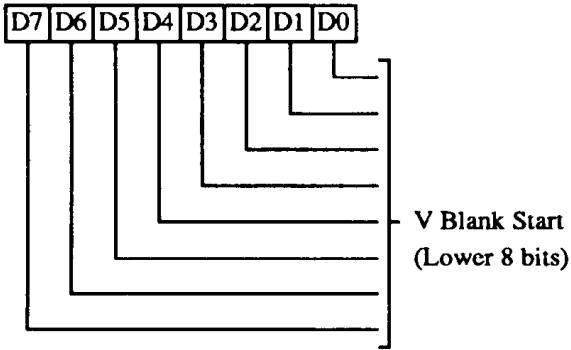
- 4-0 These bits specify the underline's scan line position within a character row. Value = Actual scan line number - 1.
- 5 Count by 4 for Doubleword Mode  
 0 Frame Buffer Address is incremented by 1 or 2  
 1 Frame Buffer Address is incremented by 4 or 2. See CR17 bit-3 for further details.
- 6 Doubleword Mode  
 0 Frame Buffer Address is byte or word address;  
 1 Frame Buffer Address is doubleword address. Used in conjunction with CR17 bit-6 to select the display memory addressing mode.
- 7 Reserved (0)

**VERTICAL BLANK START REGISTER (CR15)**

*Read/Write at I/O Address 3B5h/3D5h*

*Index 15h*

*Group 4 Protection*



This register is used in all modes.

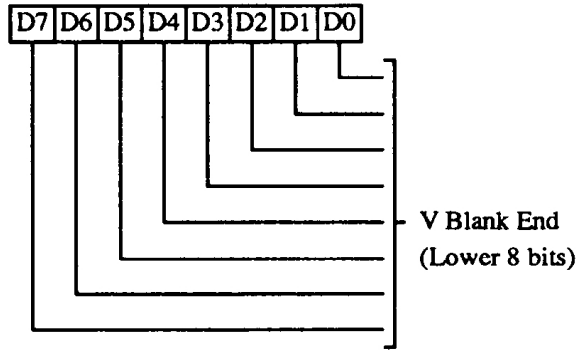
- 7-0** These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

**VERTICAL BLANK END REGISTER (CR16)**

*Read/Write at I/O Address 3B5h/3D5h*

*Index 16h*

*Group 4 Protection*



This register is used in all modes.

- 7-0** End Vertical Blank. These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. If the vertical blank width desired is Z lines these bits = (Vertical Blank Start + Z) and 0FFh.

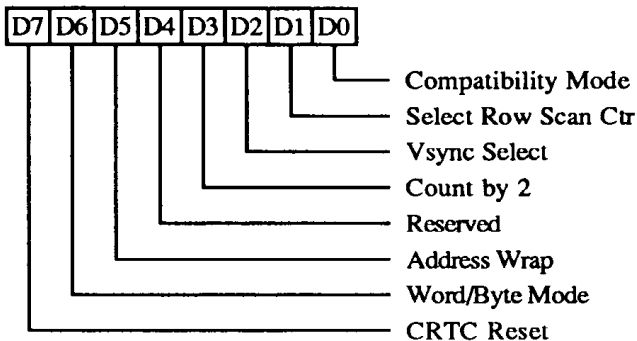
## CRT MODE CONTROL REGISTER (CR17)

Read/Write at I/O Address 3B5h/3D5h

Index 17h

Group 3 Protection for bits 0,1 and 3-5,7

Group 4 Protection for bit 2



**0** Compatibility Mode Support. This bit allows compatibility with the IBM CGA two-bank graphics mode.

- 0 The character row scan line counter bit 0 is substituted for memory address bit 13 during active display time
- 1 Normal operation, no substitution takes place.

**1** Select Row Scan Counter. This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system.

- 0 Substitute character row scan line counter bit 1 for memory address bit 14 during active display time.
- 1 Normal operation, no substitution takes place.

**2** Vertical Sync Select. This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

**3** Count By Two

- 0 Memory address counter is incremented every character clock
- 1 Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

**Note:** This bit is used in conjunction with CR14 bit-5. The net effect is as follows:

CR14 bit-5	CR17-bit-3	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

**Note:** In Hercules graphics and Hi-res CGA modes, the address increments every two clocks.

**4** Reserved (0)

**5** Address Wrap (effective only in word mode.)

- 0 Wrap display memory address at 16 Kbytes. This is used in IBM CGA mode.
- 1 Normal operation (extended mode).

**6** Word Mode or Byte Mode.

- 0 Word Mode is selected. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output
- 1 Select byte mode.

**Note:** This bit is used in conjunction with CR14 bit-6 to select byte, word, or double word memory addressing as follows:

### CR14 bit-6 CR17 bit-6 Addressing Mode

0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

**7** Hardware Rset (This bit is cleared by RESET)

- 0 Force HSYNC and VSYNC to be inactive. No other registers or outputs affected.
- 1 Normal Operation

Display memory addresses are affected by CR17 bit-6 as shown in the table below:

Logical Memory Address	Physical Memory Address		
	Byte Mode	Word Mode	Double Word Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

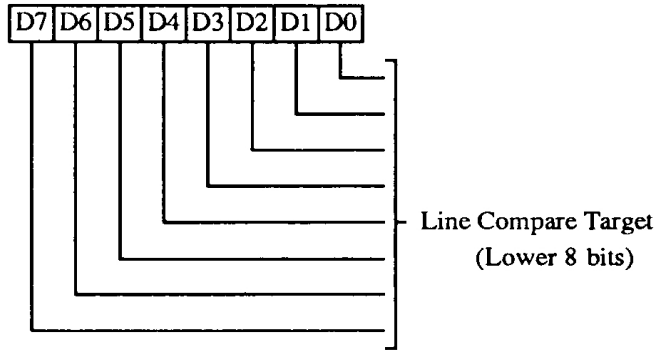
Note 1 =  $A13 * \text{NOT CR17D5} + A15 * \text{CR17D5}$   
 Note 2 =  $A12 \text{ xor } (A14 * \text{XR04D2})$   
 Note 3 =  $A13 \text{ xor } (A15 * \text{XR04D2})$

## LINE COMPARE REGISTER (CR18)

Read/Write at I/O Address 3B5h/3D5h

Index 18h

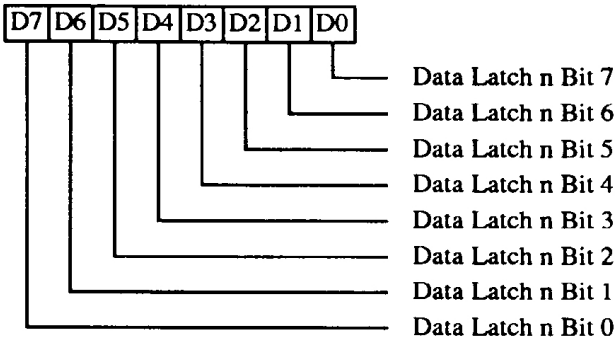
Group 3 Protection



7-0 These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09 bit-7).

**MEMORY DATA LATCH REGISTER (CR22)**

Read only at I/O Address 3B5h/3D5h  
Index 22h



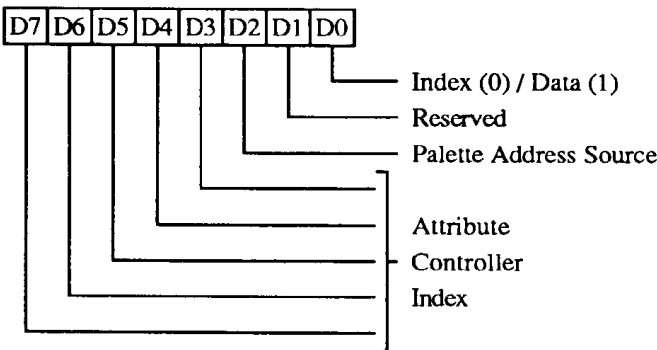
This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04 bit-0&1) and is in the range 0-3.

Writes to this register are not decoded and will be ignored.

*This is a standard VGA register which was not documented by IBM.*

**ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)**

Read only at I/O Address 3B5h/3D5h  
Index 24h



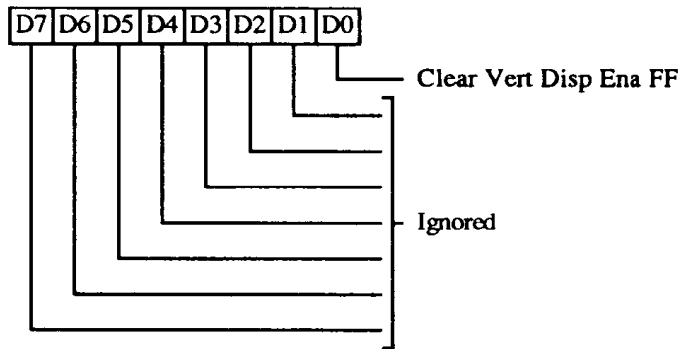
This register may be used to read back the state of the attribute controller index/data latch.

Writes to this register are not decoded and will be ignored.

*This is a standard VGA register which was not documented by IBM.*

**CLEAR VERTICAL DISPLAY ENABLE FFh (CR3x)**

Write only at I/O Address 3B5h/3D5h  
Index 3xh



Writing odd data values to CRTC index 30-3Fh causes the vertical display enable flip-flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer vertical retrace period. There are two side effects of terminating vertical display enable early: first, the screen blanks early for one frame causing a minor visual disturbance and second, the sequencer gives more display memory cycles to the CPU because vertical display is not enabled.

Reads from this register are not decoded and will return indeterminate data.

*This is a standard VGA register which was not documented by IBM.*

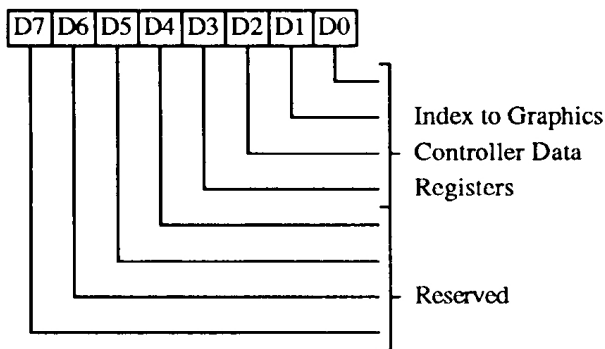


# 82C457 Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	—	W	3CEh	1	55
GR00	Set/Reset	00h	RW	3CFh	1	55
GR01	Enable Set/Reset	01h	RW	3CFh	1	56
GR02	Color Compare	02h	RW	3CFh	1	56
GR03	Data Rotate	03h	RW	3CFh	1	57
GR04	Read Map Select	04h	RW	3CFh	1	57
GR05	Graphics mode	05h	RW	3CFh	1	58
GR06	Miscellaneous	06h	RW	3CFh	1	60
GR07	Color Don't Care	07h	RW	3CFh	1	60
GR08	Bit Mask	08h	RW	3CFh	1	61

## GRAPHICS CONTROLLER INDEX REGISTER (GRX)

Write only at I/O Address 3CEh  
Group 1 Protection

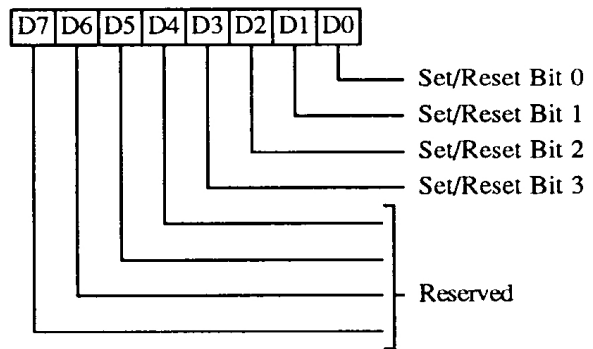


**3-0** 4-bit index to Graphics Controller registers

**7-4** Reserved (0)

## SET/RESET REGISTER (GR00)

Read/Write at I/O Address 3CFh  
Index 00h  
Group 1 Protection



The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

**3-0** When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Reset register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

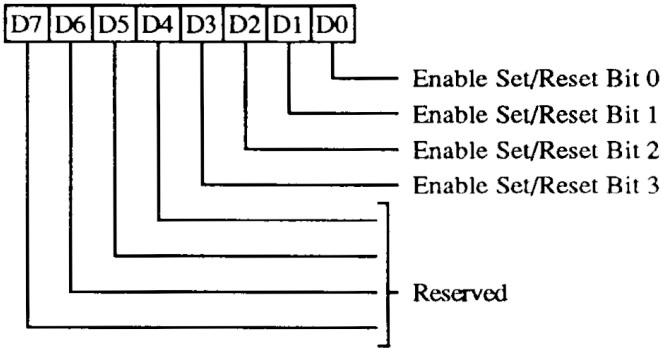
**7-4** Reserved (0)

### ENABLE SET/RESET REGISTER (GR01)

Read/Write at I/O Address 3CFh

Index 01h

Group 1 Protection



**3-0** This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

- 0 The corresponding plane is written with the data from the CPU data bus
- 1 The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

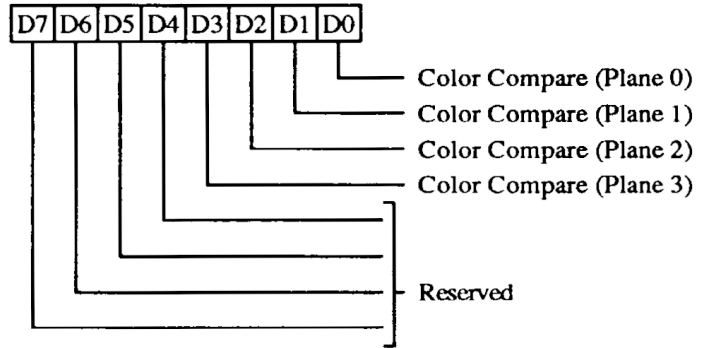
**7-4** Reserved (0)

### COLOR COMPARE REGISTER (GR02)

Read/Write at I/O Address 3CFh

Index 02h

Group 1 Protection



**3-0** This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit, a mis-match returns a logical 0.

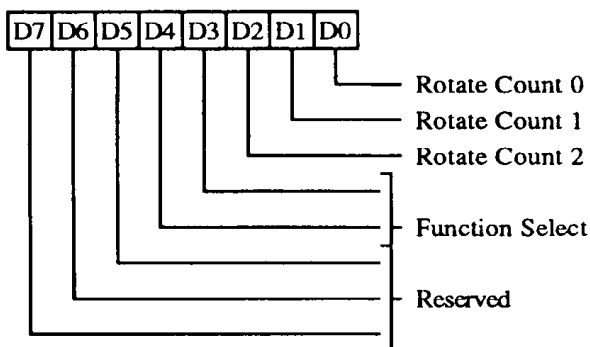
**7-4** Reserved (0)

### DATA ROTATE REGISTER (GR03)

Read/Write at I/O Address 3CFh

Index 03h

Group 1 Protection



**2-0** These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

**4-3** These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data, Latches are updated;
0	1	Logical 'AND' between Data and latched data;
1	0	Logical 'OR' between Data and latched data;
1	1	Logical 'XOR' between Data and latched data.

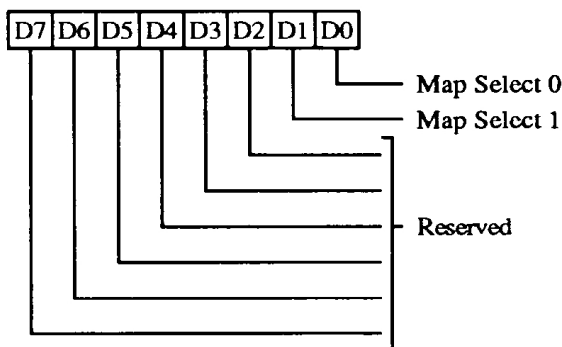
**7-5** Reserved (0)

### READ MAP SELECT REGISTER (GR04)

Read/Write at I/O Address 3CFh

Index 04h

Group 1 Protection



**1-0** This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

The four memory maps are selected as follows:

Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

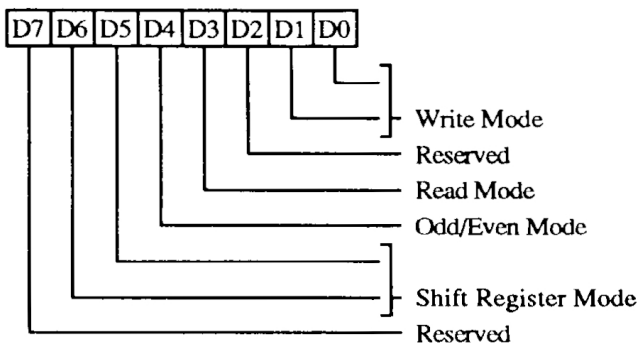
**7-2** Reserved (0)

## GRAPHICS MODE REGISTER (GR05)

Read/Write at I/O Address 3CFh

Index 05h

Group 1 Protection



**1-0** These bits specify the Write Mode as follows: (For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data).

### 1 0 Write Mode

**0 0 Write mode 0.** Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.

**0 1 Write mode 1.** Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.

**1 0 Write mode 2.** The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the

corresponding pixel in the processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.

**1 1 Write mode 3.** The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value.

A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches.

A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register.

The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

**2** Reserved (0)

**3** This bit specifies the Read Mode as follows:

**0** The CPU reads data from one of the planes as selected in the Read Map Select register.

**1** The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

**4 Odd/Even Mode:**

- 0 All CPU addresses sequentially access all planes
- 1 Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for IBM CGA-compatible memory organization.

**6-5 Shift Register Mode.** These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If the data bits in the memory planes (0-3) are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

65	Last Bit Shifted Out	Shift Direction →						1st Bit Shifted Out	Out- put to:
00:	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit3
01:	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit3
1x:	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit1
	M3D2	M2D6	M3D2	M2D6	M1D2	M1D6	M0D2	M0D6	Bit2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit3

**Note:** If the Shift Register is not loaded every character clock (see SR01bits2&4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

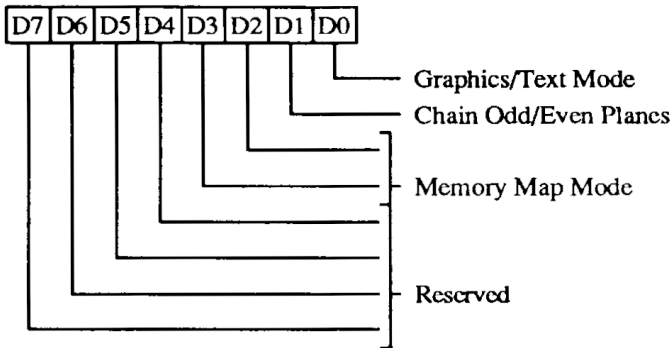
**7 Reserved (0)**

## MISCELLANEOUS REGISTER (GR06)

Read/Write at I/O Address 3CFh

Index 06h

Group 1 Protection



### 0 Graphics/Text Mode:

- 0 Text Mode
- 1 Graphics mode

### 1 Chain Odd/Even Planes. This mode can be used to double the address space into display memory.

- 1 CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:
  - A0 = 0 select planes 0 and 2
  - A0 = 1 select planes 1 and 3
- 0 A0 not replaced

### 3-2 Memory Map mode. These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

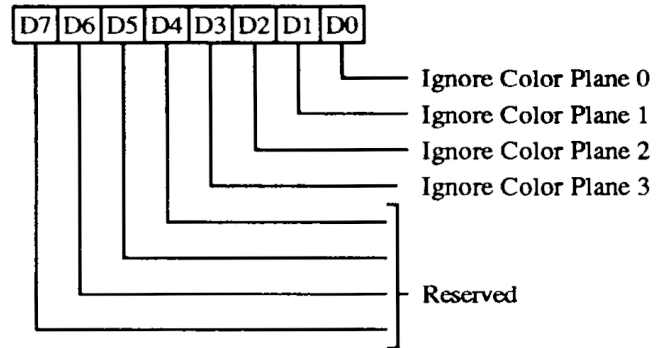
### 7-4 Reserved (0)

## COLOR DON'T CARE REGISTER (GR07)

Read/Write at I/O Address 3CFh

Index 07h

Group 1 Protection



### 3-0 Ignore Color Plane (0-3)

- 0 This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.
- 1 The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

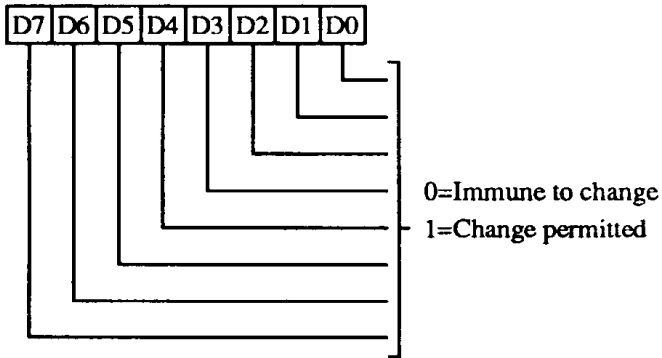
### 7-4 Reserved (0)

## BIT MASK REGISTER (GR08)

Read/Write at I/O Address 3CFh

Index 08h

Group 1 Protection



**7-0** This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the VGA), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

- 0 The corresponding bit in each of the four memory planes is written from the corresponding bit in the latches.
- 1 Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted.

## 82C457 Attribute Controller and Color Palette Registers

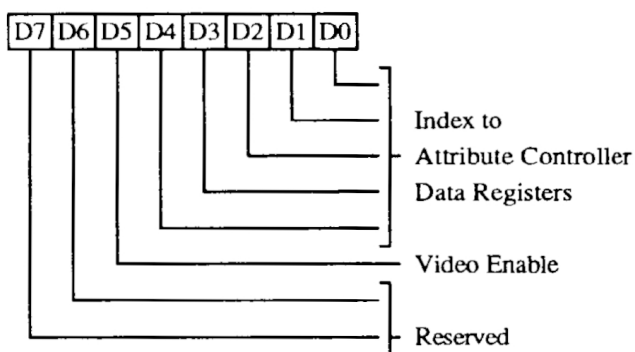
Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	RW	3C0h	1	63
AR00-AR0F	Internal Color Palette Data	00-0Fh	RW	3C0h/3C1h	1	64
AR10	Mode Control	10h	RW	3C0h/3C1h	1	64
AR11	Overscan Color	11h	RW	3C0h/3C1h	1	65
AR12	Color Plane Enable	12h	RW	3C0h/3C1h	1	65
AR13	Horizontal Pixel Panning	13h	RW	3C0h/3C1h	1	66
AR14	Pixel Pad	14h	RW	3C0h/3C1h	1	66
DACMASK	External Color Palette Pixel Mask	–	RW	3C6h	6	67
DACSTATE	External Color Palette State Register	–	R	3C7h	–	67
DACRX	External Color Palette Read-Mode Index	–	W	3C7h	6	68
DACX	External Color Palette Index (for 3C9h)	–	RW	3C8h	6	68
DACDATA	External Color Palette Data	00-FFh	RW	3C9h	6	68

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

### ATTRIBUTE INDEX REGISTER (ARX)

*Read/Write at I/O Address 3C0h  
Group 1 Protection*



- 4-0 These bits point to one of the internal registers of the Attribute Controller
- 5 Enable Video
  - 0 Disables the video, allowing the Attribute Controller color registers to be accessed by the CPU
  - 1 Enables the video and causes the Attribute Controller Color registers (AR00-AR0F) to be inaccessible by the CPU.
- 7-6 Reserved (0)



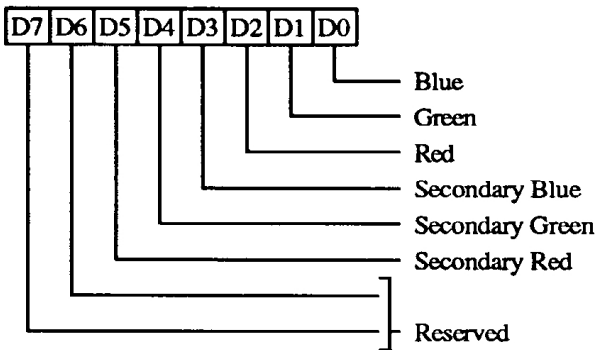
**ATTRIBUTE CONTROLLER COLOR  
PALETTE DATA REGISTERS (AR00-AR0F)**

*Read at I/O Address 3C1h*

*Write at I/O Address 3C0/1h*

*Index 00-0Fh*

*Group 1 Protection or XR63 bit-6*



**5-0** These bits are the color value in the respective palette register as pointed to by the index register.

**7-6** Reserved (0)

The Color Palette may be by-passed in flat panel mode by setting the Color Palette Enable Bit (XR63 bit-5).

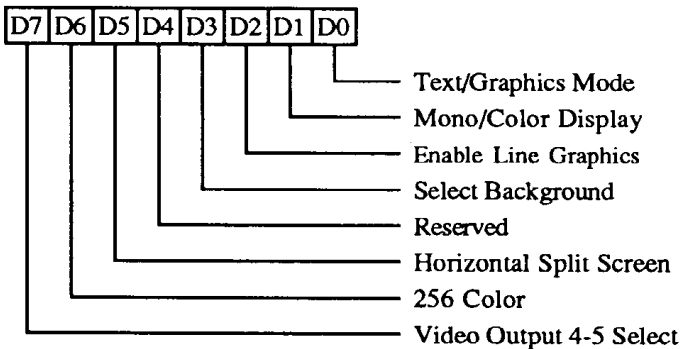
**ATTRIBUTE CONTROLLER  
MODE CONTROL REGISTER (AR10)**

*Read at I/O Address 3C1h*

*Write at I/O Address 3C0/1h*

*Index 10h*

*Group 1 Protection*



**0** Text/Graphics Mode

- 0 Select text mode
- 1 Select graphics mode

**1** Monochrome/Color Display

- 0 Select color display attributes
- 1 Select mono display attributes

**2** Enable Line Graphics Character Codes. This bit is dependent on bit 0 of the Override register.

- 0 Make the ninth pixel appear the same as the background
- 1 For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

**3** Enable Blink/Select Background Intensity. The blinking counter is clocked by the VSYNC signal. The Blink frequency is defined in the Blink Rate Control Register (XR60).

- 0 Disable Blinking and enable text mode background intensity
- 1 Enable the blink attribute in text and graphics modes.

**4** Reserved (0)

**5** Split Screen Horizontal Panning Mode

- 0 Scroll both screens horizontally as specified in the Pixel Panning register
- 1 Scroll horizontally only the top screen as specified in the Pixel panning register

**6** 256 Color Output Assembler

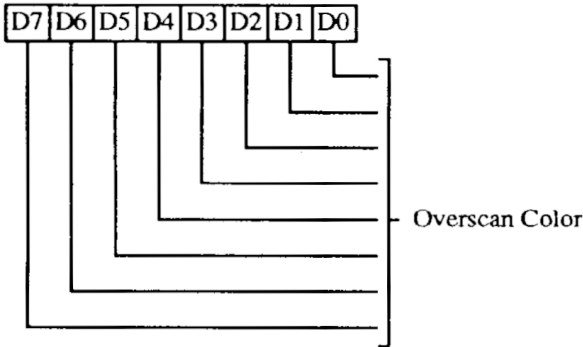
- 0 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock
- 1 Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

**7** Video Output 5-4 Select

- 0 Video bits 4 and 5 are generated by the internal Attribute Controller color palette registers
- 1 Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14)

## OVERSCAN COLOR REGISTER (AR11)

Read at I/O Address 3C1h  
Write at I/O Address 3C0/1h  
Index 11h  
Group 1 Protection

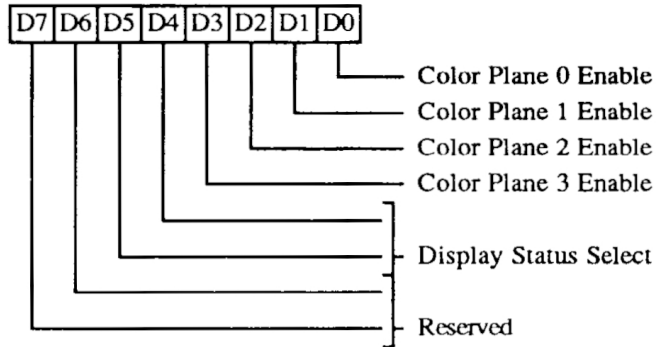


**7-0** Overscan Color. These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

## COLOR PLANE ENABLE REGISTER (AR12)

Read at I/O Address 3C1h  
Write at I/O Address 3C0/1h  
Index 12h  
Group 1 Protection



**3-0** Color Plane (0-3) Enable

0 Force the corresponding color plane pixel bit to 0 before it addresses the color palette

1 Enable the plane data bit of the corresponding color plane to pass

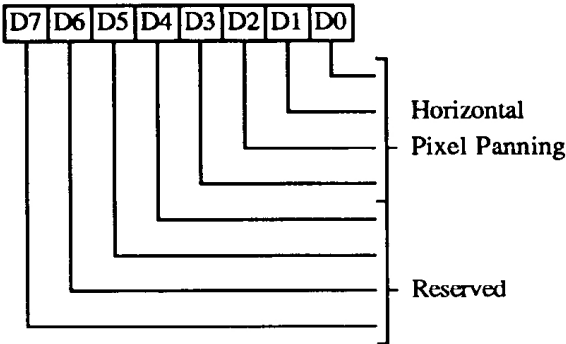
**5-4** Display Status Select. Select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

Bit 5	Bit 4	Status Register 1	
		Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

**7-6** Reserved (0)

**ATTRIBUTE CONTROLLER HORIZONTAL  
PIXEL PANNING REGISTER (AR13)**

Read at I/O Address 3C1h  
Write At I/O Address 3C01h  
Index 13h  
Group 1 Protection



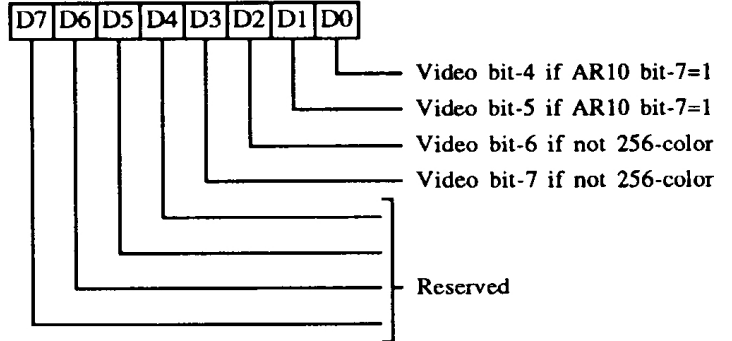
**3-0** Horizontal Pixel Panning. These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixels/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixels/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10 bit-6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

AR13	Number of Pixels Shifted		
	9-dot mode	8-dot mode	256-color mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

**7-4** Reserved (0)

**ATTRIBUTE CONTROLLER  
PIXEL PAD REGISTER (AR14)**

Read at I/O Address 3C1h  
Write At I/O Address 3C01h  
Index 14h  
Group 1 Protection



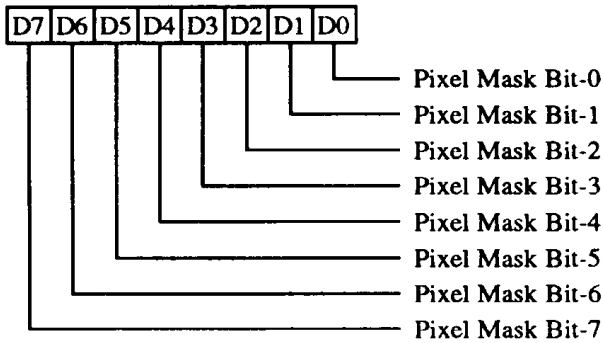
**1-0** These bits are output as video bits 4 and 5 when AR10 bit-7 = 1. They are disabled in the 256 color mode.

**3-2** These bits are output as video bits 6 and 7 in all modes except 256-color mode.

**7-4** Reserved (0)

**EXTERNAL COLOR PALETTE  
PIXEL MASK REGISTER (DACMASK)**

*Read/Write at I/O Address 3C6h  
Group 6 Protection*

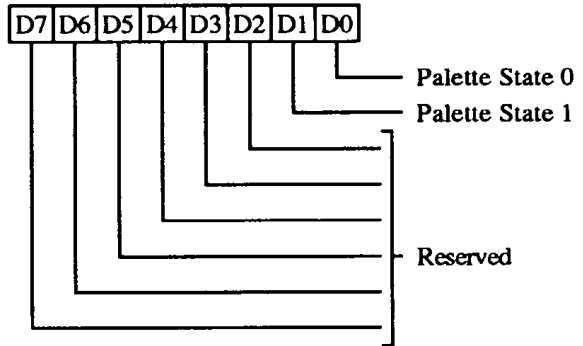


The contents of this register are logically ANDed with the 8 bits of video data coming into the external color palette. Zero bits in this register therefore cause the corresponding address input to the external color palette to be zero. For example, if this register is programmed with 7, only external color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

This register is physically located in the external color palette chip. Reads from this I/O location cause the PALRD/ pin to be asserted. Writes to this I/O location cause the PALWR/ pin to be asserted. The functionality of this port is determined by the external palette chip.

**EXTERNAL COLOR PALETTE  
STATE REGISTER (DACSTATE)**

*Read only at I/O Address 3C7h*



**1-0** Status bits indicate the I/O address of the last CPU write to the external Color Palette:

- 00 The last write was to 3C8h (write mode)
- 11 The last write was to 3C7h (read mode)

**7-2** Reserved (0)

To allow saving and restoring the state of the video subsystem, this register is required since the external color palette chip automatically increments its index register differently depending on whether the index is written at 3C7h or 3C8h.

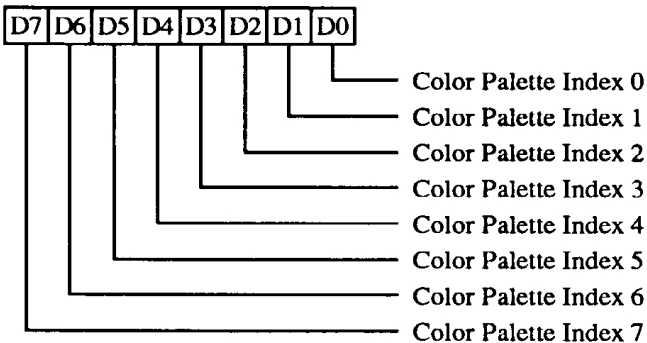
This register is physically located in the 82C457 chip, not in the color palette chip (PALRD/ is *not* asserted for reads from this I/O address).

**EXTERNAL COLOR PALETTE  
READ-MODE INDEX REGISTER (DACRX)**

*Write only at I/O Address 3C7h  
Group 6 Protection*

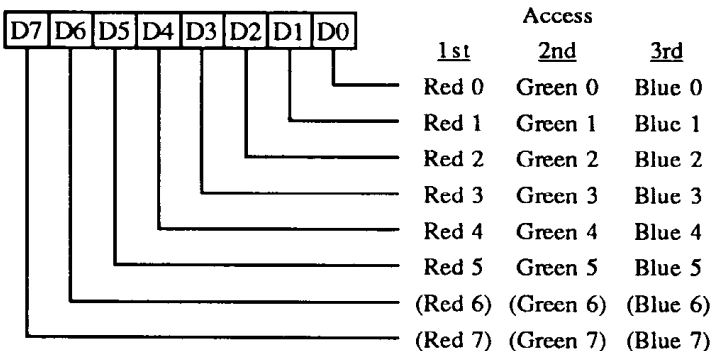
**EXTERNAL COLOR PALETTE  
INDEX REGISTER (DACX)**

*Read/Write at I/O Address 3C8h  
Group 6 Protection*



**EXTERNAL COLOR PALETTE  
DATA REGISTERS (DACDATA 00-FF)**

*Read/Write at I/O Address 3C9h  
Index 00h-FFh  
Group 6 Protection*



The color palette index and data registers are physically located in the external color palette chip (82C411). The index register is used to point to one of 256 data registers. Each data register is either 18 or 24 bits in length depending on the type of palette chip used (6 or 8 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then

repeated for the next location if desired (the index is incremented automatically by the palette chip).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register internal to the color palette chip. The save register (not the index register) is used internally by the palette chip to point at the current data register. When the index value is written to 3C7h (read mode), it is written to both the index register and the save register, then the index register is automatically incremented. When the index value is written to 3C8h (write mode), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette chip. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment the palette chip internal RGB sequence counter.

The palette chip internal data register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The 82C457 therefore saves the state of which port (3C7h or 3C8h) was last written and returns that information on reads from 3C7h (PALRD/ is only asserted on reads from 3C8h and not on reads from 3C7h). Writes to 3C7h or 3C8h cause the PALWR/ pin to be asserted.

The functionality of the index and data ports is determined by the external palette chip.

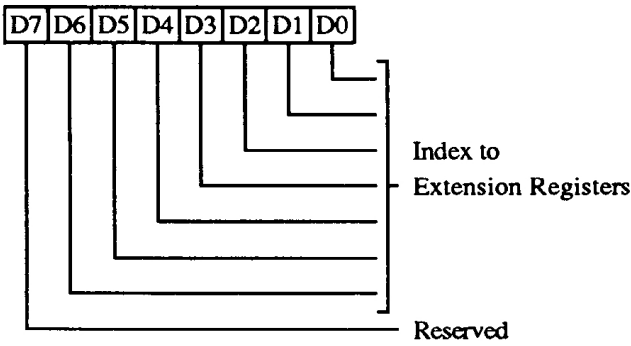
## 82C457 Extension Registers

Register Mnemonic	Register Group	Register Name	Index	I/O Access	Address	State After Reset	Page
XR00	Misc	Chip Version	00h	R	3B7h / 3D7h	0 1 1 0 r r r r	70
XR01	Misc	DIP Switch	01h	R	3B7h / 3D7h	- d d d d d d d	70
XR02	Misc	CPU Interface	02h	RW	3B7h / 3D7h	x x 0 0 0 0 0	71
XR03	Misc	ROM Decode	03h	RW	3B7h / 3D7h	- - - - - 0	71
XR04	Misc	Memory Mode	04h	RW	3B7h / 3D7h	- - - - 0 0 0	72
XR05	Misc	Sequencer Control	05h	RW	3B7h / 3D7h	- - - - 0 - -	72
XR0B	Misc	CPU Paging	0Bh	RW	3B7h / 3D7h	- - - - - 0 0	74
XR5F	Misc	Power Down Mode Refresh	5Fh	RW	3B7h / 3D7h	x x x x x x x x	89
XR60	Misc	Blink Rate Control	60h	RW	3B7h / 3D7h	1 0 0 0 0 1 1	89
XR7F	Misc	Diagnostic	7Fh	RW	3B7h / 3D7h	x x 0 0 0 0 0	93
XR08	General	General Purpose Output Select B	08h	RW	3B7h / 3D7h	- - - - - 0 0	73
XR09	General	General Purpose Output Select A	09h	RW	3B7h / 3D7h	- - - - - 0 0	73
XR0D	General	Auxiliary Offset	0Dh	RW	3B7h / 3D7h	- - - - - 0 0	75
XR28	General	Video Interface	28h	RW	3B7h / 3D7h	- - - - 0 0 1 0	81
XR2B	General	Default Video	2Bh	RW	3B7h / 3D7h	0 0 0 0 0 0 0	81
XR14	Compatibility	Emulation Mode	14h	RW	3B7h / 3D7h	0 0 0 0 x x 0 0	75
XR15	Compatibility	Write Protect	15h	RW	3B7h / 3D7h	- 0 0 0 0 0 0 0	76
XR16	Compatibility	Trap Enable	16h	RW	3B7h / 3D7h	- - 0 0 0 0 0 0	77
XR17	Compatibility	Trap Status	17h	RW	3B7h / 3D7h	- - 0 0 0 0 0 0	77
XR7E	Compatibility	CGA Color Select	7Eh	RW	3B7h / 3D7h	- - x x x x x x	92
XR18	Alternate	Alternate H Display End	18h	RW	3B7h / 3D7h	x x x x x x x x	78
XR19	Alternate	Alternate H Sync Start	19h	RW	3B7h / 3D7h	x x x x x x x x	78
XR1A	Alternate	Alternate H Sync End	1Ah	RW	3B7h / 3D7h	- - - x x x x x	79
XR1B	Alternate	Alternate H Total	1Bh	RW	3B7h / 3D7h	x x x x x x x x	79
XR1C	Alternate	Alternate H Blank Start or End	1Ch	RW	3B7h / 3D7h	x x x x x x x x	80
XR1D	Alternate	Alternate H Blank End or Start	1Dh	RW	3B7h / 3D7h	x x x x x x x x	80
XR1E	Alternate	Alternate Offset	1Eh	RW	3B7h / 3D7h	x x x x x x x x	82
XR54	Alternate	Alternate Miscellaneous Output	54h	RW	3B7h / 3D7h	x x - - 1 0 - 0	84
XR64	Alternate	Alternate Vertical Total	64h	RW	3B7h / 3D7h	x x x x x x x x	90
XR65	Alternate	Alternate Overflow	65h	RW	3B7h / 3D7h	x x x - - x x x	90
XR66	Alternate	Alternate Vertical Sync Start	66h	RW	3B7h / 3D7h	x x x x x x x x	90
XR67	Alternate	Alternate Vertical Sync End	67h	RW	3B7h / 3D7h	- - - - x x x x	90
XR68	Alternate	Alternate Vertical Display Enable End	68h	RW	3B7h / 3D7h	x x x x x x x x	91
XR50	Panel Control	Panel Format	50h	RW	3B7h / 3D7h	x 0 x x x x x x	82
XR51	Panel Control	Display Type	51h	RW	3B7h / 3D7h	0 0 x x 0 1 0 -	83
XR52	Panel Control	Panel Size	52h	RW	3B7h / 3D7h	- x x x x - x x	83
XR53	Panel Control	Line Graphics Override	53h	RW	3B7h / 3D7h	- - - - - x x	84
XR5E	Panel Control	ACDCLK Control	5Eh	RW	3B7h / 3D7h	1 x x x x x 0 0	88
XR6D	Panel Control	FRC and Palette Control	6Dh	RW	3B7h / 3D7h	0 1 0 0 0 0 1 1	92
XR6E	Panel Control	Polynomial FRC Control	6Eh	RW	3B7h / 3D7h	1 0 1 1 1 1 0 1	92
XR55	Compensation	Text Mode 350_A Compensation	55h	RW	3B7h / 3D7h	- - - 1 x x x x	85
XR56	Compensation	Text Mode 350_B Compensation	56h	RW	3B7h / 3D7h	- - - 1 x x x x	85
XR57	Compensation	Text Mode 400 Compensation	57h	RW	3B7h / 3D7h	- - - 1 x x x x	86
XR58	Compensation	Graphics Mode 350 Compensation	58h	RW	3B7h / 3D7h	- x x 0 x x x x	86
XR59	Compensation	Graphics Mode 400 Compensation	59h	RW	3B7h / 3D7h	- x x 0 x x x x	87
XR5A	Compensation	Flat Panel Vertical Display Start 400	5Ah	RW	3B7h / 3D7h	x x x x x x x x	87
XR5B	Compensation	Flat Panel Vertical Display End 400	5Bh	RW	3B7h / 3D7h	x x x x x x x x	88
XR69	Compensation	Flat Panel Vertical Display Start 350	69h	RW	3B7h / 3D7h	x x x x x x x x	91
XR6A	Compensation	Flat Panel Vertical Display End 350	6Ah	RW	3B7h / 3D7h	x x x x x x x x	91
XR6B	Compensation	Flat Panel Vertical Overflow 2	6Bh	RW	3B7h / 3D7h	x x x x x x x x	91

**Note:** These registers can be accessed only if enabled through the Extension Enable register (port 103h during setup).

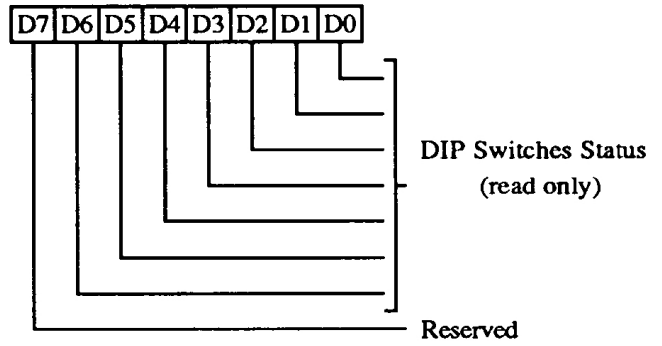
**Reset Codes:** x = Not changed by RESET (indeterminate on power-up)      - = Not implemented (always reads 0)  
d = Set from the corresponding data bus pin on falling edge of RESET      r = Chip revision # (starting from 0000)  
h = Read-only Hercules Configuration Register Readback bits      0/1 = Reset to 0/1 by falling edge of RESET

**EXTENSION REGISTER INDEX (XR0)**  
 Read/Write at I/O Address 3B6h/3D6h



- 6-0 Index value used to access the extension registers
- 7 Reserved (0)

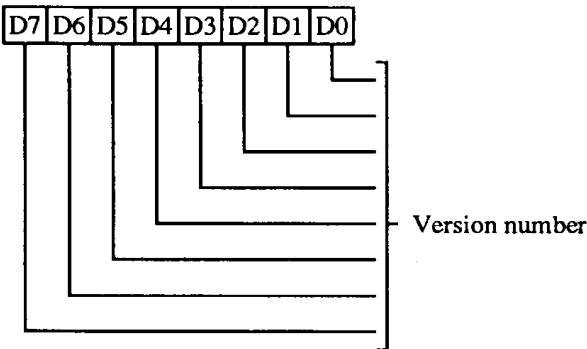
**DIP SWITCH REGISTER (XR01)**  
 Read only at I/O Address 3B7h/3D7h  
 Index 01h



- 6-0 These bits give the state of the DIP switches which are multiplexed with address/data/control signals on pins RFSH/, AEN, ADDHI, BHE/ and A18-A16.
- 7 Reserved (0)

*This register is not related to the EGA Dip Switches.*

**CHIPS VERSION REGISTER (XR00)**  
 Read only at I/O Address 3B7h/3D7h  
 Index 00h

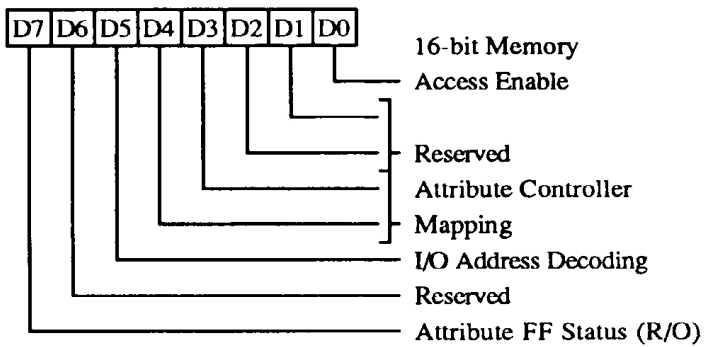


- 7-0 This register contains the version number for the 82C457. Values start at 60h and are incremented for every silicon step.

## CPU INTERFACE REGISTER (XR02)

Read/Write at I/O Address 3B7h/3D7h

Index 02h

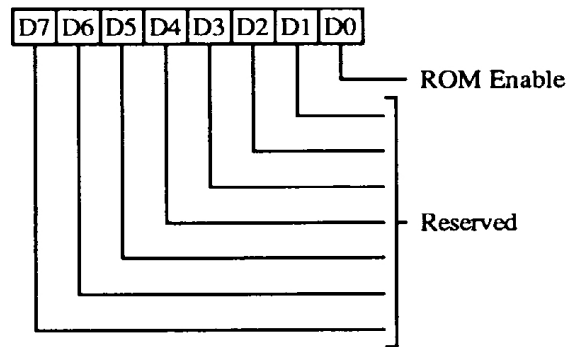


- 0** 16-bit Memory Access Enable
  - 0 Disabled
  - 1 Enabled
- 2-1** Reserved (0)
- 4-3** Attribute Controller Mapping
  - 00 Write Index at 3C0h and Data at 3C0h (8-bit access only). (Default on Reset; VGA type mapping).
  - 01 Write Index at 3C0h and Data at 3C1h (8 or 16-bit access), the attribute flip-flop is always reset in this mode (16-bit mapping).
  - 10 Write Index and Data at 3C0h/3C1h (8-bit access only EGA type mapping).
  - 11 Reserved
- 5** I/O Address Decoding. This bit affects 3B4/5h, 3D4/5h, 3C0-2h, 3C4/5h, 3CE/Fh, 3BAh, 3BFh and 3D8h.
  - 0 Decode all 16 bits of I/O address
  - 1 Decode only the lower 10 bits
- 6** Reserved (0)
- 7** Attribute Flip-flop Status (read only)
  - 0 Index
  - 1 Data

## ROM DECODE REGISTER (XR03)

Read/Write at I/O Address 3B7h/3D7h

Index 03h



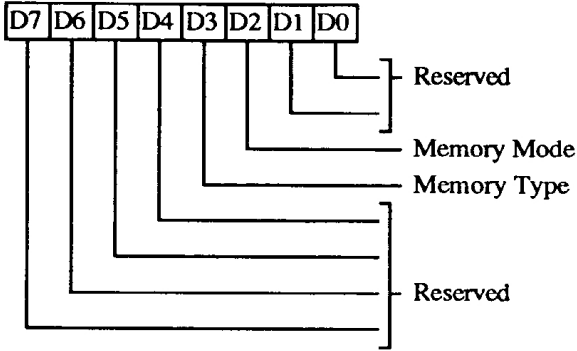
- 0** ROM Decode Enable
  - 1 ROM space decode disabled. ROMCS/ always high.
  - 0 ROM space decode enabled. ROMCS/ active (low) for CPU reads to C0000h-C7FFFh.
- 7-1** Reserved (0)



## MEMORY MODE REGISTER (XR04)

Read/Write at I/O Address 3B7h/3D7h

Index 04h



1-0 Reserved (0)

2 Memory mode

- 0 Select VGA compatible memory mode (default on reset).
- 1 Select extended "Quad Mode". In this mode, display memory is mapped to the CPU address space as 4 pages of 64 Kbytes each (or 2 pages of 128 Kbytes each). The paging is controlled through the CPU Paging register (XR0B).

3 Memory Type

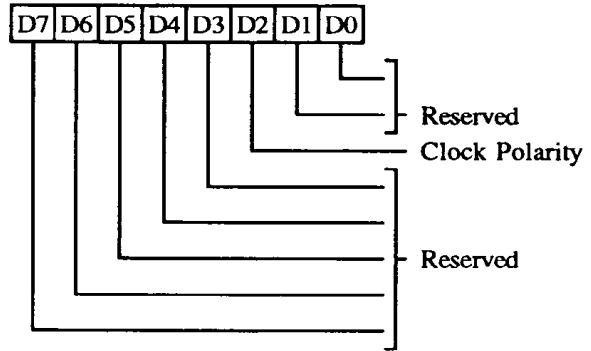
- 0 Generate DRAM timing for 64Kx4 DRAMs (4 CAS, 1 WE)
- 1 Generate DRAM timing for 64Kx16 DRAMs (4 WE, 1 CAS)

7-4 Reserved (0)

## SEQUENCER CONTROL REGISTER (XR05)

Read/Write at I/O Address 3B7h/3D7h

Index 05h



1-0 Reserved (0)

2 Clock Pin Polarity

- 0 Select one of CLK0, CLK1, or CLK2 as defined by the Miscellaneous Output or Alternate Miscellaneous Output Registers to be the display clock.
- 1 Redefine CLK0 as a common clock input and make CLK1/S0, CLK2/S1 as select outputs. CLK1/S0 and CLK2/S1 are driven by bits 2 and 3 of the Misc. Output or Alternate Misc. Output Registers.

7-3 Reserved (0)

## General Purpose Output Select Registers

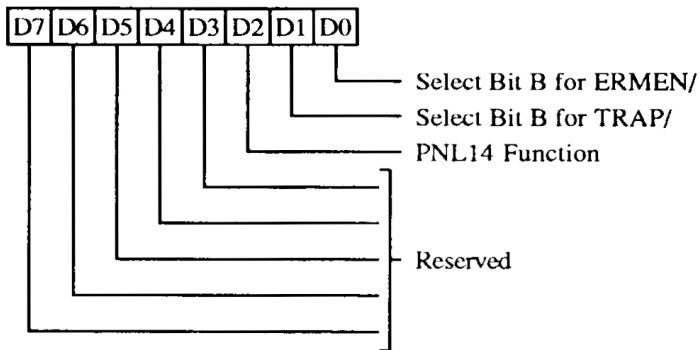
The General Purpose Output Select A and Select B registers contain 2 bits each. Together they allow the CPU to individually switch two 82C457 outputs (ERMEN and TRAP) from their normal function to a software controlled output level (3-state, low, or high).

Each pin's function is selected by 2 bits, one each in the same position in the General Purpose Output Select A Register and the General Purpose Output Select B Register.

Select Bits		Pin Function
B	A	
0	0	Normal
0	1	3-State
1	0	Force low
1	1	Force high

### GENERAL PURPOSE OUTPUT SELECT B REGISTER (XR08)

I/O Address 3B7h/3D7h  
Index 08h

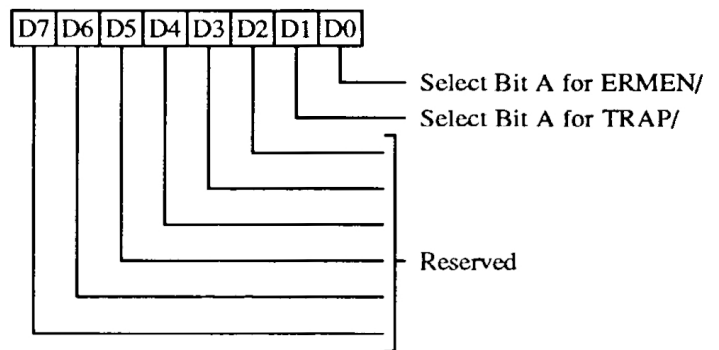


Select bit B determines if the pin should be a general purpose output or perform its normal function:

- 0** Select bit B for ERMEN/ pin
- 1** Select bit B for TRAP/ pin
- 2** PNL14 Pin Function
  - 0** PNL14 pin outputs DATEN/ (the inverse of ADREN/).
  - 1** PNL14 pin outputs panel data bit 14.
- 7-3** Reserved (0)

### GENERAL PURPOSE OUTPUT SELECT A REGISTER (XR09)

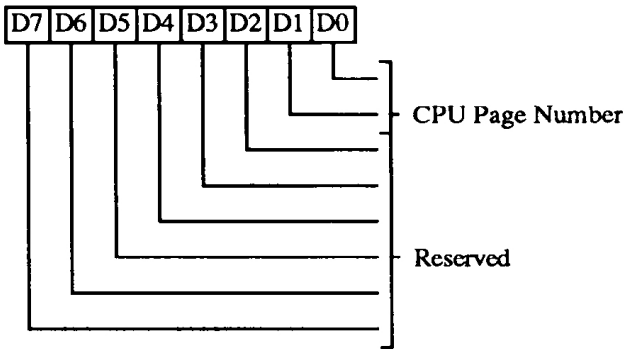
I/O Address 3B7h/3D7h  
Index 09h



If configured as a general purpose output per XR08, select bit A determines if the corresponding pin is high or low:

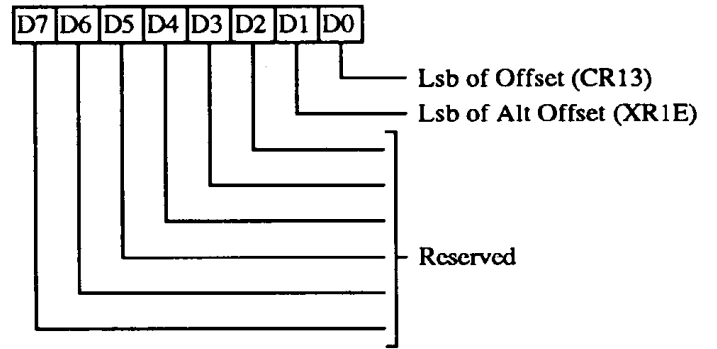
- 0** Select bit A for ERMEN/ pin
- 1** Select bit A for TRAP/ pin
- 7-2** Reserved (0)

**CPU PAGING REGISTER (XR0B)**  
 Read/Write at I/O Address 3B7h/3D7h  
 Index 0Bh



- 1-0** CPU Page Number. Display memory page number for CPU accesses in Quad mode with extended memory enabled.
- 7-2** Reserved (0)

**AUXILIARY OFFSET REGISTER (XR0D)**  
 Read/Write at I/O Address 3B7h/3D7h  
 Index 0Dh

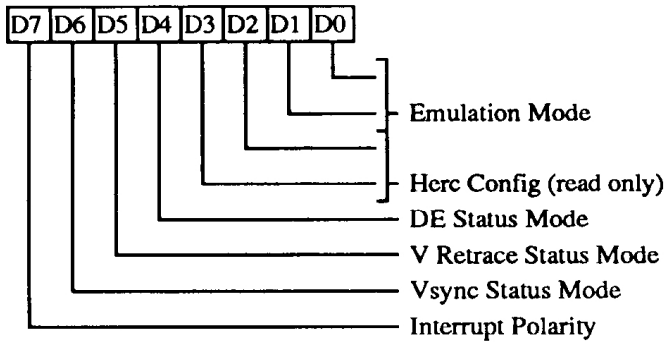


- 0** This bit provides finer granularity to the Offset when the word and double word modes are used. This bit is used with the regular Offset register (CR13).
- 1** This bit provides finer granularity to the Offset when the word and double word modes are used. This bit is used with the alternate Offset register (XR1E).
- 7-2** Reserved (0)

## EMULATION MODE REGISTER (XR14)

Read/Write at I/O Address 3B7h/3D7h

Index 14h



### 1-0 Emulation Mode

- 00 VGA / EGA
- 01 CGA
- 10 MDA
- 11 Hercules

### 3-2 Hercules Configuration Register Readback at 3BFh, bits 0&1(read only).

### 4 Display Enable Status Mode

- 0 Select Display Enable status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes).
- 1 Select Hsync status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes).

### 5 Vertical Retrace Status Mode

- 0 Select Vertical Retrace status to appear at bit 3 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes).
- 1 Select Video to appear at bit 3 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes).

### 6 Vsync Status Mode

- 0 Enable Vsync status to appear at bit 7 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes)
- 1 Prevent Vsync status from appearing at bit 7 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes).

### 7 Interrupt Output Function

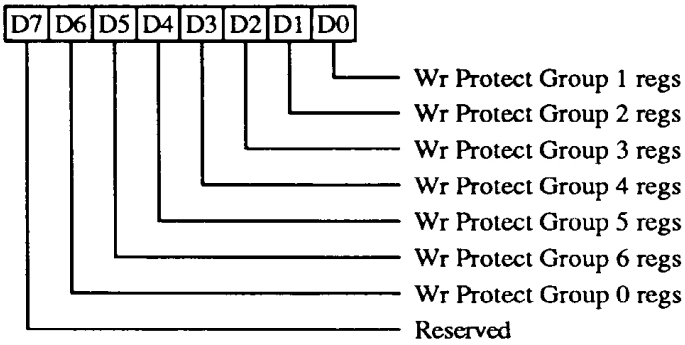
This bit controls the function of the IRQ/ output.

Interrupt State	XR14 bit-7=0	XR14 bit-7=1
Disabled	3-state	3-state
Enabled, Inactive	3-state	Low
Enabled, Active	3-state	High

## WRITE PROTECT REGISTER (XR15)

Read/Write at I/O Address 3B7h/3D7h

Index 15h



This register controls write protection for various groups of registers as shown. 0 = unprotected, 1 = protected.

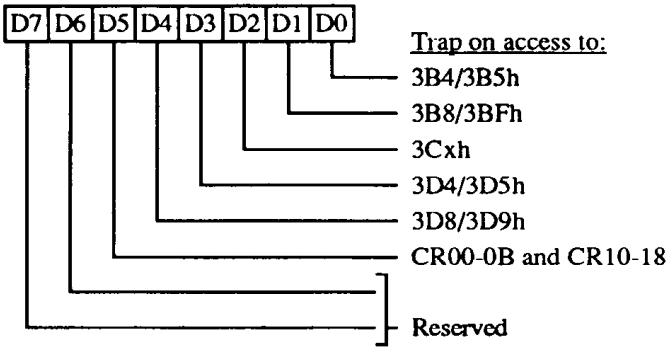
- 0** Write Protect Group 1 Registers
  - Sequencer (SR00-04)
  - Graphics Controller (GR00-08)
  - Attribute Controller (AR00-14)
- 1** Write Protect Group 2 Registers
  - Cursor Size register (CR09) bits 0-4
  - Character Height regs (CR0A, CR0B)
- 2** Write Protect Group 3 Registers
  - CRT Controller CR07 bit-4
  - CRT Controller CR08
  - CRT Controller CR11 bits 4 and 5
  - CRT Controller CR13 and CR14
  - CRT Controller CR17 bits 0,1, and 3-7
  - CRT Controller CR18
  - (Split screen, smooth scroll, & CRTC Mode)
- 3** Write Protect Group 4 Registers
  - CRT Controller CR09 bits 5-7
  - CRT Controller CR10
  - CRT Controller CR11 bits 0-3 & 6-7
  - CRT Controller CR12, CR15, CR16
  - CRT Controller CR17 bit-2
- 4** Write Protect Group 5 Registers
  - Miscellaneous Output (3C2h)
  - Feature Control (3BA/3DAh)

- 5** Write Protect Group 6 Registers. The PALRD/ and PALWR/ output signals are disabled and the 82C457 DAC state register is write protected. (I/O Addresses 3C6-3C9h).
- 6** Write Protect Group 0 Registers. Auxiliary Write Protect for CRT Controller registers CR00-07 except CR07 bit-4. This bit is logically ORed with CR11 bit-7.
- 7** Reserved (0)

## TRAP ENABLE REGISTER (XR16)

Read/Write at I/O Address 3B7h/3D7h

Index 16h



### Trap Enable bits:

- 0** Generate Trap on Access to I/O Addresses 3B4h or 3B5h.
- 1** Generate Trap on Access to I/O Addresses 3B8h or 3BFh.
- 2** Generate Trap on Access to I/O Addresses 3Cxh.
- 3** Generate Trap on Access to I/O Addresses 3D4h or 3D5h.
- 4** Generate Trap on Access to I/O Addresses 3D8h or 3D9h.
- 5** Generate Trap on Access to registers CR00 through CR0B and CR10 through CR18.
- 7-6** Reserved (0)

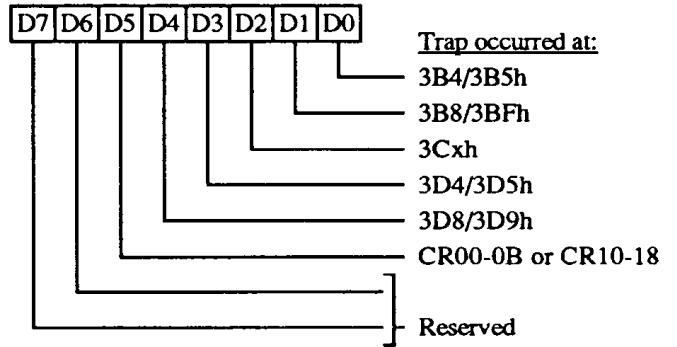
#### For all bits:

- 0 Disable trap
- 1 Enable trap

## TRAP STATUS REGISTER (XR17)

Read/Clear at I/O Address 3B7h/3D7h

Index 17h



### Trap Status bits:

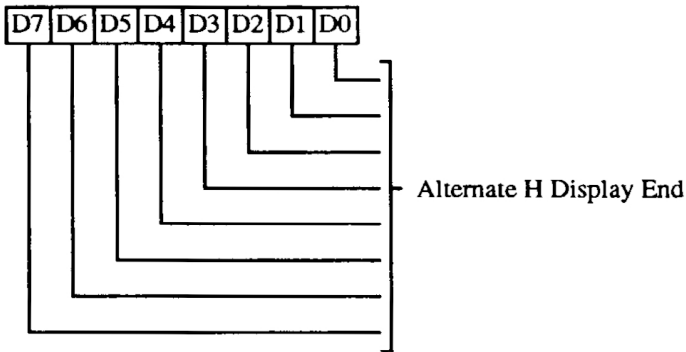
- 0** Trap occurred on access to I/O Address 3B4h or 3B5h.
- 1** Trap occurred on access to I/O Address 3B8h or 3BFh.
- 2** Trap occurred on access to I/O Address 3Cxh.
- 3** Trap occurred on access to I/O Address 3D4h or 3D5h.
- 4** Trap occurred on access to I/O Address 3D8h or 3D9h.
- 5** Trap occurred on access to CRT Controller registers CR00 through CR0B and CR10 through CR18.
- 7-6** Reserved (0)

#### For all bits:

- 0 No access occurred
- 1 Access occurred

Any or all bits in this register may be cleared by writing a one (1) to the desired bit location.

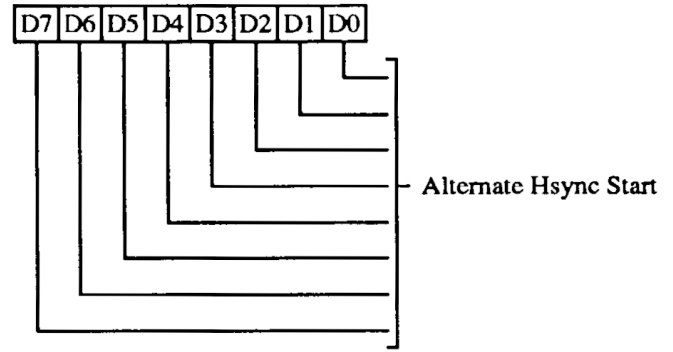
**ALTERNATE HORIZONTAL  
DISPLAY ENABLE END (XR18)**  
*Read/Write at I/O Address 3B7h/3D7h*  
*Index 18h*



This register is used in CRT low resolution CGA text and graphics modes, Hercules graphics and all flat panel modes.

- 7-0** Alternate Horizontal Display Enable End. See CR01 for description.

**ALTERNATE HORIZONTAL  
SYNC START (XR19)**  
*Read/Write at I/O Address 3B7h/3D7h*  
*Index 19h*

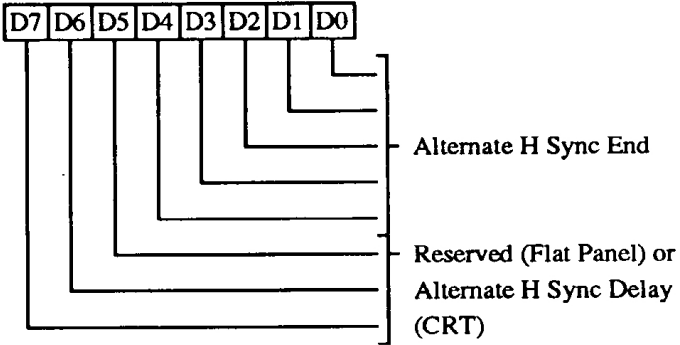


This register is used in CRT low resolution CGA text and graphics modes, Hercules graphics and all flat panel modes.

- 7-0** Alternate Horizontal Sync Start. See CR04 for description.

**ALTERNATE HORIZONTAL  
SYNC END (XR1A)**

*Read/Write at I/O Address 3B7h/3D7h  
Index 1Ah*

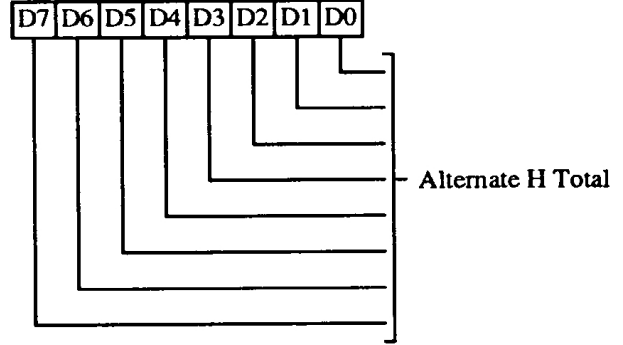


This register is used in CRT low resolution CGA text and graphics modes, Hercules graphics and all flat panel modes.

- 4-0** Alternate Horizontal Sync End. See CR05 for description.
- 7-5** For CRT: Alternate Horizontal Sync Delay. See CR05 for description.  
For Flat Panel: Reserved (0).

**ALTERNATE HORIZONTAL TOTAL  
(XR1B)**

*Read/Write at I/O Address 3B7h/3D7h  
Index 1Bh*

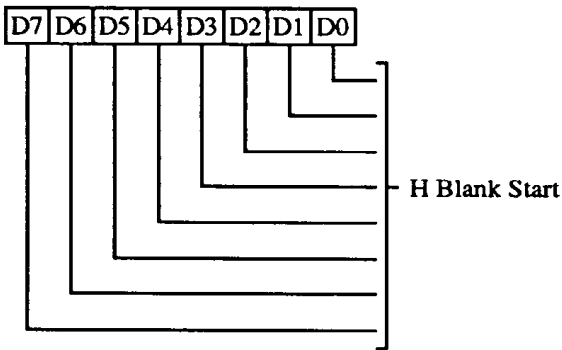


This register is used in CRT low resolution CGA text and graphics modes, Hercules graphics and all flat panel modes.

- 7-0** Alternate Horizontal Total. See CR00 for description.



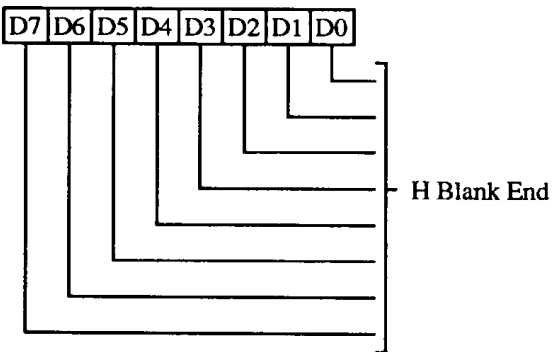
**ALTERNATE HORIZONTAL  
BLANK START (XR1C) [CRT]**  
Read/Write at I/O Address 3B7h/3D7h  
Index 1Ch



This register is used in CRT low resolution CGA text and graphics modes and Hercules graphics modes.

- 7-0 Alternate Horizontal Blank Start. See CR02 for description.

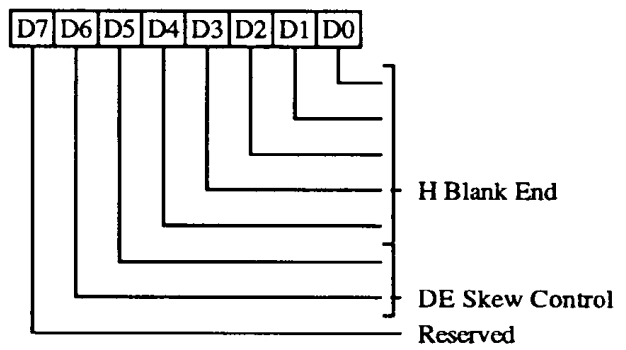
**ALTERNATE HORIZONTAL  
BLANK END (XR1C) [Flat Panel]**  
Read/Write at I/O Address 3B7h/3D7h  
Index 1Ch



This register is used in all flat panel modes.

- 7-0 These bits specify the end of horizontal blank in terms of character clocks. The period between Vertical Blank End and the Horizontal Total is the left side border on screen.

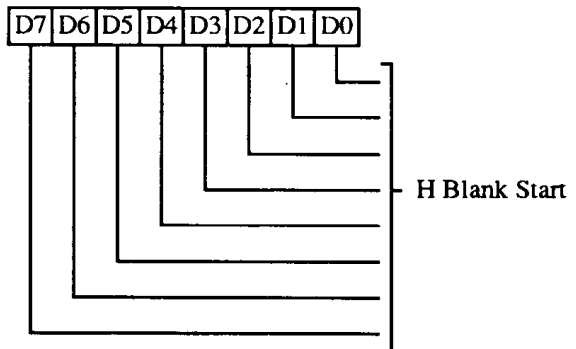
**ALTERNATE HORIZONTAL  
BLANK END (XR1D) [CRT]**  
Read/Write at I/O Address 3B7h/3D7h  
Index 1Dh



This register is used in CRT low resolution CGA text and graphics modes and Hercules graphics modes.

- 4-0 Alternate Horizontal Blank End. See CR03 for description.
- 5-6 Display Enable Skew Control. See CR03 for description.
- 7 Reserved (0)

**ALTERNATE HORIZONTAL  
BLANK START (XR1D) [Flat Panel]**  
Read/Write at I/O Address 3B7h/3D7h  
Index 1Dh



This register is used in all flat panel modes.

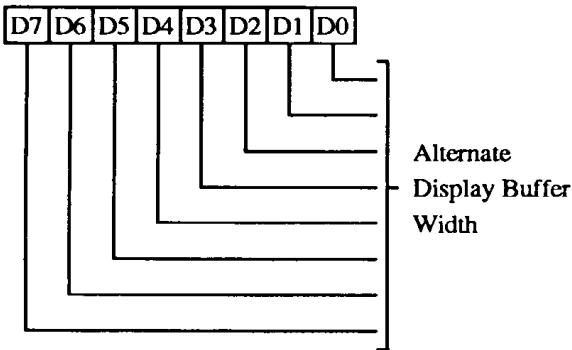
- 7-0 Alternate Horizontal Blank Start. See CR02 for description.

**Note:** The function of XR1C and XR1D change from CRT to Flat Panel modes. A separate description is provided for each mode.

### ALTERNATE OFFSET (XR1E)

Read/Write at I/O Address 3B7h/3D7h

Index 1Eh



This register is used in low resolution CGA text and graphics modes and Hercules graphics modes on both CRTs and Flat Panels.

**7-0** Alternate Offset. See CR13 for description.

### 2 Shut off Video

0 Video not forced to Default Video (XR2B) during blanking interval.

1 Video forced to default video during blanking interval.

### 3 Shut Off Blank

0 The BLANK/ output is not forced to be active during the blanking interval.

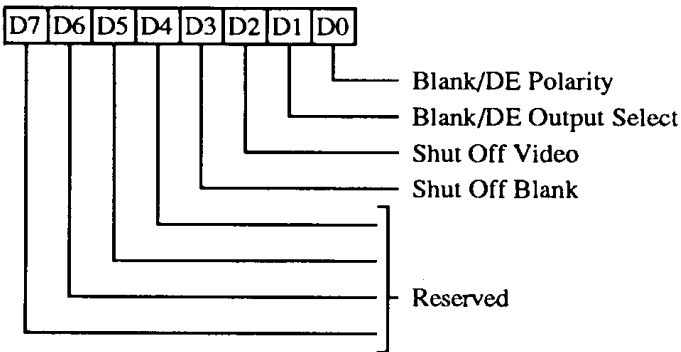
1 The BLANK/ output is forced active during the blanking interval.

**7-4** Reserved (0)

### VIDEO INTERFACE REGISTER (XR28)

Read/Write at I/O Address 3B7h/3D7h

Index 28h



### 0 BLANK/Display Enable Polarity

- 0 Negative
- 1 Positive

### 1 Blank / Display Enable Select (CRT)

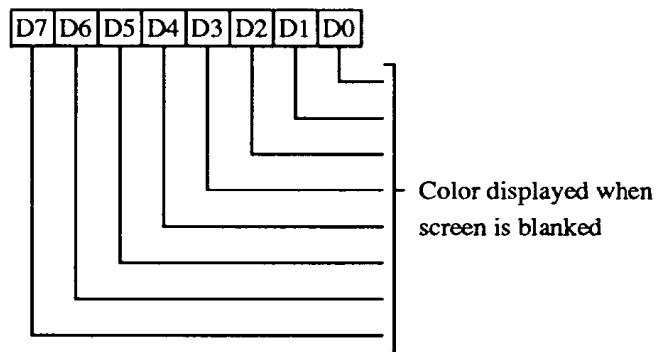
- 0 BLANK/ pin outputs DE
- 1 BLANK/ pin outputs BLANK/

The signal polarity selected by bit 0 is applicable for all functions of this pin. On Flat Panels the BLANK/ pin always outputs Display Enable.

### DEFAULT VIDEO REGISTER (XR2B)

Read/Write at I/O Address 3B7h/3D7h

Index 2Bh

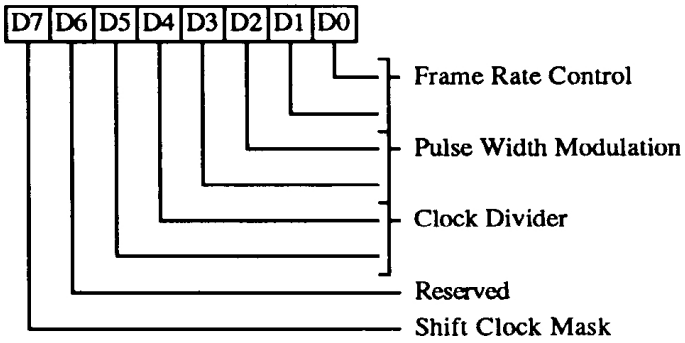


**7-0** This register is effective only on CRT displays. These bits specify the palette value to be displayed during blank time.

## PANEL FORMAT REGISTER (XR50)

Read/Write at I/O Address 3B7h/3D7h

Index 50h



This register is effective only in flat panel mode as defined in bits 2-3 of XR51.

**1-0 Frame Rate Control (FRC).** These bits specify the number of shades per color simulated by the 82C457 on a frame by frame basis. This technique is used on flat panels that do not support multiple shades internally, such as LCD panels.

- 00 No levels simulated. (8 colors are displayed.)
- 01 4 levels simulated for each color output. (64 colors are simulated.)
- 10 16 levels simulated for each color output. (4096 colors are simulated.)
- 11 3 levels simulated for each color output. (27 colors are simulated.)

**3-2 Pulse Width Modulation (PWM).** This technique is used on flat panels that support multiple colors internally.

- 00 No internal levels
- 01 4 levels are supported by the panel for each color. (64 colors are supported.)
- 10 16 levels are supported by the panel for each color. (4096 colors are supported.)
- 11 8 levels are supported by the panel for each color. (512 colors are supported.)

**5-4 Clock Divide (CD).** These bits specify the frequency ratio between the dot clock (CLK0, CLK1, CLK2 or CLKIN) and the SHFCLK signal.

- 00 Shift clock frequency = dot clock frequency. This setting is used to output one pixel per clock with flat panel displays.
- 01 Shift clock frequency = dot clock frequency/2. This setting is used to output two pixels per clock with flat panel displays.
- 10 Shift clock frequency = dot clock frequency/4. This setting is used to output four pixels per clock with flat panel displays.
- 11 Reserved

**6 Reserved (0).**

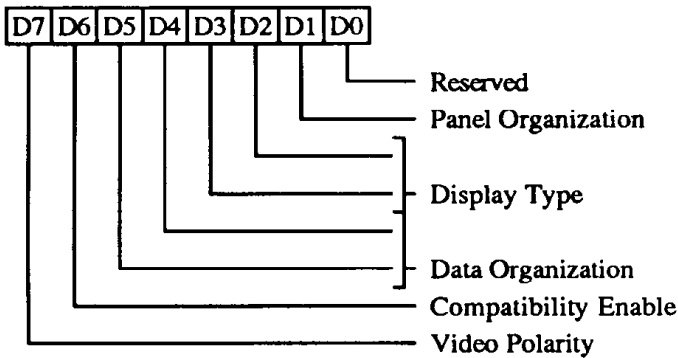
**7 Shift Clock Mask (SM).**

- 0 Enable the SHIFT CLOCK to toggle outside the Display Enable interval.
- 1 Cause the Shift Clock to stop (low) outside the Display Enable interval.

## DISPLAY TYPE REGISTER (XR51)

Read/Write at I/O Address 3B7h/3D7h

Index 51h

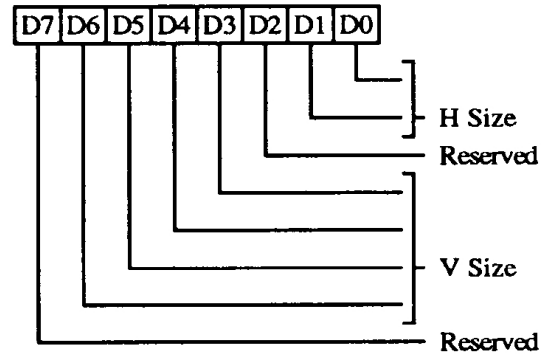


- 0** Reserved (0)
- 1** Panel Organization
  - 0 Single Panel
  - 1 Dual Panel
- 3-2** Display Type
  - 00 LCD
  - 01 CRT (default on reset)
  - 10 Plasma, EL
  - 11 Reserved
- 5-4** Data Organization
  - 00 3-bit data
  - 01 4-bit data pack
  - 10 Reserved
  - 11 Extended 4-bit pack
- 6** Compatibility Mode Enable (CMEN). When compatibility mode is enabled, the display is adjusted depending on the panel size, the current display mode and the contents of the compensation registers. When compatibility mode is disabled, the display is not adjusted.
  - 0 Compatibility mode disabled
  - 1 Compatibility mode enabled
- 7** Video Output Polarity. This bit sets the polarity of the video data.

## PANEL SIZE REGISTER (XR52)

Read/Write at I/O Address 3B7h/3D7h

Index 52h



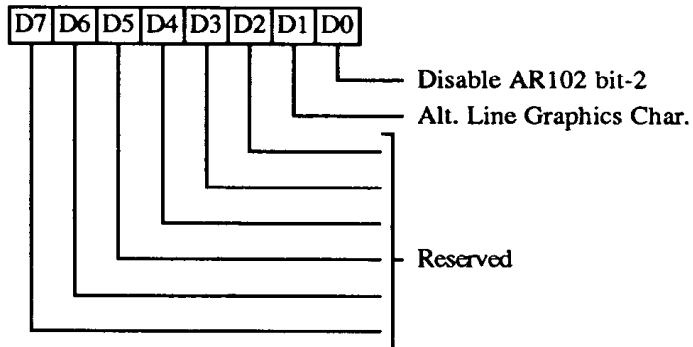
This register is effective in Flat Panel Mode only.

- 1-0** Horizontal SizeSelect
  - 00 Reserved
  - 01 640 pixels
  - 10 720 pixels
  - 11 Reserved
- 2** Reserved (0)
- 6-3** Vertical Size Select
  - 0000 Reserved
  - 0001 200 lines
  - 0010 350 lines
  - 0011 Reserved
  - 0100 400 lines
  - 0101 Reserved
  - 0110 Reserved
  - 0111 Reserved
  - 1000 480 lines
  - 1001 Reserved
  - 1010 Reserved
  - 1011 Reserved
  - 1100 Reserved
  - 1101 Reserved
  - 1110 Reserved
  - 1111 Reserved
- 7** Reserved (0)

## OVERRIDE REGISTER (XR53)

Read/Write at I/O Address 3B7h/3D7h

Index 53h



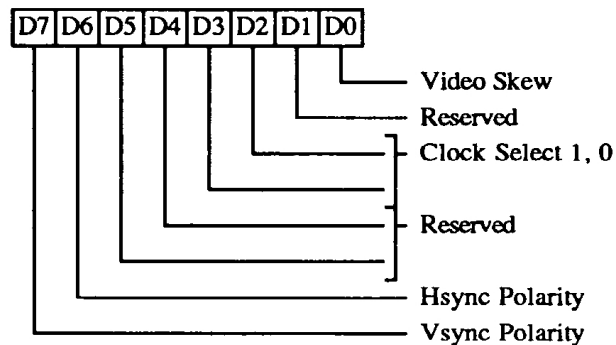
This register is used on both CRTs and flat panels only.

- 0** Disable AR10 bit-2. This bit determines if the Line Graphics Character Code Enable is defined in the Attribute Controller by bit 1 of this register. This bit is also used to force 8 or 9 pixel fonts.
  - 0** Use AR10 bit-2 for Line Graphics control
  - 1** Use bit 1 of this register for Line Graphics control
- 1** Alternate Line Graphics Character Code Control. If bit 0 of this register is 1, then this bit determines if the Line Graphics Character Codes are enabled.
  - 0** Ninth pixel of Line Graphics Character Codes is set to the back ground color
  - 1** Ninth pixel of Line Graphics Character Codes is identical to the eighth pixel.
- 7-2** Reserved (0)

## ALTERNATE MISCELLANEOUS OUTPUT REGISTER (XR54)

Read/Write at I/O Address 3B7h/3D7h

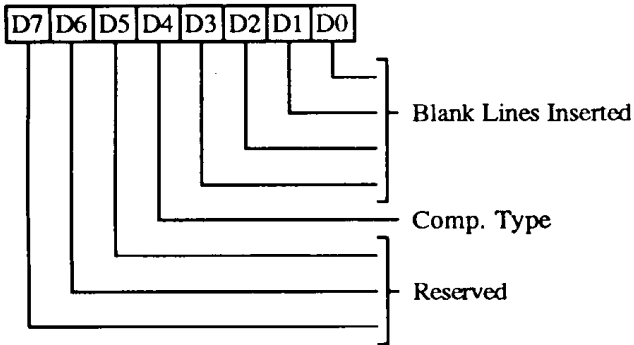
Index 54h



This register is used in Flat Panel modes.

- 0** Panel Video Skew
    - 0** No Panel Video data delay
    - 1** Video data delayed 1 clock cycle
  - 1** Reserved (0)
  - 3-2** Clock Select Bits. These bits select the flat panel dot clock source as follows:
    - 00** Select CLK0
    - 01** Select CLK1
    - 10** Select CLK2
    - 11** Reserved
  - 5-4** Reserved (0)
  - 6** Hsync Polarity (0 = pos, 1 = neg)
  - 7** Vsync Polarity (0 = pos, 1 = neg)
- (The polarity of the Blank pin is controlled through the Video Interface Register.)

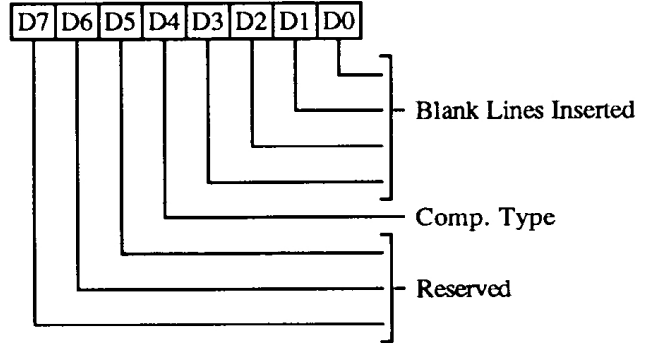
**TEXT MODE 350 A**  
**COMPENSATION REGISTER (XR55)**  
*Read/Write at I/O Address 3B7h/3D7h*  
*Index 55h*



This register is used in Flat Panel Text Modes when the vertical registers are configured for a 350 line display and the scan lines/row register (CR09) is programmed to be greater than 8 (CR09 bit-3 = 1).

- 0-3** Inserted Blank Lines (TCOMP). These bits specify the number of blank lines + 1 to insert after each row. The line inserted is set to the border color. This field is effective only when bit 4 of this register is 0.
- 4** Compensation Type (TXTC)
  - 0 Insert blank lines after each row. Graphics compensation, if enabled, is turned off
  - 1 Do not insert blank lines. Graphics compensation, if enabled, is used.
- 7-5** Reserved (0)

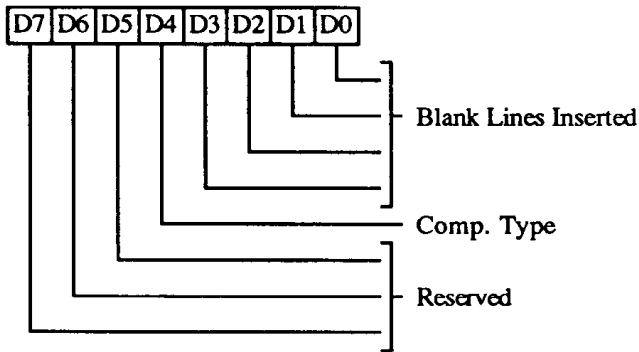
**TEXT MODE 350 B**  
**COMPENSATION REGISTER (XR56)**  
*Read/Write at I/O Address 3B7h/3D7h*  
*Index 56h*



This register is used in Flat Panel Text Modes when the vertical registers are configured for a 350 line display and the scan lines/row register (CR09) is programmed to be less than or equal to 8 (CR09 bit-3 = 0).

- 0-3** Inserted Blank Lines (TCOMP). These bits specify the number of blank lines + 1 to insert after each row. The line inserted is set to the border color. This field is effective only when bit 4 of this register is 0.
- 4** Compensation Type (TXTC)
  - 0 Insert blank lines after each row. Graphics compensation, if enabled, is turned off
  - 1 Do not insert blank lines. Graphics compensation, if enabled, is used.
- 7-5** Reserved (0)

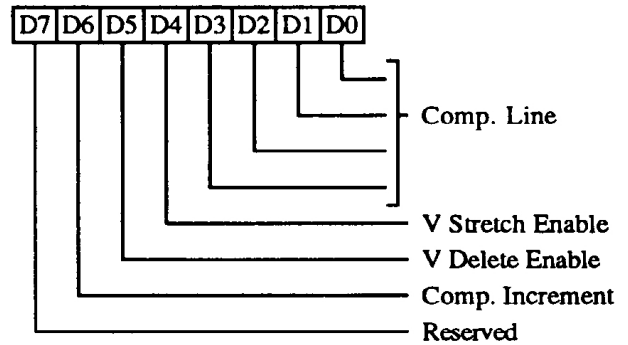
**TEXT MODE 400**  
**COMPENSATION REGISTER (XR57)**  
 Read/Write at I/O Address 3B7h/3D7h  
 Index 57h



This register is used in Flat Panel Text Mode when the vertical registers are configured for 200 or 400 line displays.

- 3-0** Inserted Blank Lines (TCOMP). These bits specify the number of blank lines + 1 to insert after each row. The line inserted is set to the border color. This field is effective only when bit 4 of this register is 0.
- 4** Compensation Type (TXTC).
  - 0 Insert blank lines after each row. Graphics compensation, if enabled, is turned off
  - 1 Do not insert blank lines. Graphics compensation, if enabled, is used.
- 7-5** Reserved (0)

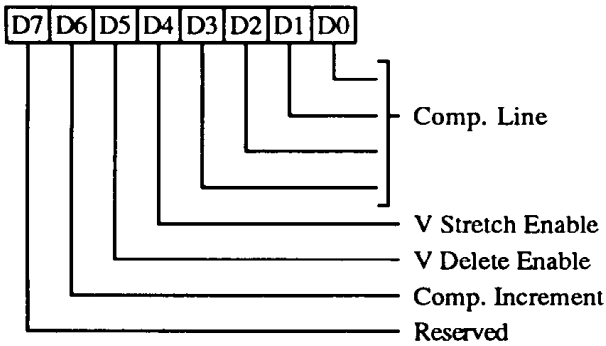
**GRAPHICS MODE 350**  
**COMPENSATION REGISTER (XR58)**  
 Read/Write at I/O Address 3B7h/3D7h  
 Index 58h



This register is used in Flat Panel 350 line modes. This feature is used for text modes when text compensation is disabled and in graphics modes.

- 3-0** Compensation Line (COMPL). These bits specify the number of displayed scan lines after which a scan line is replicated or skipped. When double scanning is enabled, one absolute scan line is actually two display scan lines.
- 4** Vertical Stretch Enable (STR)
  - 0 No scan line is replicated
  - 1 A scan line is periodically replicated as specified by bits 0-3.
- 5** Vertical Delete Enable (DEL)
  - 0 No scan line is deleted
  - 1 A scan line is periodically deleted (skipped) as specified by bits 0-3. These bits are effective only when double scanning is enabled. This ensures that there is no loss of information because only the second scan line is deleted.
- 6** Compensation Increment (COM+)
  - 0 The COMPL field (bits 0-3) is used as programmed
  - 1 Increment the COMPL field every other period
- 7** Reserved (0)

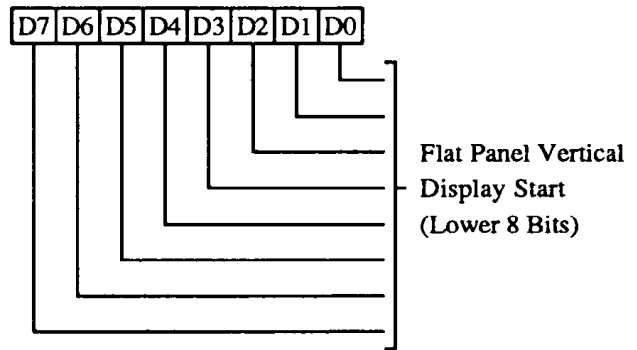
**GRAPHICS MODE 400  
COMPENSATION REGISTER (XR59)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 59h



This register is used in Flat Panel 400 line modes. This register is also used for 200 line modes. This feature is used for text modes when text compensation is disabled and graphics modes.

- 3-0 Compensation Line (COMPL).** These bits specify the number of displayed (not absolute) scan lines after which a scan line is replicated or skipped. When double scanning is enabled, one absolute scan line is actually two display scan lines.
- 4 Vertical Stretch Enable (STR)**
  - 0 No scan line is replicated.
  - 1 A scan line is periodically replicated as specified by bits 0-3.
- 5 Vertical Delete Enable (DEL)**
  - 0 No scan line is deleted
  - 1 A scan line is periodically deleted (skipped) as specified by bits 0-3. These bits are effective only when double scanning is enabled. This ensures that there is no loss of information because only the second scan line is deleted.
- 6 Compensation Increment (COM+)**
  - 0 The COMPL field (bits 0-3) is used as programmed
  - 1 Increment the COMPL field every other period
- 7 Reserved (0)**

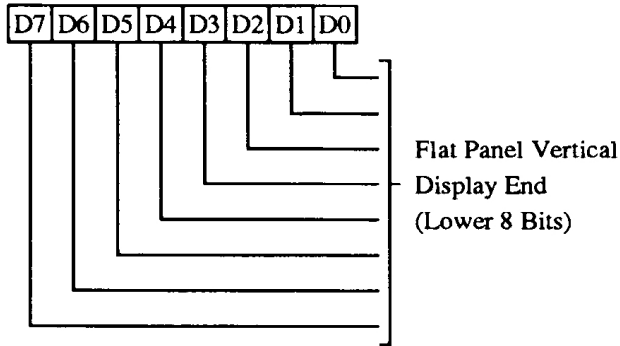
**FLAT PANEL VERTICAL  
DISPLAY START 400 (XR5A)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 5Ah



- 7-0** These bits are used in 400-line flat panel modes. They specify the lower 8-bits of the vertical start address for Display Enable (in scan lines). The higher 2 bits are in the Flat Panel Vertical Overflow 2 register. To set the display start at the first scan line program this register with a value equal to the vertical total (XR64) + 1.

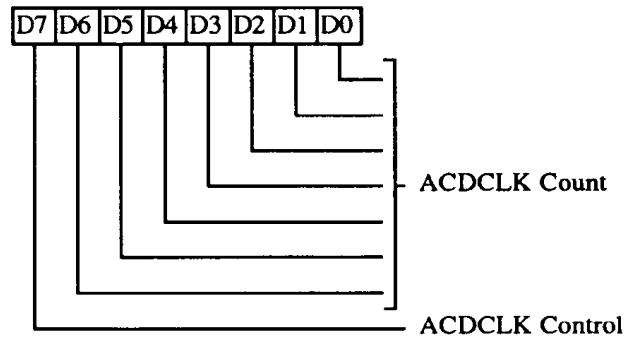


**FLAT PANEL VERTICAL  
DISPLAY END 400 (XR5B)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 5Bh



**7-0** These bits are used in 400-line flat panel modes. They specify the lower 8-bits of the vertical end address for Display Enable (in scan lines). The high order 2 bits are in the Flat Panel Vertical Overflow 2 register. The correct value for this register is the start value + number of displayed lines (including inserted or replicated lines). Failure to correctly program this register will result in missing or extra lines at the bottom of the display.

**ACDCLK CONTROL REGISTER (XR5E)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 5Eh



**6-0** ACDCLK Count. These bits define the number of Hsync or Vsyncs between adjacent phase changes (Toggles) of the ACDCLK output. The function of this field varies depending on the value of bit-7 of this register.

If bit-7=0, ACDCLK is synchronized with Hsync. The number of Hsyncs between phase changes is equal to the value programmed in these bits plus two.

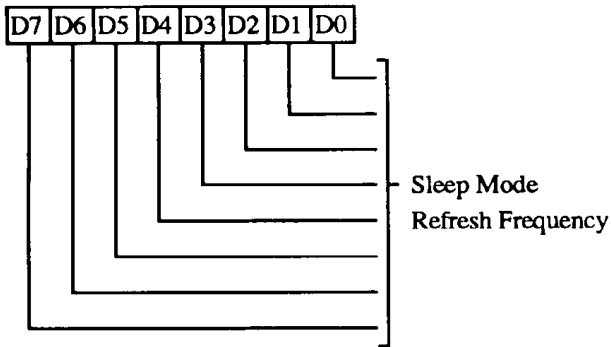
If bit-7=1, ACDCLK is synchronized with Hsync, bits 2-6 are "don't care" and bits 0-1 are defined as follows:

- 00 ACDCLK toggles every Vsync.
- 01 ACDCLK toggles every other Vsync.
- 1x ACDCLK toggles every Vsync and inverts every 16 Vsyncs.

**7** ACDCLK Control. This bit determines whether the ACDCLK is synchronized with Hsync or Vsync.

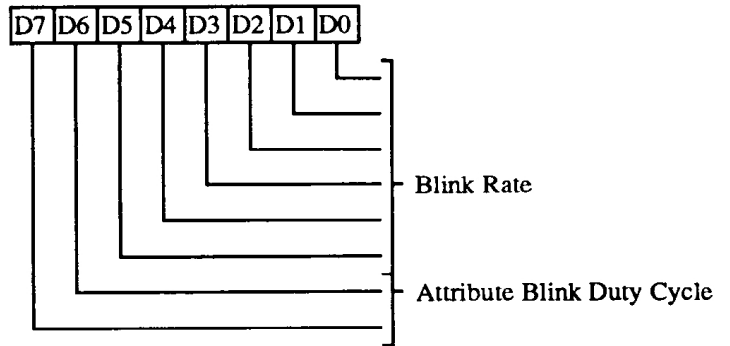
- 0 ACDCLK changes phase based on Hsync
- 1 ACDCLK changes phase based on Vsync

**POWER DOWN MODE  
REFRESH REGISTER (XR5F)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 5Fh



**7-0** These bits define the frequency of RAS-only memory refresh cycles when the PWRDN2 pin is high. The interval between two refresh cycles = Clock Period \* [ (4 \* contents of this register) + 8]. A value of 0 causes no refresh to be done. The clock selected is specified by the Clock Select bits in the Miscellaneous Output register (3C2h).

**BLINK RATE CONTROL (XR60)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 60h



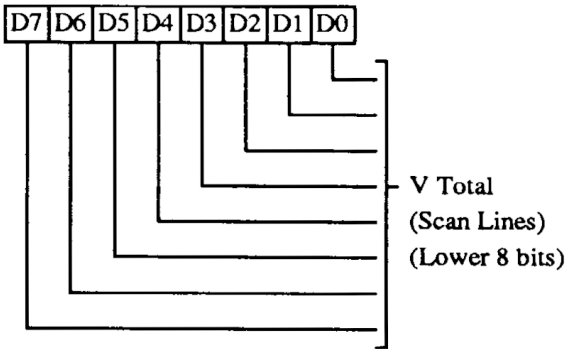
This register is used in all text modes. The graphics blink rate is fixed at 32 Vsyncs.

**5-0** Blink Rate. These bits specify the number of VSYNC periods during which the cursor will be on and off (50% duty cycle). A character and pixel blink period will always be double the cursor blink period. The blink rate is selected as follows: Cursor Blink Frequency = VSYNC Frequency [2 \* (contents of this register+1)].

**7-6** Attribute Blink Duty Cycle. The cursor blink duty cycle is fixed at 50%. The character and pixel blink duty cycle is dependent on these bits as follows (default is 50% on reset):

Bit-7	Bit-6	Attribute Blink Duty Cycle
0	0	Reserved
0	1	25%
1	0	50%
1	1	75%

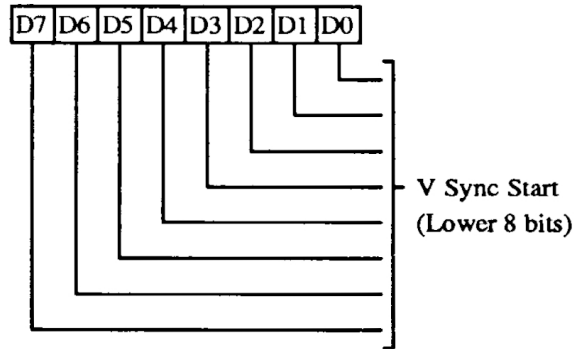
**ALTERNATE  
VERTICAL TOTAL (XR64)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 64h



This register is used in flat panel modes.

- 7-0 Alternate Vertical Total. See CR06 for description.

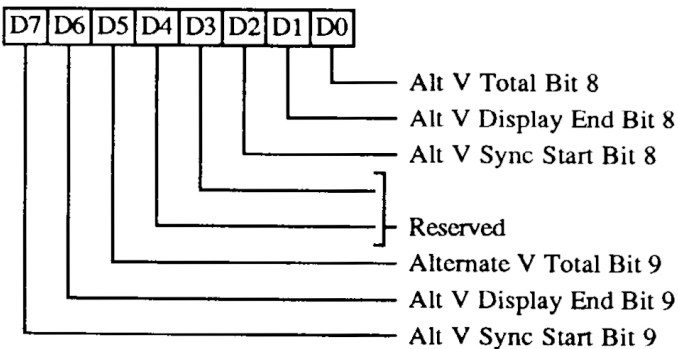
**ALTERNATE  
VERTICAL SYNC START (XR66)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 66h



This register is used in flat panel modes.

- 7-0 Alternate Vsync Start. See CR10 for description.

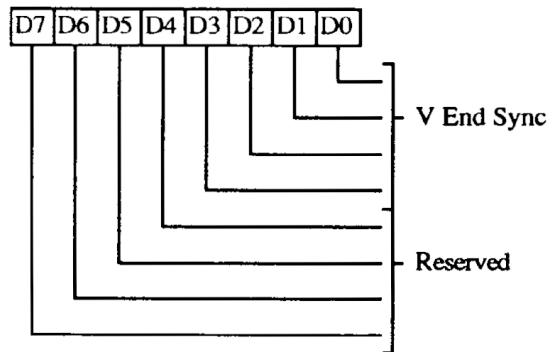
**ALTERNATE OVERFLOW (XR65)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 65h



This register is used in flat panel modes.

- 0 Alternate Vertical Total Bit 8
- 1 Alternate Vertical Display End Bit 8
- 2 Alternate Vertical Sync Start Bit 8
- 3 Reserved (0)
- 4 Reserved (0)
- 5 Alternate Vertical Total Bit 9
- 6 Alternate Vertical Display End Bit 9
- 7 Alternate Vertical Sync Start Bit 9

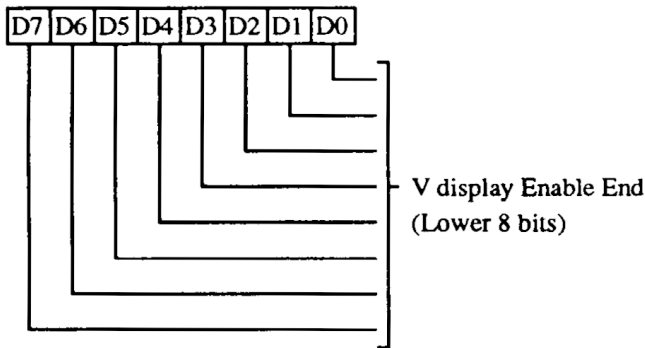
**ALTERNATE  
VERTICAL SYNC END (XR67)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 67h



This register is used in flat panel modes.

- 3-0 Alternate Vsync End. See CR11 for description.
- 7-4 Reserved (0)

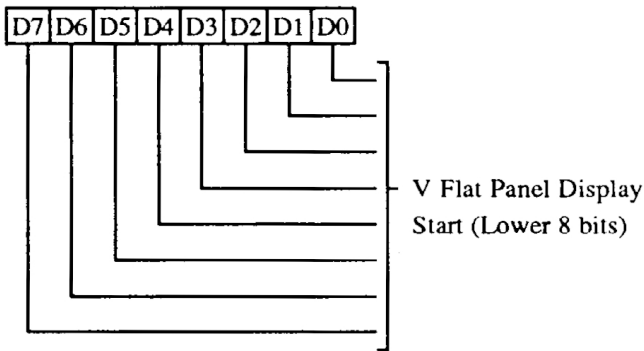
**ALTERNATE  
VERTICAL DISPLAY ENABLE (XR68)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 68h



This register is used in flat panel modes. It is used to determine the size of the flat panel.

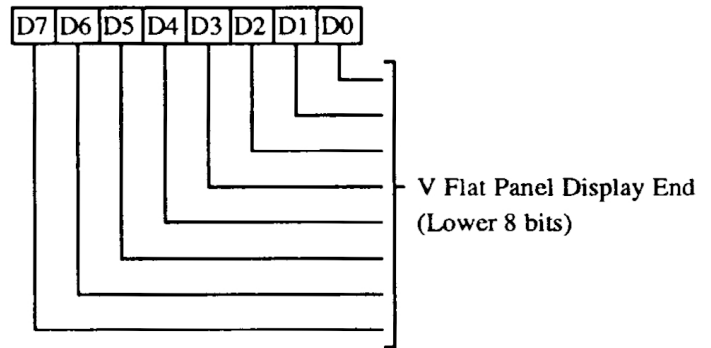
- 7-0** Alternate Vertical Display Enable End. See CR12 for description.

**FLAT PANEL  
VERTICAL DISPLAY START 350 (XR69)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 69h



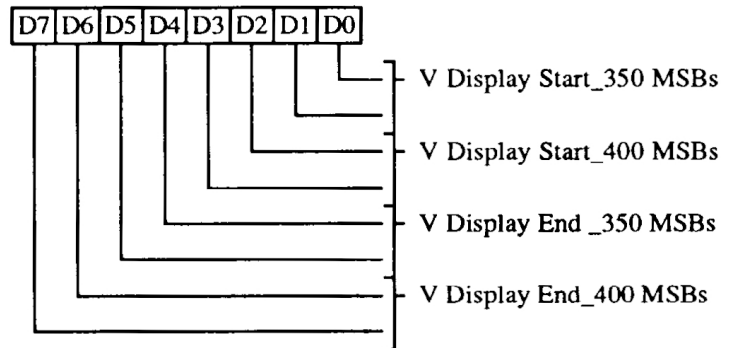
- 7-0** These bits are used only in 350-line flat panel modes. They specify the lower 8-bits of the vertical start address for Display Enable (in scan lines). The high order 2 bits are in the Flat Panel Vertical Overflow 2 register. To set the display start at the first scan line program this register with a value equal to the vertical total (XR64) + 1.

**FLAT PANEL  
VERTICAL DISPLAY END 350 (XR6A)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 6Ah



- 7-0** These bits are used only in 350-line flat panel modes. They specify the lower 8-bits of the vertical end address for Display Enable (in scan lines). The high order 2 bits are in the Flat Panel Vertical Overflow 2 register. The correct value for this register is the start value + number of displayed lines (including inserted or replicated lines). Failure to correctly program this register will result in missing or extra lines at the bottom of the display.

**FLAT PANEL  
VERTICAL OVERFLOW 2 (XR6B)**  
Read/Write at I/O Address 3B7h/3D7h  
Index 6Bh

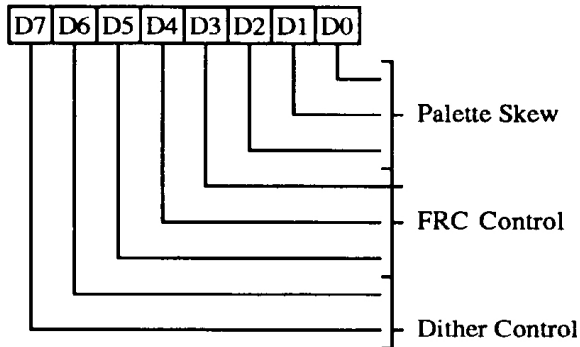


- 1-0** Bits 9 & 8 of Vertical Display Start\_350
- 3-2** Bits 9 & 8 of Vertical Display Start\_400
- 5-4** Bits 9 & 8 of Vertical Display End\_350
- 7-6** Bits 9 & 8 of Vertical Display End\_400

Bits 0-1 and 4-5 are used in 350-line Flat Panel modes only. Bits 2-3 and 6-7 are used in 400-line Flat Panel modes only.

## FRC AND PALETTE CONTROL REGISTER (XR6D)

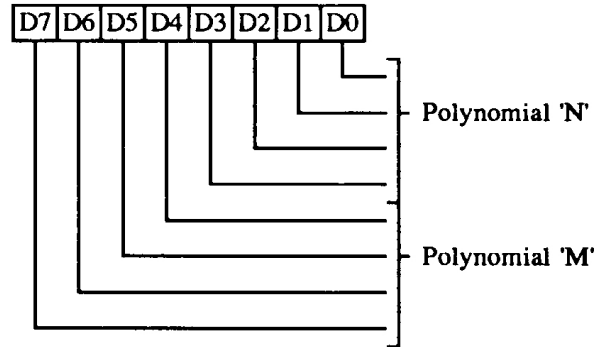
Read/Write at I/O Address 3B7h/3D7h  
Index 51h



- 2-0** External Palette Skew. These bits select the delay, in clocks, through the external flat panel palette. A value of 000 selects 1 clock delay. The 82C411 requires a value of 101.
- 3** FRC Control 0. This bit determines the FRC matrix size.
  - 0 31x15 Matrix
  - 1 32x16 Matrix
- 4** FRC Control 1. This bit determines the FRC pattern used.
  - 0 Select Pattern A
  - 1 Select Pattern B
- 5** FRC Control 2. This bit determines how the FRC counter runs.
  - 0 FRC counter is reset to new offset for each row
  - 1 FRC Counter is allowed to free run
- 7-6** Dither Control
  - 00 No dither enabled
  - 01 Dither enabled only in 256 Color modes
  - 1x Dither always enabled

## POLYNOMIAL FRC CONTROL REGISTER (XR6E)

Read/Write at I/O Address 3B7h/3D7h  
Index 6Eh



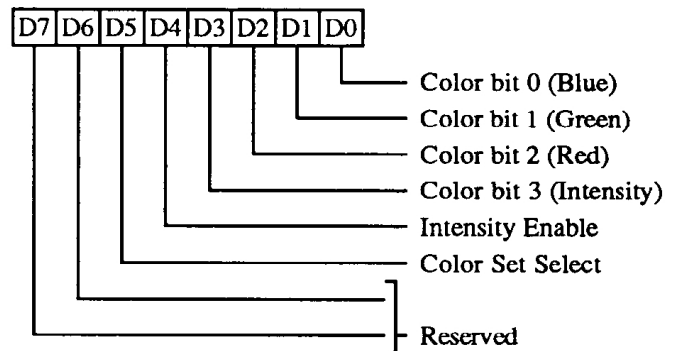
This register is used to control the FRC polynomial counters. The values in the counters determine the offset in rows and columns of the FRC count. These values are usually determined by trial and error.

**3-0** Polynomial 'N' value

**7-4** Polynomial 'M' value

## CGA COLOR SELECT (XR7E)

Read/Write at I/O Address 3B7h/3D7h  
Index 7Eh

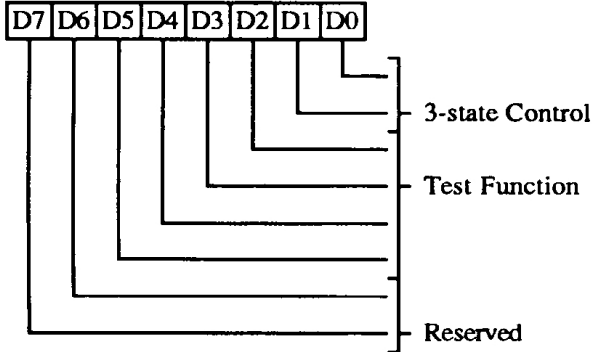


This register is a copy of the CGA color select register 3D9h. Writes to this register will change the copy at 3D9h. It is effective in CGA emulation mode. The copy at 3D9h is visible only in CGA emulation mode or when the extension registers are enabled. The copy at XR7E is always visible.

## DIAGNOSTIC (XR7F)

Read/Write at I/O Address 3B7h/3D7h

Index 7Fh



### 0 3-State Control bit 0

0 Normal Outputs

1 3-state output pins PALRD/, PALWR/, HSYNC, VSYNC, ACDCLK, BLANK/, P[7:0], RDY, ADREN/ and IRQ/.

### 1 3-state Control bit 1

0 Normal Outputs

1 3-state output pins WE/, RAS/, CAS/, CAS1/, CAS2/, CAS3/, AA0-7 and BA0-7.

5-2 Test Function Pins. These bits are used for internal testing of the chip. They should be 0 for normal operation.

7-6 Reserved (0)

# Design Considerations

This section covers a variety of topics pertinent to designing a system which contains the 82C457 and 82C411.

## CLOCK INPUTS

The 82C457 provides two configurations for selecting the clock input. In both configurations, the desired clock is selected via the Miscellaneous Output Register. The configuration is determined by the Sequencer Control Register, XR05.

The first configuration provides 3 dot clock inputs, CLK0, CLK1 and CLK2. The first two of these inputs are typically driven by 25.175 MHz and 28.322 MHz signals, respectively, ensuring VGA compatibility on a CRT monitor. The third input is usually used for a flat panel clock, however any of the three clocks may be used.

In the second configuration, two clock select signals are provided and a single clock input is used. The clock select signals are controlled by the Miscellaneous Output Register. The clock muxing is done external to the 82C457 and the desired clock is applied to the CLKIN pin. This configuration has the advantage of providing four possible clock sources and interfacing directly to most clock synthesizer chips.

The MCLK input is always required. It is used for internal sequencing of I/O cycles and is usually connected to a 28.322 MHz or greater source.

## ROM DECODE

A ROM Decode signal (ROMCS/) is provided. This signal may be used to decode memory reads to the address space C0000h-C7FFFh. The output is not valid until MEMR/ is active (low). Since the address/data transceivers are directed inward, towards the 82C457 AD-bus, a separate data buffer must be used for the ROM. The ROM decode may be disabled through the ROM Decode Control Register (XR03). In most laptop applications, the Video BIOS is merged with the system BIOS and this signal is not used.

## DATA BUFFER ENABLE

In most systems, both non-inverted and inverted copies of ADREN/ are required. In systems that do not require all 16 Panel Data signals, PNL14 may be

configured as an inverted copy of ADREN/. This feature will save an inverter in most designs. This feature is controlled by the GP I/O register (XR08).

## ENABLING THE 82C457

After being reset the 82C457 is disabled. It must be explicitly enabled by writing to I/O address 102h in Setup Mode.

Bit-3 of port 46E8h must be set to zero to disable the 82C457 and to one to enable it. When disabled, it is not visible in the CPU memory and I/O space. This port is *internal* to the 82C457. Under normal circumstances, enable the 82C457 using the following sequence:

- 1) Place the 82C457 in Setup mode by setting bit-3 at I/O address 46E8h to 1.
- 2) Set bit-1 of port 102h to 1.
- 3) Place the 82C457 in its normal operating mode by setting bit-4 at I/O address 46E8h to 0 and bit-3 to 1.

## Disconnecting the Video Subsystem

The 82C457 and the Video Subsystem can be disconnected from the CPU as follows:

### Disabling the 82C457:

This mode is entered after Reset or can be forced by the following technique.

- Write 0 to bit-3 of port 46E8h.
- Enter Retire mode (PWRDN pin high).

### Enabling the 82C457:

- Force the PWRDN2 pin low.
- Set bits 4&3 of port 46E8h to 01.

# Panel Pixel Order

The 82C457 is the most flexible color flat panel graphics controller available. It is designed to interface directly to the widest possible range of color flat panels. This section describes pixel output order and provides diagrams for various clock divides and different levels of color support.

Extension register 50 (XR50) bits 1-0 define the FRC level supported (FRC):

- 00 No FRC levels
- 01 4 level FRC supported
- 10 16 level FRC supported
- 11 3 level FRC supported

XR50 bits 3-2 define the number of shades per color the panel supports internally (PWM):

- 00 No internal shades, panel has RGB only
- 01 4 shades per color supported by the panel
- 10 16 shades per color supported by the panel
- 11 8 shades per color supported by the panel

XR50 bits 5-4 define the clock divide (CD):

- 00 Shift clock = dot clock (1 pixel / clock)
- 01 Shift clock = dot clock / 2 (2 pixel / clock)
- 10 Shift clock = dot clock / 4 (4 pixel / clock)
- 11 Reserved

XR50 bit 7 defines the shift mask (SM):

- 0 Shift clock toggles during the blank interval
- 1 Shift clock is halted during the blank interval

XR51 bit 1 defines whether the display is a single or dual panel:

- 0 Single panel display (SS)
- 1 Dual panel display (DS)

Since dual panel data is output sequentially, there is no difference between single and dual panel output order and data organization. The upper panel data is output then the lower panel data.

XR51 bits 5-4 define the data organization:

- 00 3-bit data
- 01 4-bit packed data
- 10 Reserved
- 11 Extended 4-bit packed data

Color Type	Colors	w / Dither	CD	Data Org.
None	8	125	00	3-bit
PWM-4	64	2,197	00	3-bit
PWM-8	512	24,389	00	3-bit
PWM-16	4,096	226,981	00	3-bit
PWM-4	64	2,197	01	3-bit
FRC-3	27	729	00	3-bit
FRC-4	64	2,197	00	3-bit
FRC-16	4,096	226,981	00	3-bit
FRC-3	27	729	01	3-bit
FRC-4	64	2,197	01	3-bit
FRC-16	4,096	226,981	01	3-bit
FRC-3	27	729	10	3-bit
FRC-4	64	2,197	10	3-bit
FRC-16	4,096	226,981	10	3-bit
FRC-3	27	729	00	4-bit pack
FRC-4	64	2,197	00	4-bit pack
FRC-16	4,096	226,981	00	4-bit pack
FRC-3	27	729	01	4-bit pack
FRC-4	64	2,197	01	4-bit pack
FRC-16	4,096	226,981	01	4-bit pack
FRC-3	27	729	10	4-bit pack
FRC-4	64	2,197	10	4-bit pack
FRC-16	4,096	226,981	10	4-bit pack
FRC-3	27	729	10	Ext. 4-bit pack
FRC-4	64	2,197	10	Ext. 4-bit pack
FRC-16	4,096	226,981	10	Ext. 4-bit pack

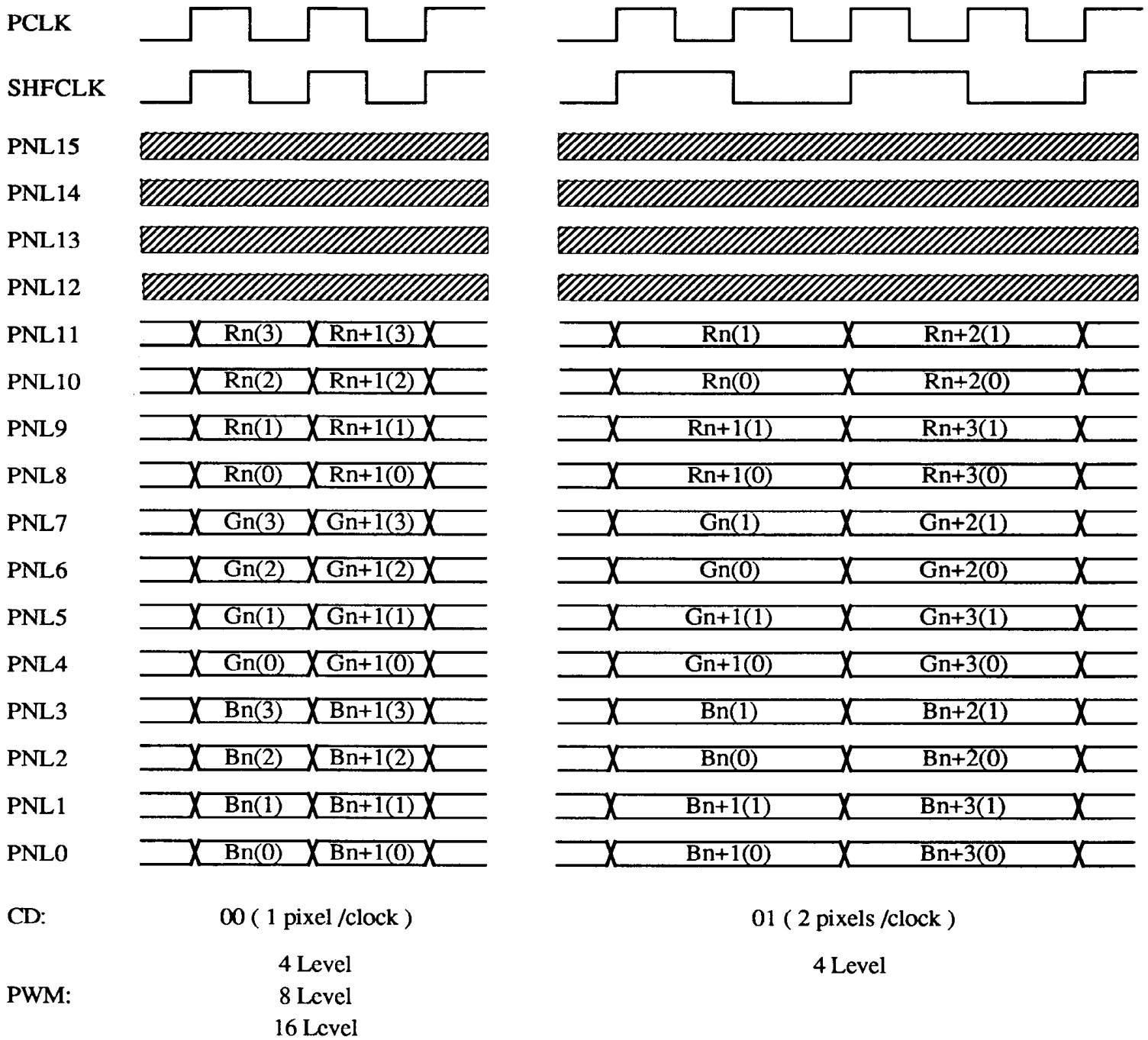
For PWM, only the 3-bit data format is supported. If both PWM and FRC are disabled, output is assumed to be "FRC" and the output order is determined by the clock divide and data format.

The following diagrams showing pixel order are included:

- 1) PWM
- 2) FRC, 3-bit
- 3) FRC, 4-bit Packed Data
- 4) FRC, Extended 4-bit Packed Data
- 5) One vs. Four pixel / clock
- 6) Single vs. Dual panel
- 7) Sync timing restrictions

PWM, FRC, all data formats and clock divides are supported for both Plasma/EL and LCD display types and for both single and dual panel displays.



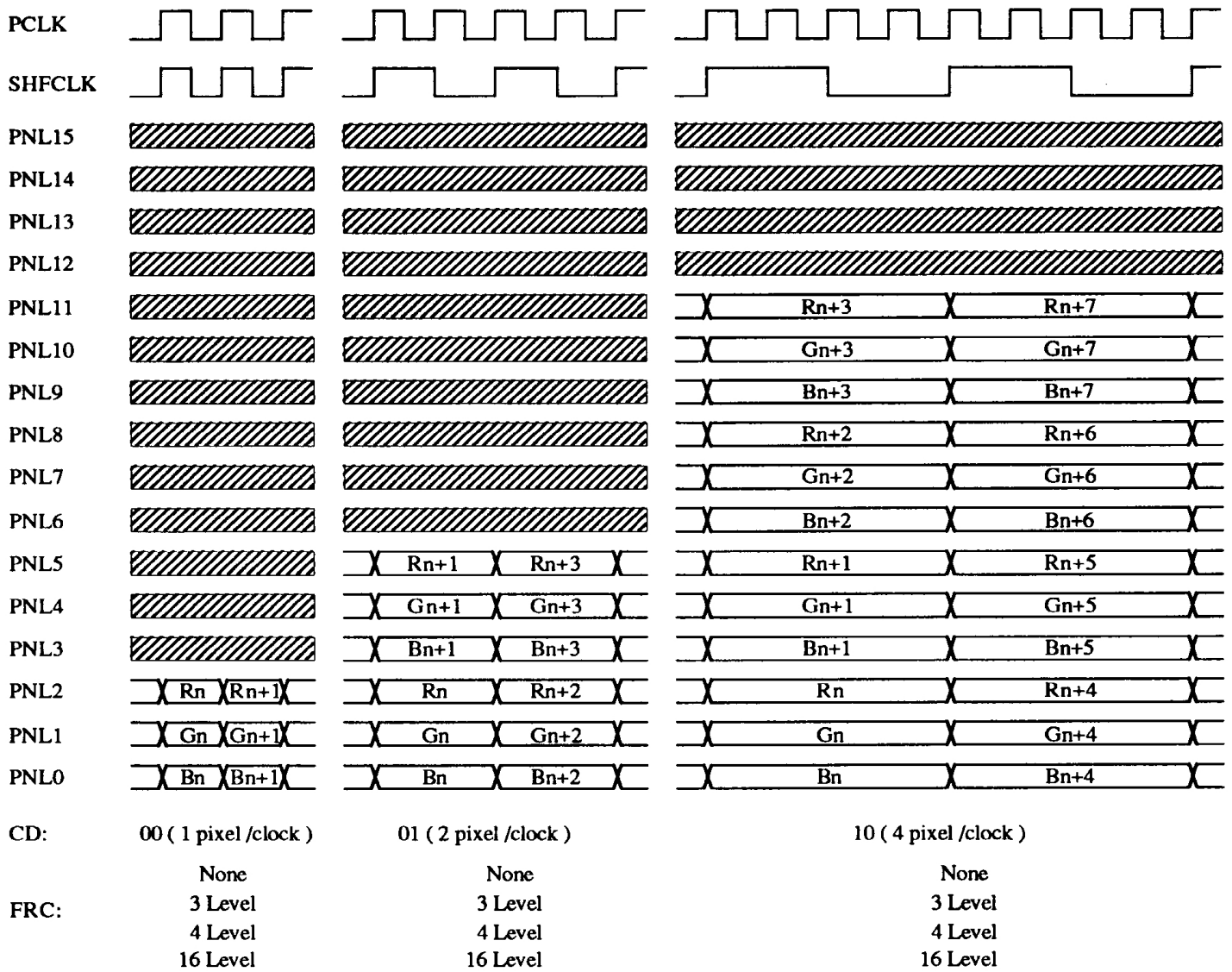


**82C457 Panel Pixel Order - PWM with Clock Divide 00 (1/1) & 01 (1/2)**

This diagram shows the pixel output order for PWM (internal color shades) with clock divides of 1 and 2. In this configuration, the panel is assumed to support up to 16 shades per color (4 shades for a clock divide of 2.) If the panel does not support the expected number of shades, the panel data inputs should be connected to the highest order bits for each color.

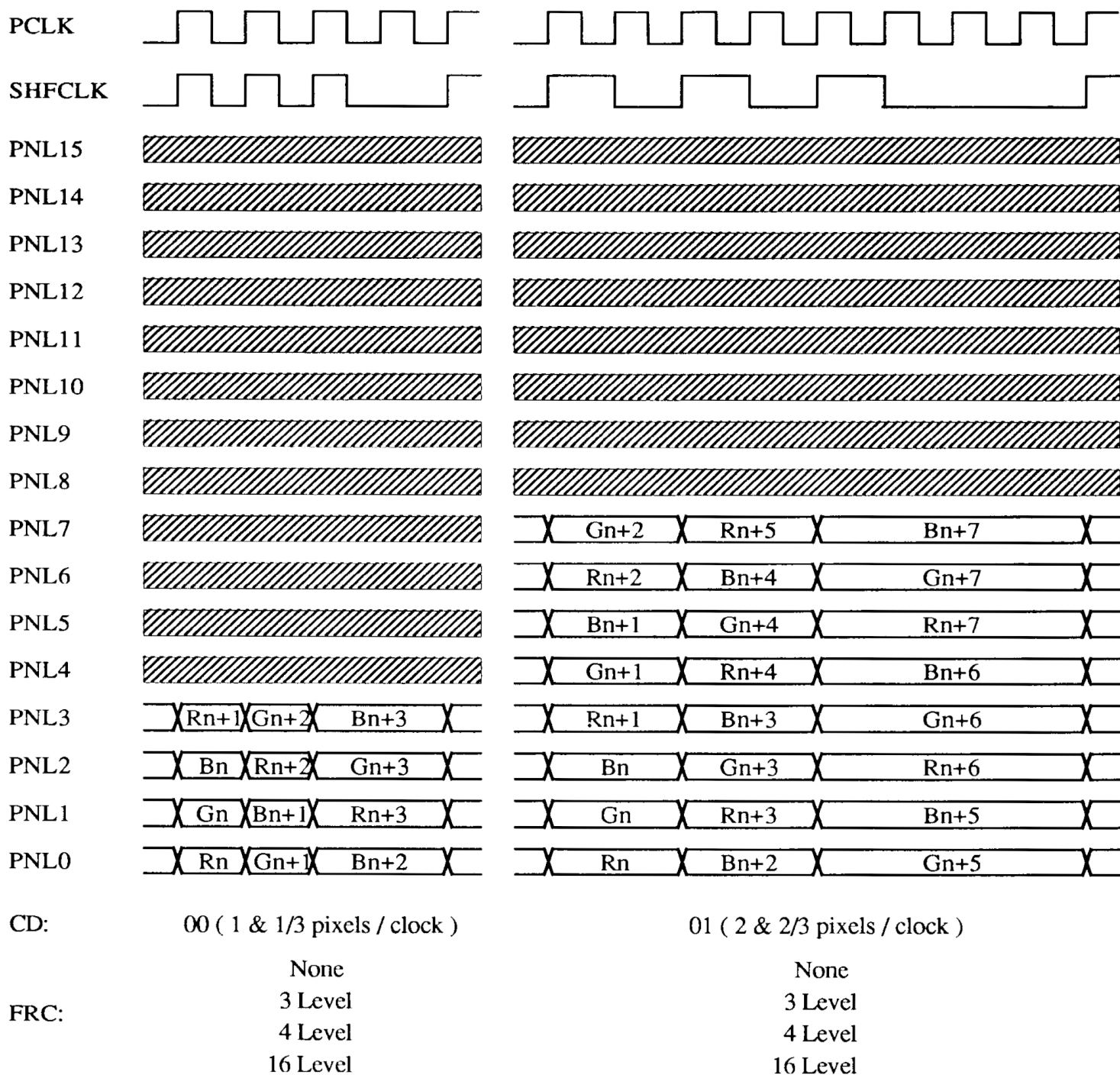
For example, if the panel only supports 2 shades per color, connect the panel data inputs as follows:

- PNL10 <-> R0
- PNL11 <-> R1
- PNL6 <-> G0
- PNL7 <-> G1
- PNL2 <-> B0
- PNL3 <-> B1



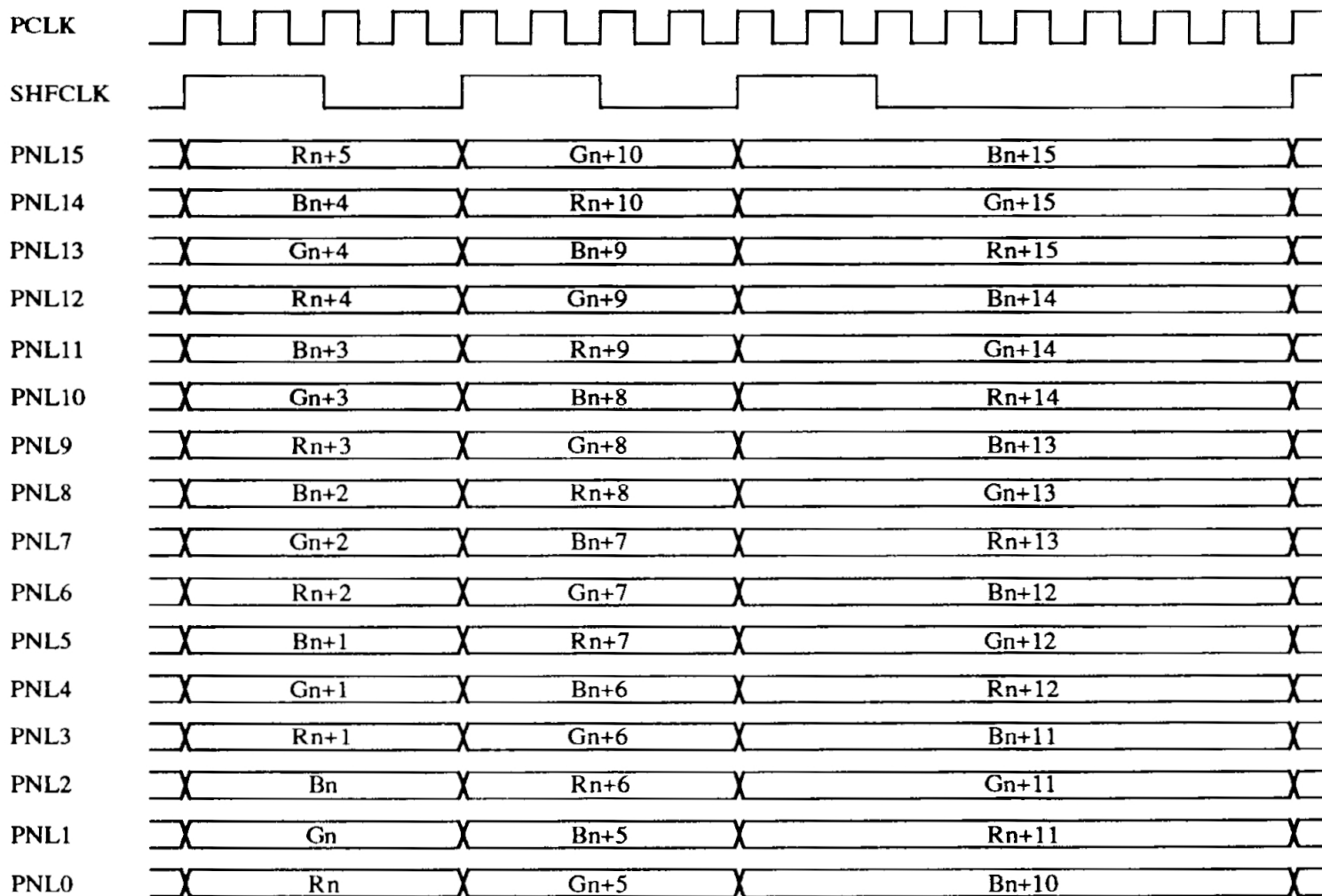
**82C457 Panel Pixel Order - 3-bit FRC with Clock Divide 00 (1/1), 01 (1/2) & 10 (1/4)**

This diagram shows the pixel output order for 3-bit FRC with clock divides of 1, 2 and 4. This is one of three data formats available for panels with no internal color support. Although one or more pixels may be required per shift clock, these panels use only one bit of color data per pixel.



**82C457 Panel Pixel Order - 4-bit Packed Data with Clock Divide 00 (1/1) & 01 (1/2)**

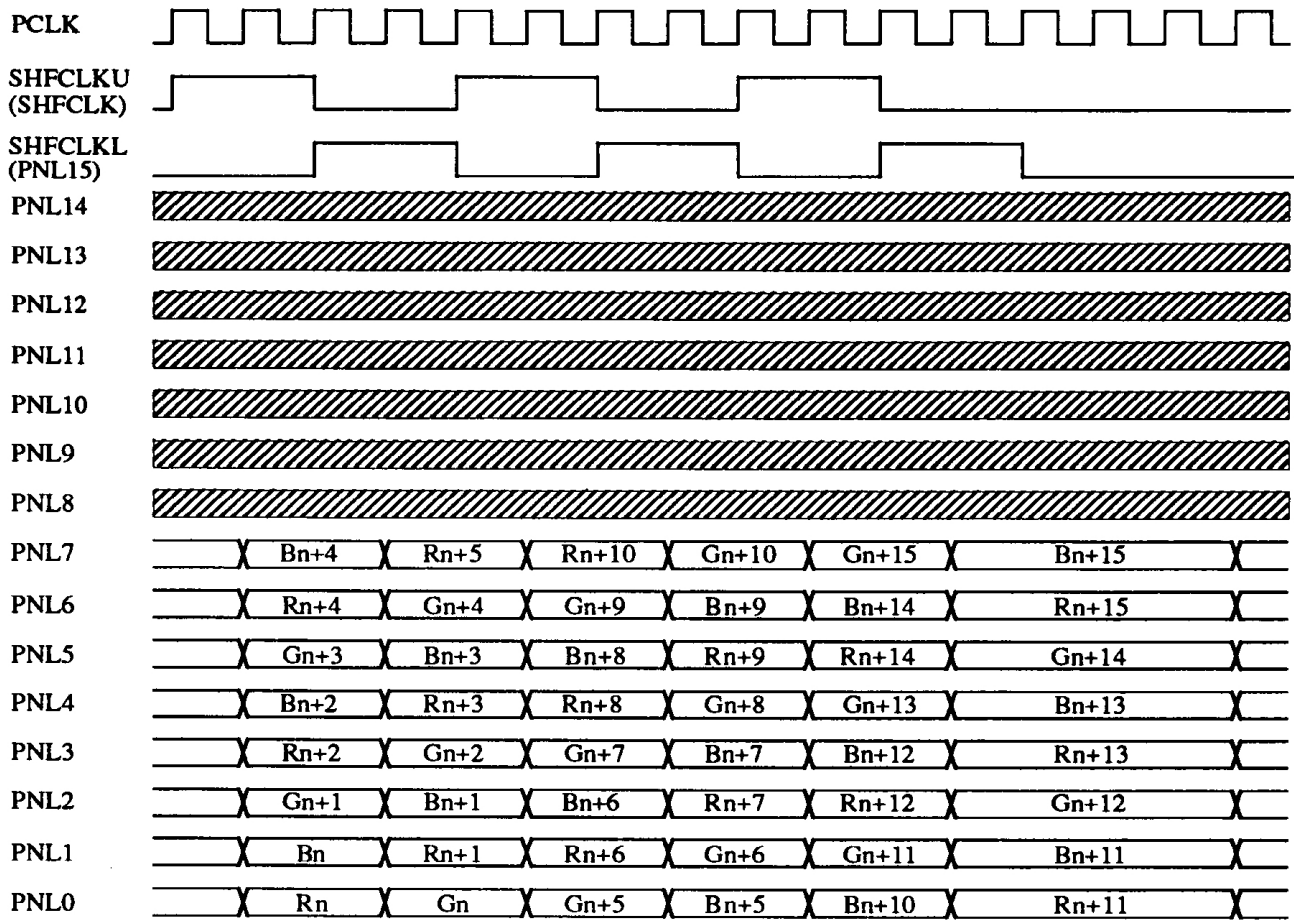
This diagram and the one following show the pixel output order for 4-bit packed data with clock divides of 1, 2 and 4. In this data format, the data order changes with each clock. After three clock cycles, one clock is "dropped" and the data order repeats.



CD: 10 ( 5 & 1/3 pixels / clock )

FRC: None  
3 Level  
4 Level  
16 Level

**82C457 Panel Pixel Order - 4-bit Packed Data with Clock Divide 10 (1/4)**



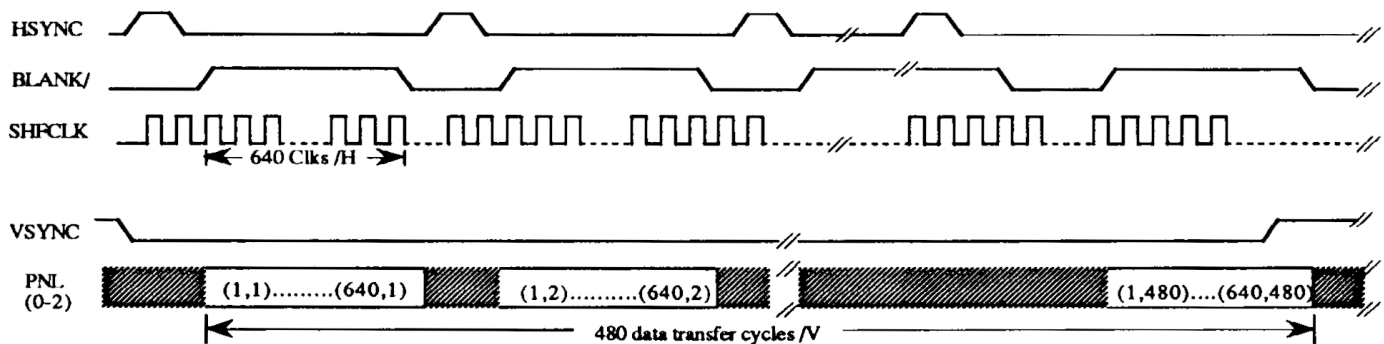
CD: 10 ( 5 & 1/3 pixels / clock )

FRC: None  
3 Level  
4 Level  
16 Level

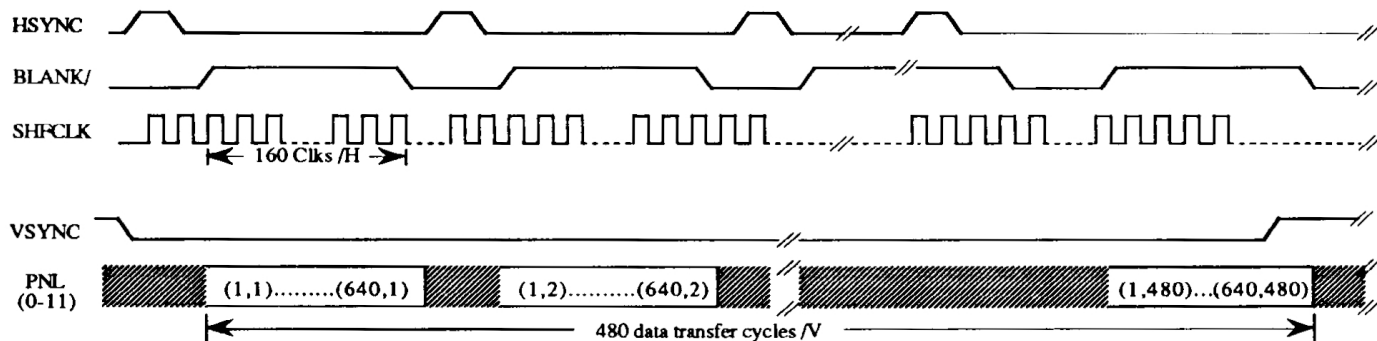
**82C457 Panel Pixel Order - Extended 4-bit Packed Data with Clock Divide 10 (1/4)**

This diagram shows the pixel order for the Extended 4-bit packed data format. In this configuration, the PNL15 data pin is redefined as an additional shift clock. The two shift clocks operate out-of-phase, clocking data on the falling edge of each shift clock. The data order changes with every clock cycle. After each shift clock has latched three data packets, one shift clock is dropped and the cycle repeats.

This format is only supported for a clock divide of 4.



**Single Panel, 3-bit Data, SM=0, CD=00  
(1 pixel / clock)**

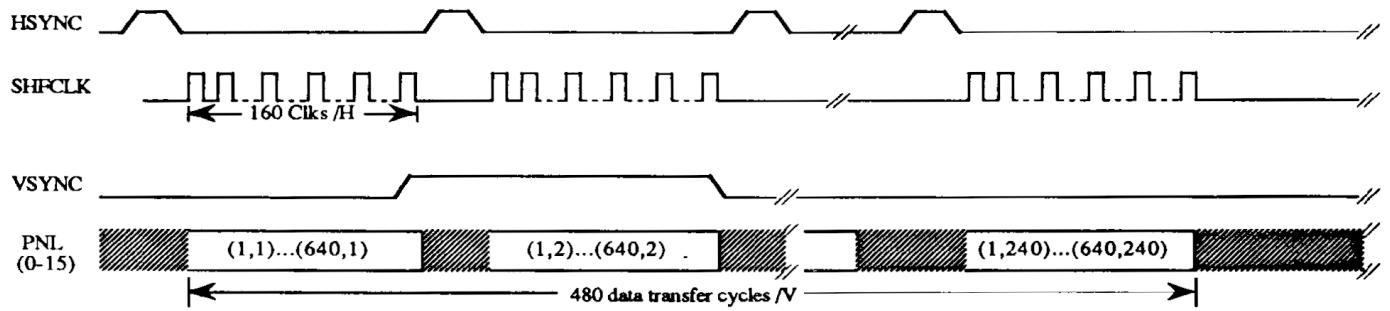


**Single Panel, 3-bit Data, SM=0, CD=10  
(4 pixel / clock)**

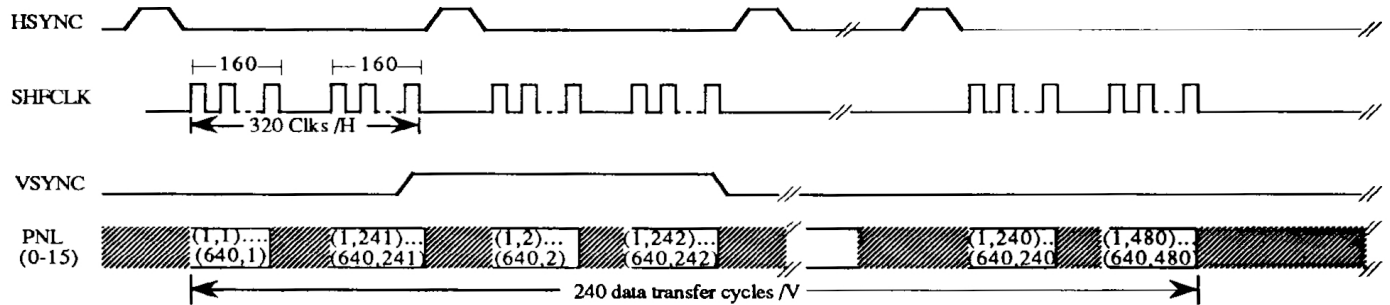
**82C457 Panel Pixel Order for CD=00 vs CD=10  
(1 vs. 4 pixel / clock)**

This diagram shows the pixel data output order for a single panel with 3-bit FRC data. The upper figure shows a clock divide of one (CD=00). There are 640 clock pulses per line, one for each pixel. The lower figure shows a clock divide of 4 (CD=10). There are 160 clock pulses per line, 4 pixels per clock.

In both figures, the clock masking is off (SM=0). Therefore the clock toggles continuously and the BLANK/ pin is used to qualify the valid video data. In the following figures, clock masking is enabled (SM=1). In that case, the shift clock stops during the blank interval, thereby qualifying the valid data. The BLANK/ pin is not used.



**Single Panel , 3-bit Data, SM=1, CD=10  
(4 pixel / clock )**



**Dual Panel, 3-bit Data, SM=1, CD=10  
(4 pixel / clock)**

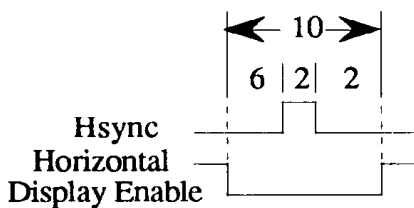
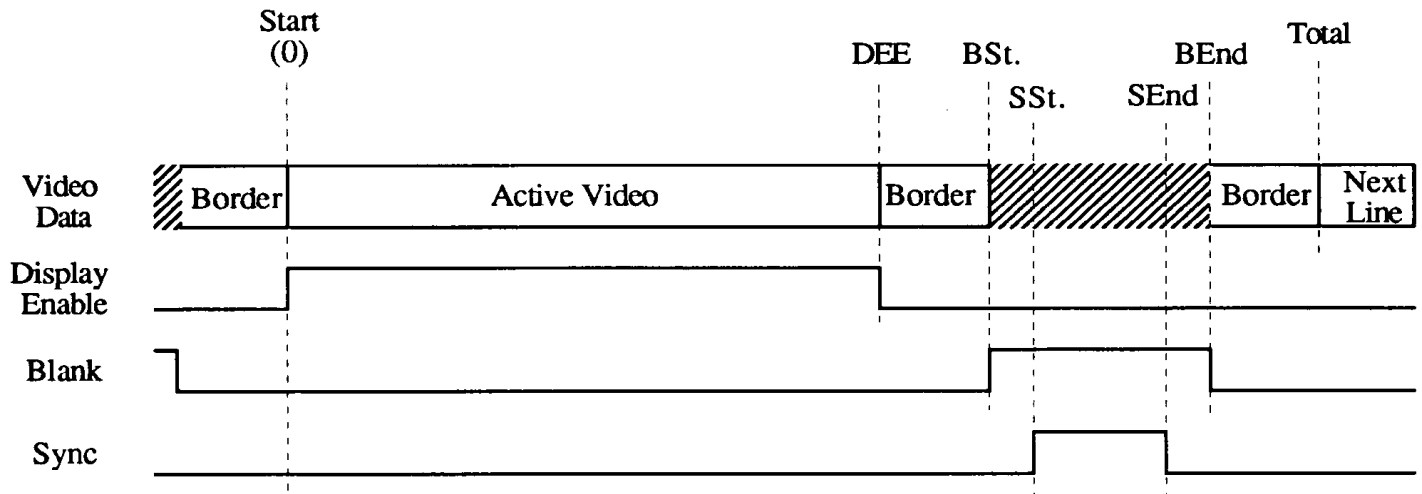
**82C457 Panel Pixel Order for Single Panel (SS) vs Dual Panel (DS)**

This diagram shows the pixel data output order for 3-bit packed FRC data with 4 pixels / clock (CD=10).

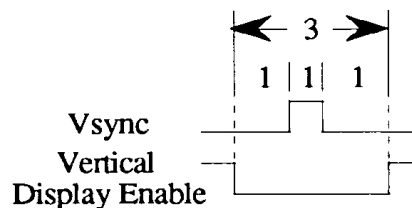
The upper figure shows a single panel display. Since four pixels are transferred per clock, there are 160 clocks per line. There are 480 active display lines and one line is transferred during each horizontal interval. There are 480 horizontal syncs in each vertical interval.

The lower figure shows a dual panel display. In this case, two lines are transferred per horizontal interval and there are 320 clock per horizontal interval. Even though there are still 480 active display lines, there are only 240 horizontal syncs per vertical. The data for the upper panel is shifted out first, followed by the data for the lower panel.

In both figures, the clock masking is enabled (SM=1). Therefore the shift clock stops during the blank interval, thereby qualifying the valid data. The BLANK/ pin is not used. In the figures on the preceding pages, clock masking is disabled (SM=0). In that case, the clock toggles continuously and the BLANK/ pin is used to qualify the valid video data.



Min HSYNC parameters (characters)



Min VSYNC parameters (lines)

**82C457 Panel Sync Relationship**

This diagram shows the relationship of active data, border area, blank and sync signals. It also shows the limits for the horizontal and vertical parameters.

The origin for all timing information is the start of the active display area. All horizontal values are measured in character clocks and vertical values in lines. The relationship of active video to the blank and sync signals is the same both horizontally and vertically.

The start of the active display area is the point from which all other edges are measured. The end of active video is determined by the "Display Enable End" (DEE). The total time of a line or frame is determined by the "Total" value. Horizontally, the total must be 5 greater than the display enable end; vertically it must be one greater than the display end. On flat panels, the vertical display end is the size of the panel. The end of the border is determined the Blank Start (BSt.) For flat panel horizontal timing, there is no border and DEE=BSt. The Sync start is determined by SSt. and the end by SEnd. There are two restrictions on sync. 1) It must start and end during the blank interval. 2) The minimum sync is 3 characters wide horizontally and 1 line vertically.

For flat panels, the minimum timing relationships may be summarized as follows:

Hsync End - Hsync Start  $\geq$  2 (Single panel/Single Drive, SS), 3 (Dual panel/Single Drive, DS)

Hsync End = Horizontal Total = Horizontal Blank End = Horizontal Display End + 10 (SS) or 14 (DS)

Vsync End - Vsync Start  $\geq$  1

Vsync End = Vertical Total = Vertical Display End + 3



# Panel Interface Examples

This section contains hook-up schemes and register parameters for each of the following panels.

- 1) HITACHI TM26D05VC 640x480 8-color TFT
- 2) HITACHI TM26D50VC 640x480 512-color TFT
- 3) OPTREX DMF6121 640x480 8-color STN
- 4) SANYO LCM5313/5314 640x480 8-color STN
- 5) SEIKO INSTRUMENT X642G 640x480 8-color STN
- 6) SHARP LM64C02P 640x400 8-color STN
- 7) SHARP LM64C03P 640x480 8-color STN
- 8) SHARP LQ10D015 640x480 512-color TFT
- 9) Simultaneous Display Implementation

## HITACHI TM26D05VC Hook-up Example

For an interface to the Hitachi TM26D05VC 8-color TFT panel, the signals should be hooked up as follows:

457 DK board Connector P3		Hitachi TM26D05VC		
Pin#	Signal	Pin#	Signal	
3	VSYNC	→	12	VSYNC
5	HSYNC	→	14	HSYNC
7	BLANK	→	16	DTMG
15	PNL1	→	18	GD
17	PNL2	→	20	RD
13	PNL0	→	22	BD
9	SHFCLK	→	26	DCLK

## HITACHI TM26D05VC Display File (Centering; No Stretching)

### ; Display switches

XR08 = 02 ; General Purpose Output B

XR09 = 00 ; General Purpose Output A

### ; Alternate/Flat Panel Horizontal Display Registers

XR18 = 4F ; Alternate Horizontal Display Enable End

XR19 = 56 ; Alternate Horizontal Sync Start

XR1A = 18 ; Alternate Horizontal Sync End

XR1B = 54 ; Alternate Horizontal Total

XR1C = 54 ; Alternate Horizontal Blanking Start

XR1D = 4F ; Alternate Horizontal Blanking End

XR1E = 28 ; Alternate Offset

### ; Flat Panel Interface Registers

XR50 = 03 ; Panel Format

XR51 = 48 ; Display Type

XR52 = 41 ; Panel Size

XR53 = 00 ; Override

XR54 = 08 ; Alternate Miscellaneous Output

XR55 = 10 ; Text Mode 350A Compensation

XR56 = 10 ; Text Mode 350B Compensation

XR57 = 10 ; Text Mode 400 Compensation

XR58 = 00 ; Graphics Mode 350 Compensation

XR59 = 00 ; Graphics Mode 400 Compensation

XR5A = 27 ; Flat Panel Vertical Display Start 400

XR5B = B7 ; Flat Panel Vertical Display End 400

XR5E = 81 ; ACDCLK Control

XR5F = 4E ; Power down Mode Refresh

XR60 = 88 ; Blink Rate Control

### ; Alternate/Flat Panel Vertical Display Registers

XR64 = E0 ; Alternate Vertical Total

XR65 = 07 ; Alternate Overflow

XR66 = E0 ; Alternate Vertical Sync Start

XR67 = 01 ; Alternate Vertical Sync End

XR68 = DF ; Alternate Vertical Display Enable End

XR69 = 40 ; Flat Panel Vertical Display Start 350

XR6A = 9E ; Flat Panel Vertical Display End 350

XR6B = 50 ; Flat Panel Vertical Overflow 2

XR6D = 7B ; FRC and Palette Control

XR6E = BD ; Polynomial FRC Counter

## HITACHI TM26D50VC Hook-up Example

For an interface to the HITACHI TM26D50VC 512 color TFT color panel, the signals should be hooked up as follows:

457 DK board Connector P3			Hitachi TM26D50VC	
<u>Pin#</u>	<u>Signal</u>		<u>Pin #</u>	<u>Signal</u>
40	PNL11	→	2	R3
38	PNL10	→	3	R2
36	PNL9	→	4	R1
32	PNL7	→	6	G3
30	PNL6	→	7	G2
28	PNL5	→	8	G1
19	PNL3	→	10	B3
17	PNL2	→	11	B2
15	PNL1	→	12	B1
7	BLANK	→	15	DTMG
3	VSYNC	→	17	VSYNC
5	HSYNC	→	19	HSYNC
9	SHFCLK	→	21	DCLK
	GND	→	29	DOTC
	VCC	→	28	BLC
	GND	→	14	HREV

## HITACHI TM26A02VC Display File (Centering; No Stretching)

; Display switches

XR08 = 02 ; General Purpose Output B

XR09 = 00 ; General Purpose Output A

; Alternate/Flat Panel Horizontal Display Registers

XR18 = 4F ; Alternate Horizontal Display Enable End

XR19 = 56 ; Alternate Horizontal Sync Start

XR1A = 1D ; Alternate Horizontal Sync End

XR1B = 5F ; Alternate Horizontal Total

XR1C = 5F ; Alternate Horizontal Blanking End

XR1D = 4F ; Alternate Horizontal Blanking Start

XR1E = 28 ; Alternate Offset

XR50 = 08 ; Panel Format

XR51 = 48 ; Display Type

XR52 = 41 ; Panel Size

XR53 = 00 ; Override

XR54 = C4 ; Alternate Miscellaneous Output

XR55 = 10 ; Text Mode 350\_A Compensation

XR56 = 10 ; Text Mode 350\_B Compensation

XR57 = 10 ; Text Mode 400 Compensation

XR58 = 00 ; Graphics Mode 350 Compensation

XR59 = 00 ; Graphics Mode 400 Compensation

XR5A = 27 ; Flat Panel Vertical Display Start\_400

XR5B = B7 ; Flat Panel Vertical Display End\_400

XR5E = 80 ; ACDCLK Control

XR5F = 4E ; Power Down Mode Refresh

XR60 = 88 ; Blink Rate Control

XR64 = 04 ; Alternate Vertical Total

XR65 = 26 ; Alternate Overflow

XR66 = E2 ; Alternate Vertical Sync Start

XR67 = 05 ; Alternate Vertical Sync End

XR68 = DF ; Alternate Vertical Display Enable End

XR69 = 40 ; Flat Panel Vertical Display Start\_350

XR6A = 9E ; Flat Panel Vertical Display End\_350

XR6B = 50 ; Flat Panel Vertical Overflow 2

XR6D = 7B ; FRC and Palette Control

XR6E = BD ; Polynomial FRC Control

## OPTREX DMF6121 Hook-up Example

For an interface to the Optrex DMF6121 STN color panel, the signals should be hooked up as follows:

457 DK board Connector P3			Optrex DMF6121		
Pin#	Signal		Pin#	Signal	
3	VSYNC	→	2	FLM	
5	HSYNC	→	3	LP	
9	SHFCLK	→	4	CP	
1	ACDCLK	→	5	M	
46	PNL14	→	10	UD0	
42	PNL12	→	11	UD1	
38	PNL10	→	12	UD2	
34	PNL8	→	13	UD3	
30	PNL6	→	14	UD4	
26	PNL4	→	15	UD5	
17	PNL2	→	16	UD6	
13	PNL0	→	17	UD7	
48	PNL15	→	18	LD0	
44	PNL13	→	19	LD1	
40	PNL11	→	20	LD2	
36	PNL9	→	21	LD3	
32	PNL7	→	22	LD4	
28	PNL5	→	23	LD5	
19	PNL3	→	24	LD6	
15	PNL1	→	25	LD7	

## OPTREX DMF6121 Display File (Centering; No Stretching)

### ; Display switches

XR08 = 06 ; General Purpose Output B  
XR09 = 00 ; General Purpose Output A

### ; Alternate/Flat Panel Horizontal Display Registers

XR18 = 4F ; Alternate Horizontal Display Enable End  
XR19 = 56 ; Alternate Horizontal Sync Start  
XR1A = 18 ; Alternate Horizontal Sync End  
XR1B = 54 ; Alternate Horizontal Total  
XR1C = 54 ; Alternate Horizontal Blanking Start  
XR1D = 4F ; Alternate Horizontal Blanking End  
XR1E = 28 ; Alternate Offset

### ; Flat Panel Interface Registers

XR50 = A2 ; Panel Format  
XR51 = 50 ; Display Type  
XR52 = 41 ; Panel Size  
XR53 = 00 ; Override  
XR54 = 08 ; Alternate Miscellaneous Output  
XR55 = 10 ; Text Mode 350A Compensation  
XR56 = 10 ; Text Mode 350B Compensation  
XR57 = 10 ; Text Mode 400 Compensation  
XR58 = 00 ; Graphics Mode 350 Compensation  
XR59 = 00 ; Graphics Mode 400 Compensation  
XR5A = 27 ; Flat Panel Vertical Display Start 400  
XR5B = B7 ; Flat Panel Vertical Display End 400  
XR5E = 80 ; ACDCLK Control  
XR5F = 4E ; Power down Mode Refresh  
XR60 = 88 ; Blink Rate Control

### ; Alternate/Flat Panel Vertical Display Registers

XR64 = E0 ; Alternate Vertical Total  
XR65 = 07 ; Alternate Overflow  
XR66 = E0 ; Alternate Vertical Sync Start  
XR67 = 01 ; Alternate Vertical Sync End  
XR68 = DF ; Alternate Vertical Display Enable End  
XR69 = 40 ; Flat Panel Vertical Display Start 350  
XR6A = 9E ; Flat Panel Vertical Display End 350  
XR6B = 50 ; Flat Panel Vertical Overflow 2  
XR6D = 7B ; FRC and Palette Control  
XR6E = BD ; Polynomial FRC Control

## SANYO LCM5413/5314 Hook-up Example

For an interface to the Sanyo LCM5313/5314-NAK22 STN color panel, the signals should be hooked up as follows:

457 DK board Connector P3		Sanyo LCM5313/5314-NAK22	
<u>Pin#</u>	<u>Signal</u>		<u>Pin#</u> <u>Signal</u>
3	VSYNC	→	1    FLM
1	ACDCLK	→	2    M
5	HSYNC	→	4    CL1
9	SHFCLK	→	6    CL2
46	PNL14	→	9    UD0
42	PNL12	→	10   UD1
38	PNL10	→	11   UD2
34	PNL8	→	12   UD3
30	PNL6	→	13   UD4
26	PNL4	→	14   UD5
17	PNL2	→	15   UD6
13	PNL0	→	16   UD7
48	PNL15	→	17   LD0
44	PNL13	→	18   LD1
40	PNL11	→	19   LD2
36	PNL9	→	20   LD3
32	PNL7	→	21   LD4
28	PNL5	→	22   LD5
19	PNL3	→	23   LD6
15	PNL1	→	24   LD7



## SANYO LCM5413/5314 Display File (Centering; No Stretching)

### ; Display switches

XR08 = 06 ; General Purpose Output B  
XR09 = 00 ; General Purpose Output A

### ; Alternate/Flat Panel Horizontal Display Registers

XR18 = 4F ; Alternate Horizontal Display Enable End  
XR19 = 56 ; Alternate Horizontal Sync Start  
XR1A = 18 ; Alternate Horizontal Sync End  
XR1B = 54 ; Alternate Horizontal Total  
XR1C = 54 ; Alternate Horizontal Blanking Start  
XR1D = 4F ; Alternate Horizontal Blanking End  
XR1E = 28 ; Alternate Offset

### ; Flat Panel Interface Registers

XR50 = A2 ; Panel Format  
XR51 = 50 ; Display Type  
XR52 = 41 ; Panel Size  
XR53 = 00 ; Override  
XR54 = 08 ; Alternate Miscellaneous Output  
XR55 = 10 ; Text Mode 350A Compensation  
XR56 = 10 ; Text Mode 350B Compensation  
XR57 = 10 ; Text Mode 400 Compensation  
XR58 = 00 ; Graphics Mode 350 Compensation  
XR59 = 00 ; Graphics Mode 400 Compensation  
XR5A = 27 ; Flat Panel Vertical Display Start 400  
XR5B = B7 ; Flat Panel Vertical Display End 400  
XR5E = 80 ; ACDCLK Control  
XR5F = 4E ; Power down Mode Refresh  
XR60 = 88 ; Blink Rate Control

### ; Alternate/Flat Panel Vertical Display Registers

XR64 = E0 ; Alternate Vertical Total  
XR65 = 07 ; Alternate Overflow  
XR66 = E0 ; Alternate Vertical Sync Start  
XR67 = 01 ; Alternate Vertical Sync End  
XR68 = DF ; Alternate Vertical Display Enable End  
XR69 = 40 ; Flat Panel Vertical Display Start 350  
XR6A = 9E ; Flat Panel Vertical Display End 350  
XR6B = 50 ; Flat Panel Vertical Overflow 2  
XR6D = 7B ; FRC and Palette Control  
XR6E = BD ; Polynomial FRC Control

## SEIKO INSTRUMENT X642G Hook-up Example

For an interface to the SEIKO INSTRUMENT X642G STN color panel, the signals should be hooked up as follows:

457 DK board Connector P3			Seiko Instrument X642G	
<u>Pin#</u>	<u>Signal</u>		<u>Pin#</u>	<u>Signal</u>
19	PNL3	→	3	D4
17	PNL2	→	5	D5
15	PNL1	→	7	D6
13	PNL0	→	9	D7
32	PNL7	→	13	D0
30	PNL6	→	15	D1
28	PNL5	→	17	D2
26	PNL4	→	19	D3
1	ACDCLK	→	23	M
3	VSYNC	→	25	YD
9	SHFCLK	→	27	XSCLU
5	HSYNC	→	31	LP
48	PNL15	→	37	XSCLL

## SEIKO INSTRUMENT X642G Display File (Centering; No Stretching)

### ; Display switches

XR08 = 02 ; General Purpose Output B

XR09 = 00 ; General Purpose Output A

### ; Alternate/Flat Panel Horizontal Display Registers

XR18 = 4F ; Alternate Horizontal Display Enable End

XR19 = 56 ; Alternate Horizontal Sync Start

XR1A = 18 ; Alternate Horizontal Sync End

XR1B = 54 ; Alternate Horizontal Total

XR1C = 54 ; Alternate Horizontal Blanking Start

XR1D = 4F ; Alternate Horizontal Blanking End

XR1E = 28 ; Alternate Offset

### ; Flat Panel Interface Registers

XR50 = A2 ; Panel Format

XR51 = 70 ; Display Type

XR52 = 41 ; Panel Size

XR53 = 00 ; Override

XR54 = 08 ; Alternate Miscellaneous Output

XR55 = 10 ; Text Mode 350A Compensation

XR56 = 10 ; Text Mode 350B Compensation

XR57 = 10 ; Text Mode 400 Compensation

XR58 = 00 ; Graphics Mode 350 Compensation

XR59 = 00 ; Graphics Mode 400 Compensation

XR5A = 27 ; Flat Panel Vertical Display Start 400

XR5B = B7 ; Flat Panel Vertical Display End 400

XR5E = 80 ; ACDCLK Control

XR5F = 4E ; Power down Mode Refresh

XR60 = 88 ; Blink Rate Control

### ; Alternate/Flat Panel Vertical Display Registers

XR64 = E0 ; Alternate Vertical Total

XR65 = 07 ; Alternate Overflow

XR66 = E0 ; Alternate Vertical Sync Start

XR67 = 01 ; Alternate Vertical Sync End

XR68 = DF ; Alternate Vertical Display Enable End

XR69 = 40 ; Flat Panel Vertical Display Start 350

XR6A = 9E ; Flat Panel Vertical Display End 350

XR6B = 50 ; Flat Panel Vertical Overflow 2

XR6D = 7B ; FRC and Palette Control

XR6E = BD ; Polynomial FRC Control

## SHARP LM64C02P Hook-up Example

For an interface to the Sharp LM64C02P STN color panel, the signals should be hooked up as follows:

457 DK board Connector P3			Sharp LM64C02P	
<u>Pin#</u>	<u>Signal</u>		<u>Pin#</u>	<u>Signal</u>
3	VSYNC	→	1	YD
5	HSYNC	→	2	LP
9	SHFCLK	→	3	XCKL
48	PNL15	→	4	XCKU
13	PNL0	→	10	D0
15	PNL1	→	11	D1
17	PNL2	→	12	D2
19	PNL3	→	13	D3
26	PNL4	→	14	D4
28	PNL5	→	15	D5
30	PNL6	→	16	D6
32	PNL7	→	17	D7

## SHARP LM64C02P Display File (Centering; No Stretching)

### ; Display switches

XR08 = 02 ; General Purpose Output B

XR09 = 00 ; General Purpose Output A

### ; Alternate/Flat Panel Horizontal Display Registers

XR18 = 4F ; Alternate Horizontal Display Enable End

XR19 = 56 ; Alternate Horizontal Sync Start

XR1A = 18 ; Alternate Horizontal Sync End

XR1B = 54 ; Alternate Horizontal Total

XR1C = 54 ; Alternate Horizontal Blanking Start

XR1D = 4F ; Alternate Horizontal Blanking End

XR1E = 28 ; Alternate Offset

### ; Flat Panel Interface Registers

XR50 = A2 ; Panel Format

XR51 = 70 ; Display Type

XR52 = 21 ; Panel Size

XR53 = 00 ; Override

XR54 = 08 ; Alternate Miscellaneous Output

XR55 = 10 ; Text Mode 350A Compensation

XR56 = 10 ; Text Mode 350B Compensation

XR57 = 10 ; Text Mode 400 Compensation

XR58 = 00 ; Graphics Mode 350 Compensation

XR59 = 00 ; Graphics Mode 400 Compensation

XR5A = 00 ; Flat Panel Vertical Display Start 400

XR5B = B7 ; Flat Panel Vertical Display End 400

XR5E = 80 ; ACDCLK Control

XR5F = 4E ; Power down Mode Refresh

XR60 = 88 ; Blink Rate Control

### ; Alternate/Flat Panel Vertical Display Registers

XR64 = 90 ; Alternate Vertical Total

XR65 = 07 ; Alternate Overflow

XR66 = 90 ; Alternate Vertical Sync Start

XR67 = 01 ; Alternate Vertical Sync End

XR68 = 8F ; Alternate Vertical Display Enable End

XR69 = 19 ; Flat Panel Vertical Display Start 350

XR6A = 77 ; Flat Panel Vertical Display End 350

XR6B = 50 ; Flat Panel Vertical Overflow 2

XR6D = 7B ; FRC and Palette Control

XR6E = BD ; Polynomial FRC Control

## SHARP LM64C03PHook-up Example

For an interface to the Sharp LM64C03P STN color panel, the signals should be hooked up as follows:

457 DK board Connector P3			Sharp LM64C03P	
<u>Pin#</u>	<u>Signal</u>		<u>Pin#</u>	<u>Signal</u>
3	VSYNC	→	1	YD
5	HSYNC	→	2	LP
9	SHFCLK	→	3	XCKL
48	PNL15	→	4	XCKU
13	PNL0	→	11	D0
15	PNL1	→	12	D1
17	PNL2	→	13	D2
19	PNL3	→	14	D3
26	PNL4	→	15	D4
28	PNL5	→	16	D5
30	PNL6	→	17	D6
32	PNL7	→	18	D7

## SHARP LM64C03P Display File (Centering; No Stretching)

; Display switches

XR08 = 02 ; General Purpose Output B

XR09 = 00 ; General Purpose Output A

; Alternate/Flat Panel Horizontal Display Registers

XR18 = 4F ; Alternate Horizontal Display Enable End

XR19 = 56 ; Alternate Horizontal Sync Start

XR1A = 18 ; Alternate Horizontal Sync End

XR1B = 54 ; Alternate Horizontal Total

XR1C = 54 ; Alternate Horizontal Blanking Start

XR1D = 4F ; Alternate Horizontal Blanking End

XR1E = 28 ; Alternate Offset

; Flat Panel Interface Registers

XR50 = A2 ; Panel Format

XR51 = 70 ; Display Type

XR52 = 41 ; Panel Size

XR53 = 00 ; Override

XR54 = 08 ; Alternate Miscellaneous Output

XR55 = 10 ; Text Mode 350A Compensation

XR56 = 10 ; Text Mode 350B Compensation

XR57 = 10 ; Text Mode 400 Compensation

XR58 = 00 ; Graphics Mode 350 Compensation

XR59 = 00 ; Graphics Mode 400 Compensation

XR5A = 27 ; Flat Panel Vertical Display Start 400

XR5B = B7 ; Flat Panel Vertical Display End 400

XR5E = 80 ; ACDCLK Control

XR5F = 4E ; Power down Mode Refresh

XR60 = 88 ; Blink Rate Control

; Alternate/Flat Panel Vertical Display Registers

XR64 = E0 ; Alternate Vertical Total

XR65 = 07 ; Alternate Overflow

XR66 = E0 ; Alternate Vertical Sync Start

XR67 = 01 ; Alternate Vertical Sync End

XR68 = DF ; Alternate Vertical Display Enable End

XR69 = 40 ; Flat Panel Vertical Display Start 350

XR6A = 9E ; Flat Panel Vertical Display End 350

XR6B = 50 ; Flat Panel Vertical Overflow 2

XR6D = 7B ; FRC and Palette Control

XR6E = BD ; Polynomial FRC Control

### SHARP LQ10D01 TFT Hook-up Example

The 512 color TFT LCD panel that Sharp is currently sampling (part #LQ10D01) has a CRT-like interface. A special interface chip on the panel converts the CRT-like data input to the panel for the panel's column drivers. This interface chip counts the number of shift clocks from the edge of HSYNC, counts the number of HSYNCs from the edge of VSYNC, measures shift clock frequency, detects the polarity of HSYNC and VSYNC, and then determines the active display timing for the various graphics modes in order to achieve display centering. This technique shifts the panel display noticeably between text, graphics, and 40/80 column modes. **The 82C457 provides direct interface to this panel in the 8 level PWM mode and generates 24,389 colors.** Chips provides Video BIOS to compensate for the screen shift from text to graphics modes. However, this technique has limitations to the extent that the 82C457 vertical compensation techniques for low resolution modes cannot be utilized and the display quality is severely inhibited by the fixed refresh rates.

Sharp is introducing a new model of their 512 color TFT LCD, LQ10D015, which contains one additional input pin - Display Enable - to interface directly to the 82C457 and thus overcome the above mentioned limitations. **Customers should contact Sharp and request the new model of the 512 color TFT LCD panel which contains the display enable signal.** The 82C457 has several vertical compensation techniques to center and stretch low resolution graphics modes (CGA, EGA, VGA mode 13) to symmetrically fill the panel display.

To interface the Sharp LQ10D01 panel with the display enable input to the 82C457 full color controller, the signals should be hooked-up as follows:

Sharp LQ10D015			DK82457 Connector P3	
<u>Pin#</u>	<u>Signal</u>		<u>Pin#</u>	<u>Signal</u>
1	CK	←	9	SHFCLK
2	GND	←	2	GND
3	R0	←	36	PNL9
4	R1	←	38	PNL10
5	R2	←	40	PNL11
6	GND	←	4	GND
7	G0	←	28	PNL5
8	G1	←	30	PNL6
9	G2	←	32	PNL7
10	GND	←	6	GND
11	B0	←	15	PNL1
12	B1	←	17	PNL2
13	B2	←	19	PNL3
14	GND	←	8	GND
15	HSYNC	←	5	HSYNC
16	GND	←	10	GND
17	VSYNC	←	3	VSYNC
18	VCC	←	20	+5V
19	GND	←	12	GND
20	VDD	←	+12V	
21	Enable	←	7	BLANK/



The 82C457 Rev. 0 behaves incorrectly in 8-level PWM mode with dither enabled. In order to interface to the Sharp LQ10D01 panel, the following signals should be rerouted between the 82C411 and the 82C457 (Rev. 0) to simulate 8-level PWM mode with dither using 16-level PWM with dither:

82C411 Output			82C457 Input	
<u>Signal</u>	<u>Pin#</u>		<u>Pin#</u>	<u>Signal</u>
R5	56	→	114	R5
R4	55	→	113	R4
R3	54	→	112	R3
R2	52	→	111	R2 - Gnd
R1	51	→	110	R1
		→	109	R0
R0	50	→	Not Connected	
<hr/>				
B5	1	→	127	B5
B4	64	→	126	B4
B3	63	→	125	B3
B2	61	→	124	B2 - Gnd
B1	60	→	123	B1
		→	122	B0
B0	59	→	Not Connected	
<hr/>				
G5	9	→	121	G5
G4	8	→	120	G4
G3	7	→	119	G3
G2	5	→	118	G2 - Gnd
G1	4	→	117	G1
		→	116	G0
G0	3	→	Not Connected	

Chips and Technologies, Inc. provides an 82C411 Plastic Flat Pack (PFP) carrier (called the 82C411 PFP-01) which incorporates the above illustrated changes. The 82C411 PFP-01 is designed to replace the existing 82C411 PFP module on the DK457-RC-01. No other changes need to be made to the DK457-RC-01 to support a 512 color TFT panel like the SHARP LQ10D01. Please contact your local CHIPS sales office for the 82C411 PFP-01 module to overcome the 8 level PWM anomaly.

To aid in interfacing the 82C457 to the Sharp LQ10D01 panel, the display files containing all the register parameters needed for panel only operation and simultaneous panel and CRT operation is attached.

## SHARP LQ10D01 TFT Display File

```
; "SRPT48.DIS" for SHARP Color TFT "LQ10D01" 640x480
; -3 bit-pack. -12 bit data. -16PWM. -SS. f=28.322MHz
; initialize 82C457 DK-Board
XR08 = 02 ; General Purpose Output Select B
XR09 = 00 ; General Purpose Output Select A
; panel related parameters
XR18 = 4F ; Alternate Horizontal Display Enable End
XR19 = 56 ; Alternate Horizontal Sync Start
XR1A = 1D ; Alternate Horizontal Sync End
XR1B = 5F ; Alternate Horizontal Total
XR1C = 5F ; Alternate Horizontal Blanking End
XR1D = 4F ; Alternate Horizontal Blanking Start
XR1E = 28 ; Alternate Offset
XR50 = 08 ; Panel Format
XR51 = 48 ; Display Type
XR52 = 41 ; Panel Size
XR53 = 00 ; Override
XR54 = C4 ; Alternate Miscellaneous Output
XR55 = 10 ; Text Mode 350_A Compensation
XR56 = 10 ; Text Mode 350_B Compensation
XR57 = 10 ; Text Mode 400 Compensation
XR58 = 00 ; Graphics Mode 350 Compensation
XR59 = 00 ; Graphics Mode 400 Compensation
XR5A = 27 ; Flat Panel Vertical Display Start_400
XR5B = B7 ; Flat Panel Vertical Display End_400
XR5E = 80 ; ACDCLK Control
XR5F = 4E ; Power Down Mode Refresh
XR60 = 88 ; Blink Rate Control
XR64 = 04 ; Alternate Vertical Total
XR65 = 26 ; Alternate Overflow
XR66 = E2 ; Alternate Vertical Sync Start
XR67 = 05 ; Alternate Vertical Sync End
XR68 = DF ; Alternate Vertical Display Enable End
XR69 = 40 ; Flat Panel Vertical Display Start_350
XR6A = 9E ; Flat Panel Vertical Display End_350
XR6B = 50 ; Flat Panel Vertical Overflow 2
XR6D = 7B ; FRC and Palette Control
XR6E = BD ; Polynomial FRC Control
```

## Simultaneous Display

The 82C457 is capable of providing simultaneous CRT and flat panel display. Using the current revision (Rev. 0) of the 82C457, limited external hardware is required.

### Hardware Implementation

The 82C457 Rev. 0 device outputs a CRT blank signal in CRT mode and a panel display enable signal in the flat panel mode on the BLANK/ pin. However, to support simultaneous CRT/LCD display, separate CRT blank and flat panel display enable signals need to be provided. The external circuitry generates a display enable signal from the CRT blank signal with the appropriate delays as shown below:

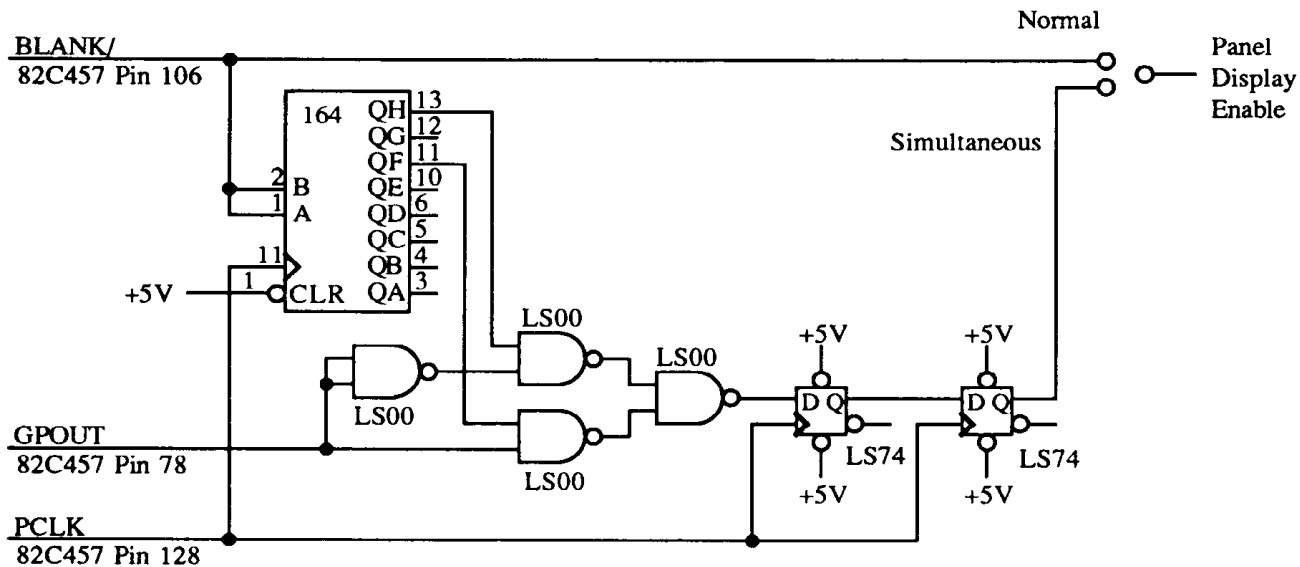
#### Graphics Mode

640/720 dot mode  
320x200 dot mode, 256 colors

#### Delay

10 PCLKs  
8 PCLKs

In order to generate the CRT BLANK/ signal and the panel video Display Enable signal with the proper timing on 82C457 Rev.0 silicon, external delay logic is required.



ERMEN/ (also called GPOUT) on pin 78 of the 82C457 is used to switch between the above mentioned two cases.

## **BIOS Modification for Simultaneous Display**

In order to switch modes correctly in simultaneous display, the BIOS needs to work in conjunction with the external logic. Every time a mode change is performed, the 82C457 Rev. 0 extension registers should be programmed as follows:

<u>Extension Register</u>	<u>640 dot mode</u>	<u>320 dot mode</u>	<u>256 color mode</u>
XR09	0	1	1
XR19	54	58	53
XR1A	1F	0	1F
XR54	C0	C1	C0
XR6D	79	7C	78

For simultaneous display, XR1C and XR1D also need to be programmed to generate the active CRT signal before the active panel signal.

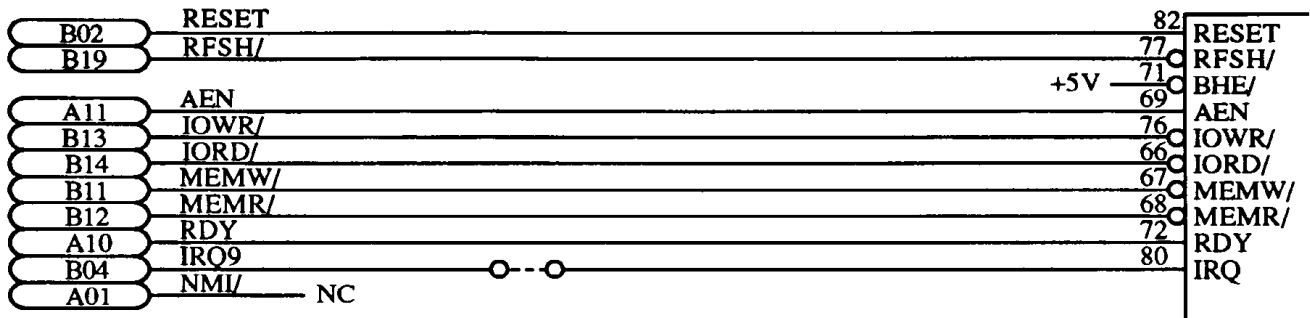
<u>Extension Register</u>	<u>Simultaneous Display</u>	<u>Normal Display</u>
XR1C	60	5F
XR1D	50	4F

Chips and Technologies, Inc. provides a modified version of the 82C457 BIOS which incorporates these parameters and allows the end user to switch between panel only, CRT only, and simultaneous panel and CRT display. Please contact your local CHIPS Sales Office for details on this BIOS.

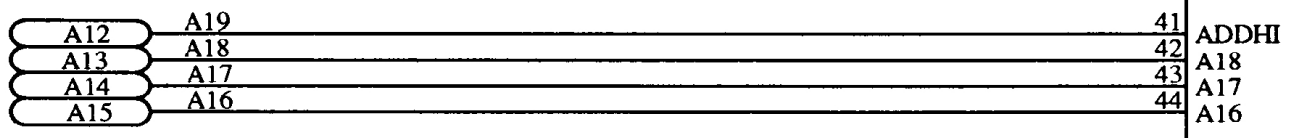
# Application Schematic Examples

This section includes schematic examples showing how to connect the 82C457 chip. The schematics are broken down into four main groups for discussion:

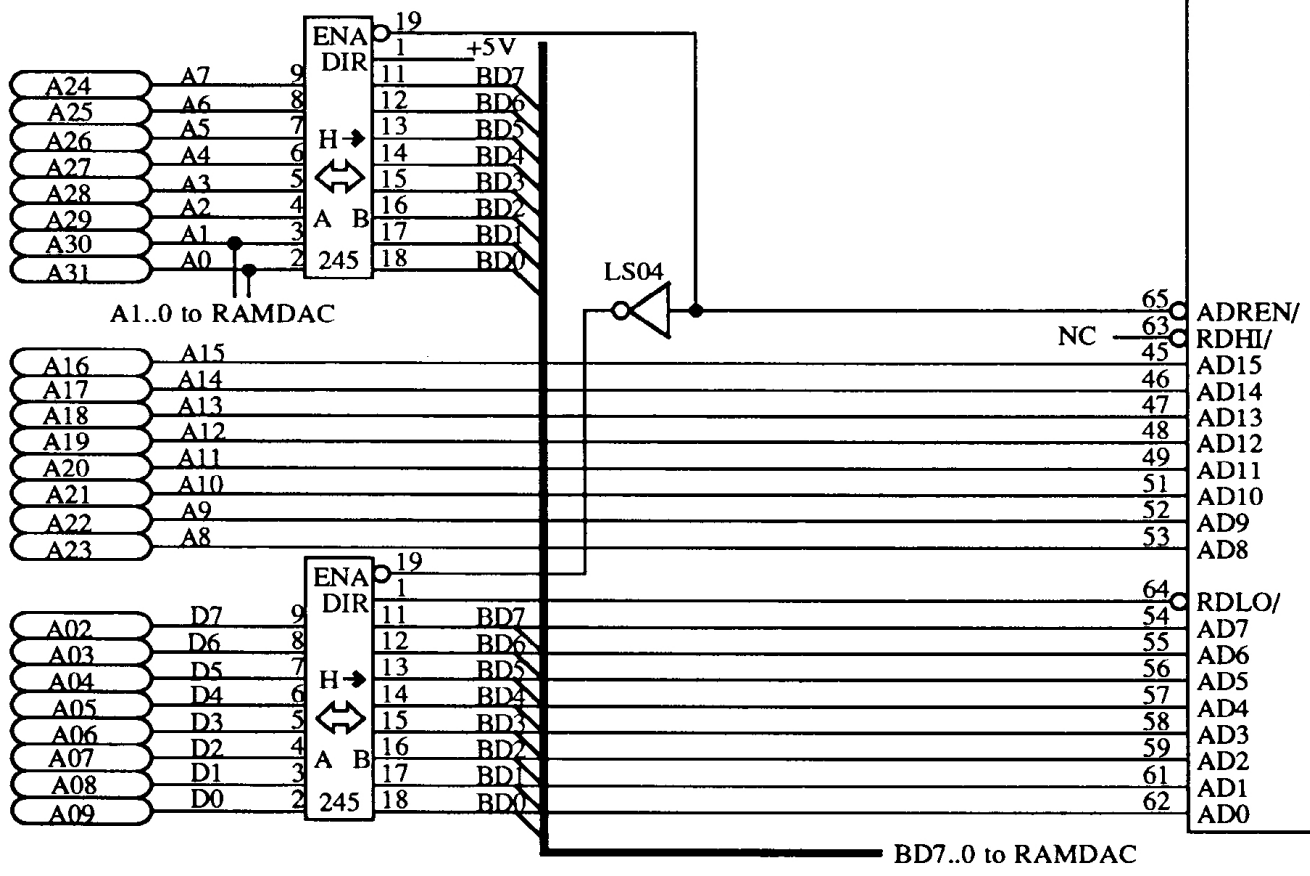
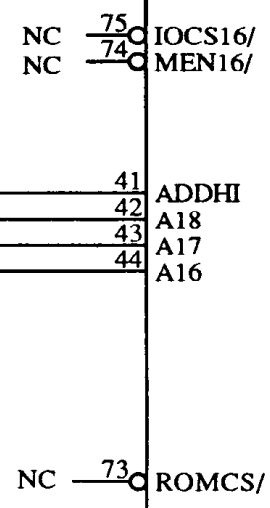
- 1) System Bus Interface
- 2) Display Memory Interface
- 3) Video Interface
- 4) Clock Interface



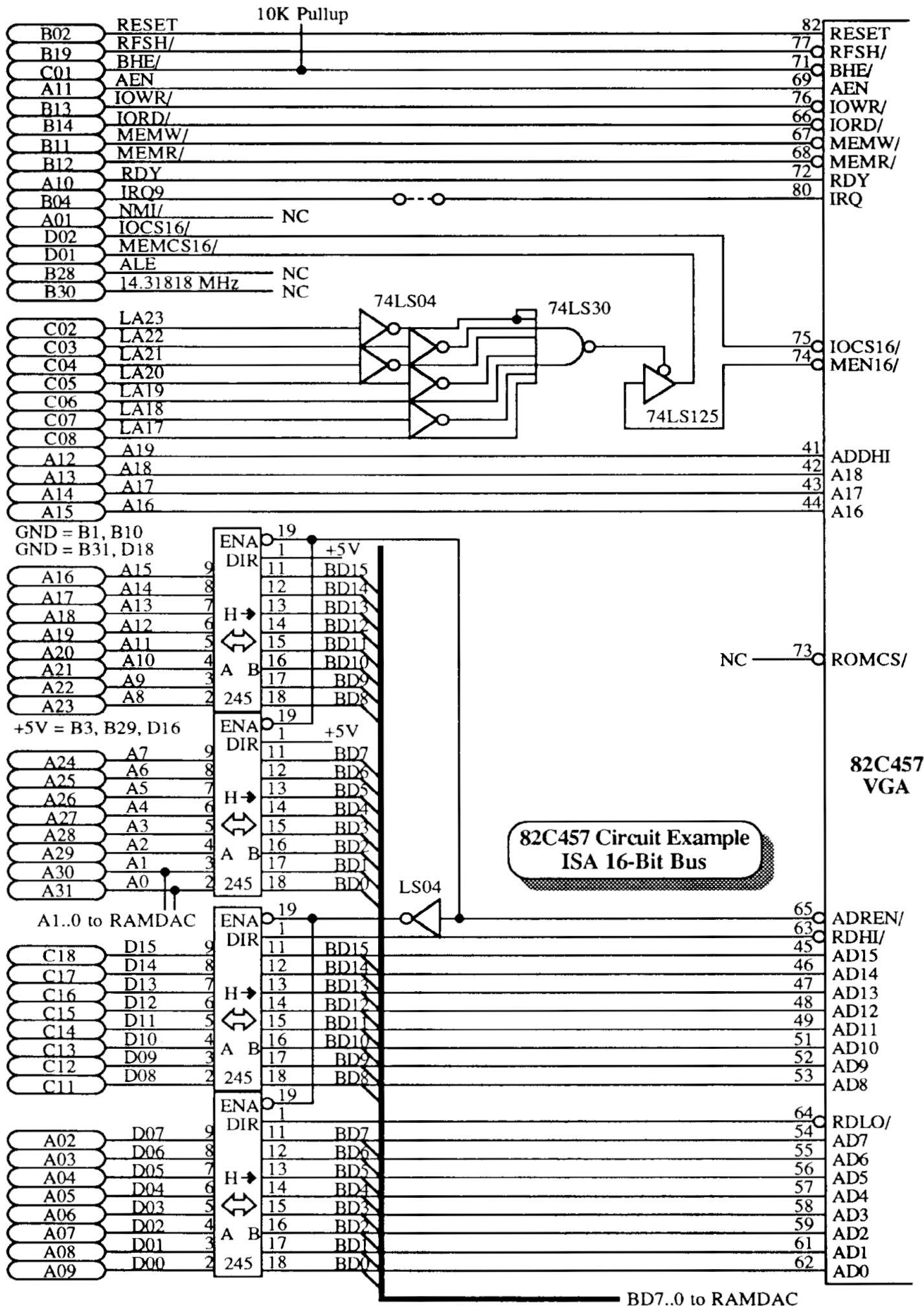
**82C457 Circuit Example  
ISA 8-Bit Bus**

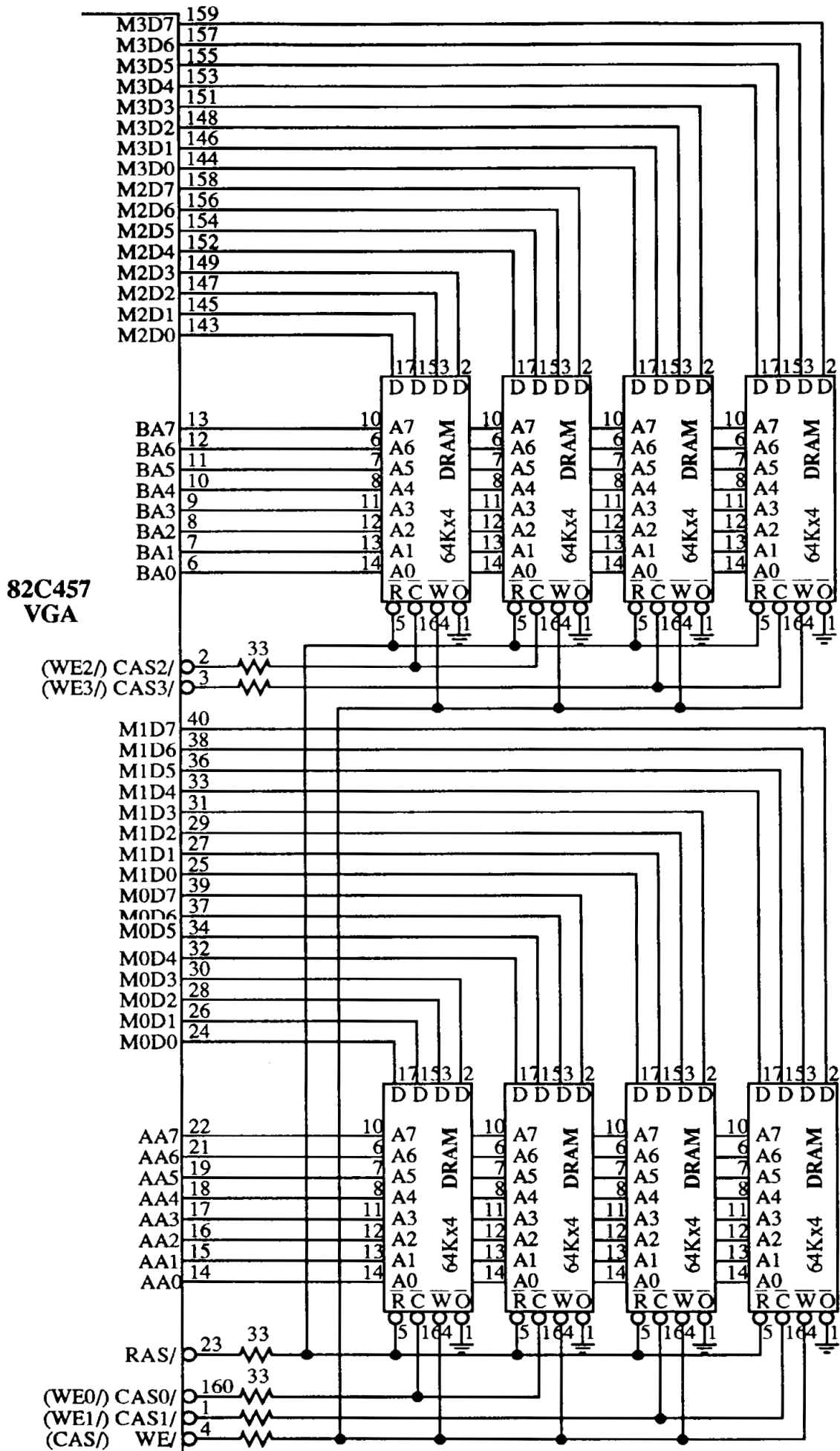


GND = B1, B10, B31  
+5V = B3, B29



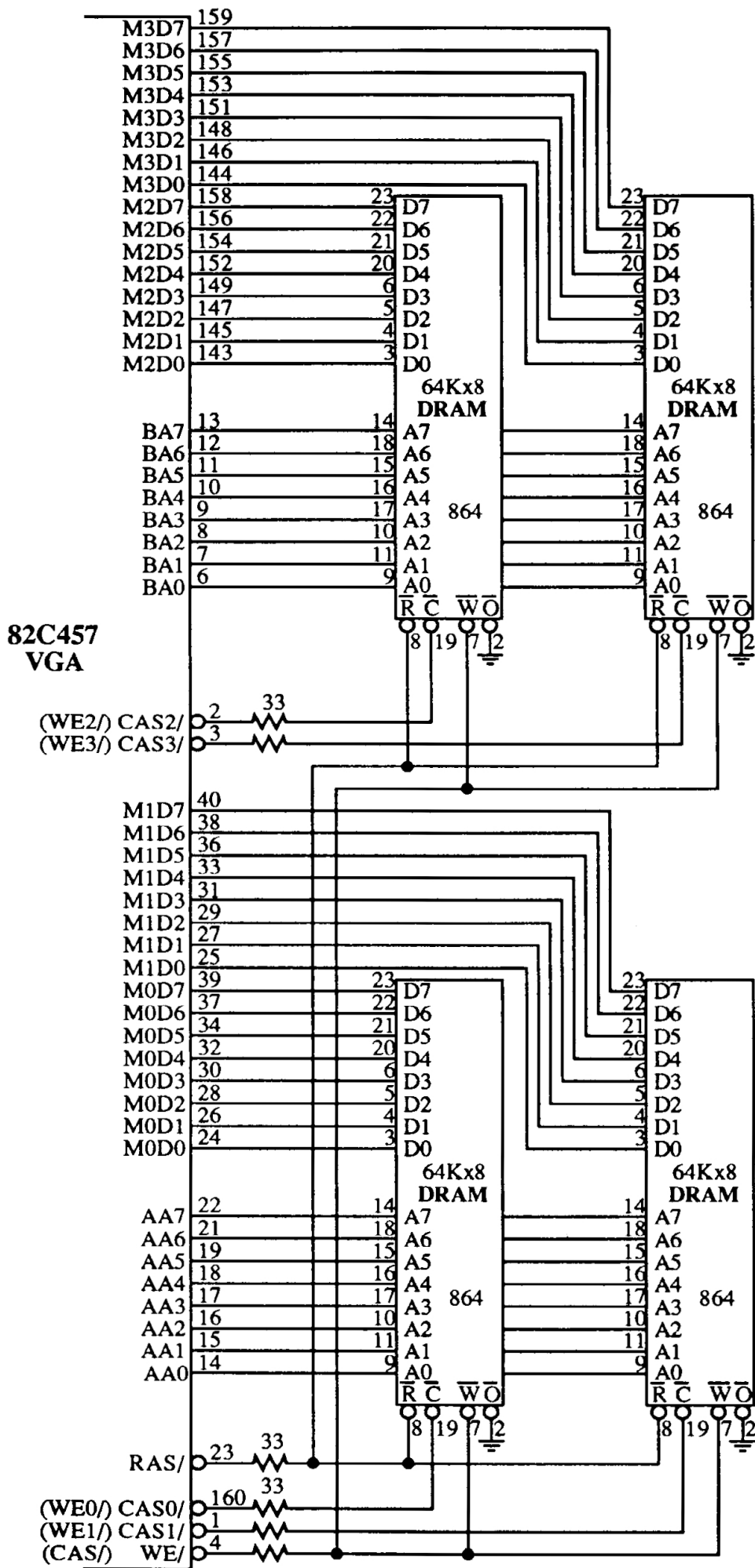
**82C457  
VGA**



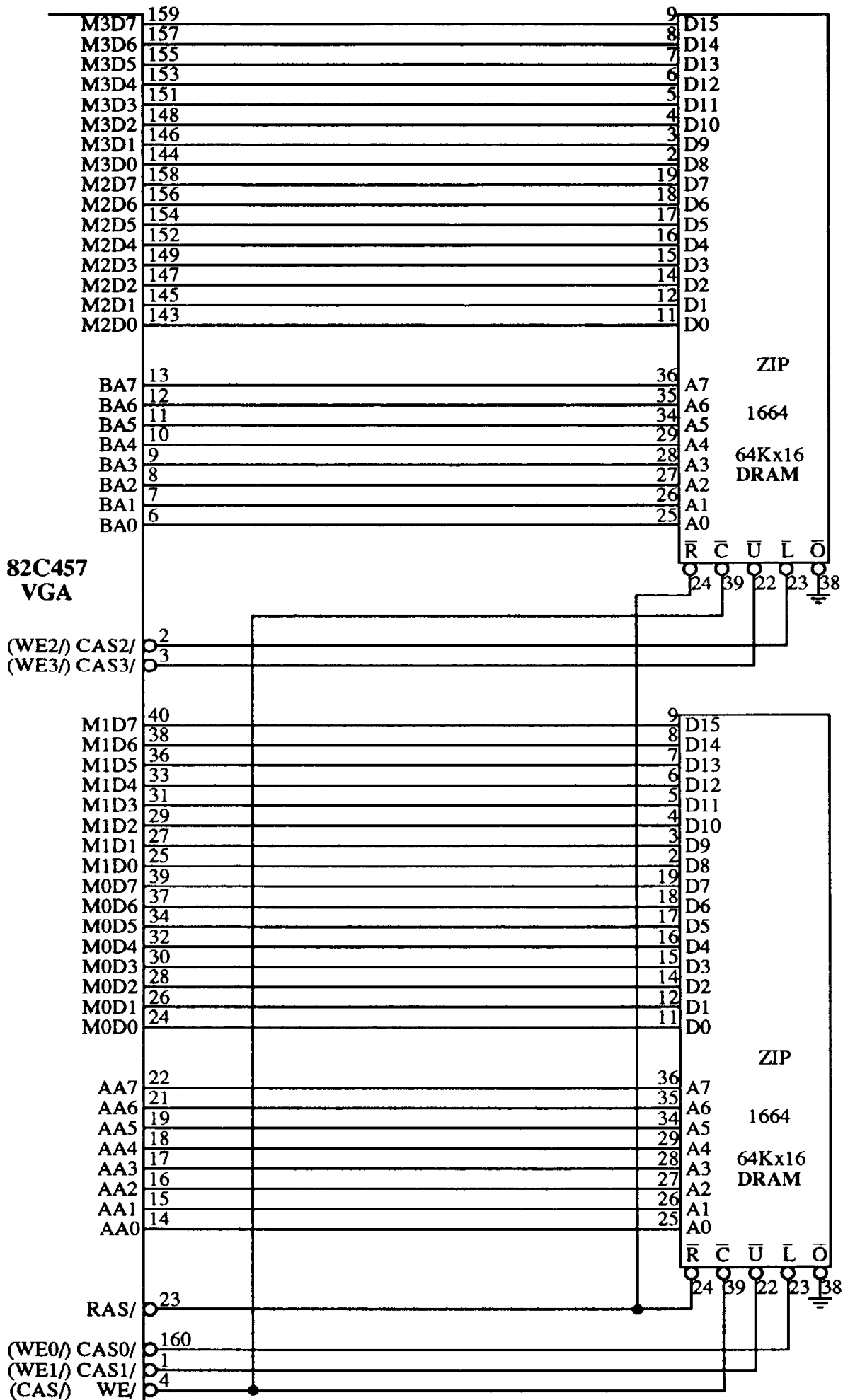


**82C457  
Display Memory  
Circuit  
64Kx4 DRAMs**

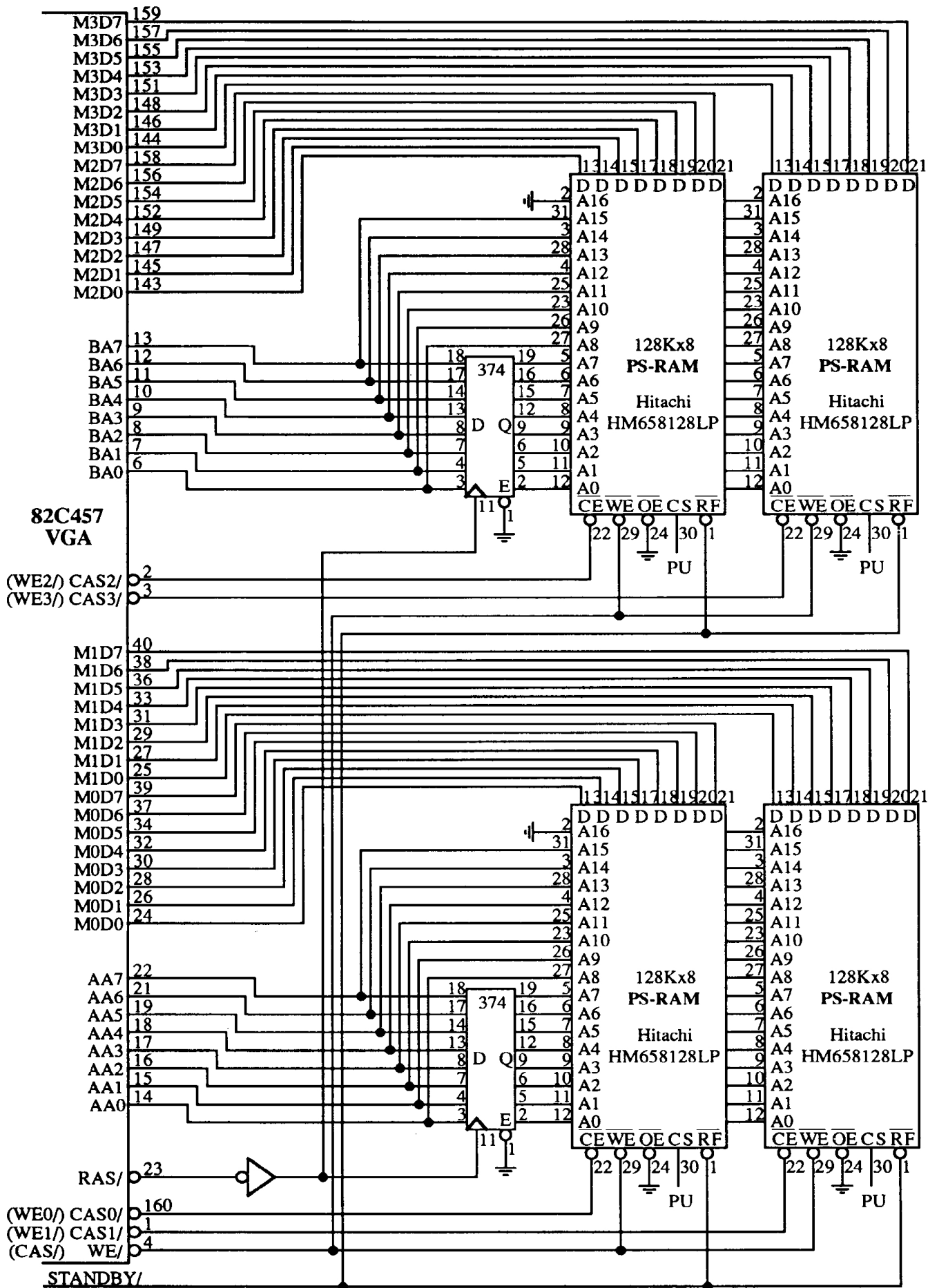




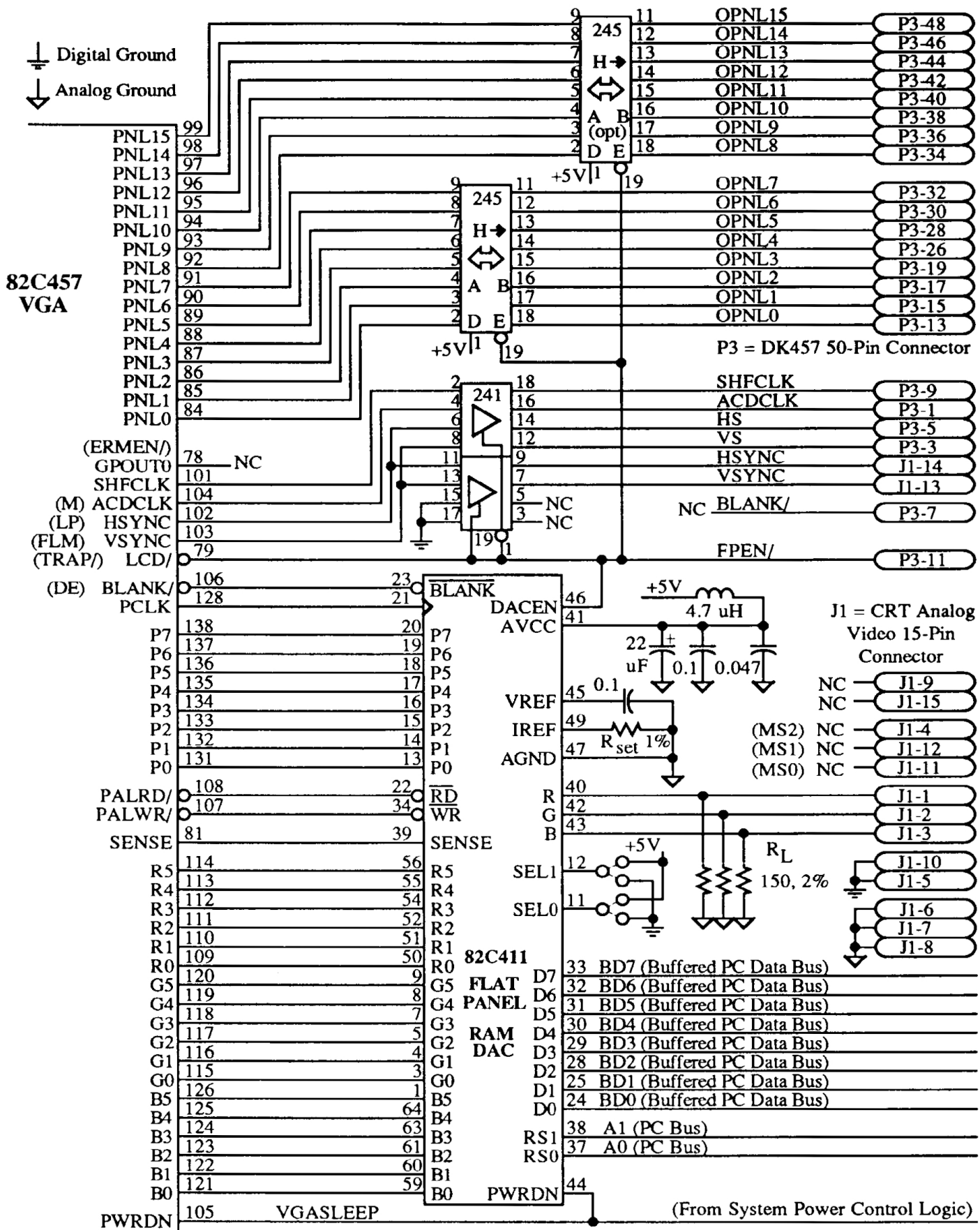
**82C457  
Display Memory  
Circuit  
64Kx8 DRAMs**



**82C457 Display Memory Circuit**  
**64Kx16 DRAMs**

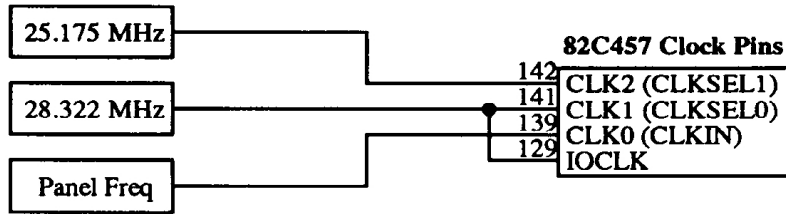


**82C457**  
**128Kx8**  
**Pseudo**  
**Static**  
**RAM**  
**Display**  
**Memory**  
**Circuit**

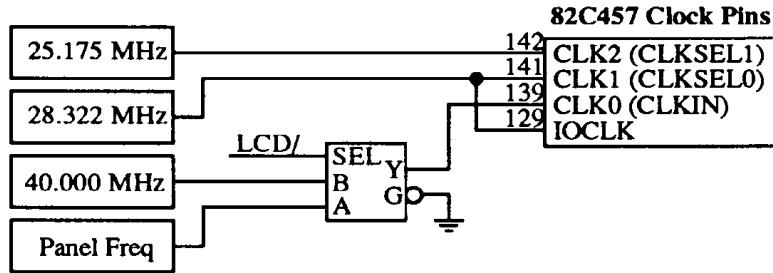


**82C457 Video Circuit Example  
For Color LCD Panels  
(Chips 82C411 Color Palette)**

Note: R<sub>set</sub> = 220Ω (assuming R<sub>L</sub> = 150Ω)  
 Note: Flat panel signals PNL8-15 are not needed for most color panels, so the buffer marked '(opt)' is not usually required.

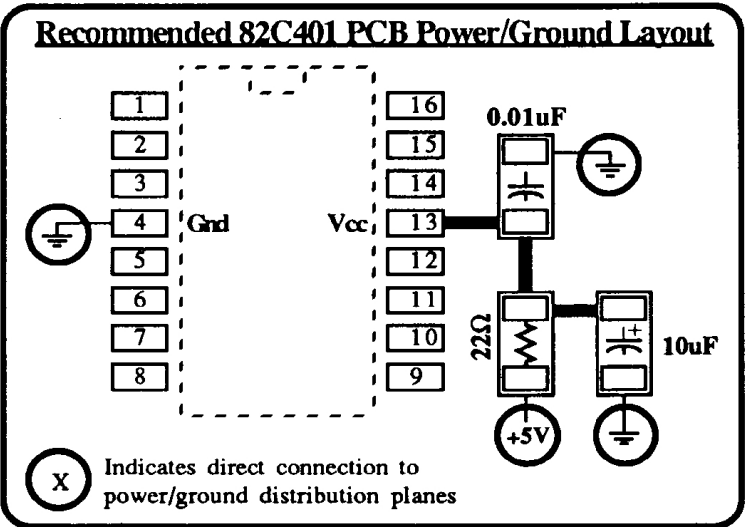
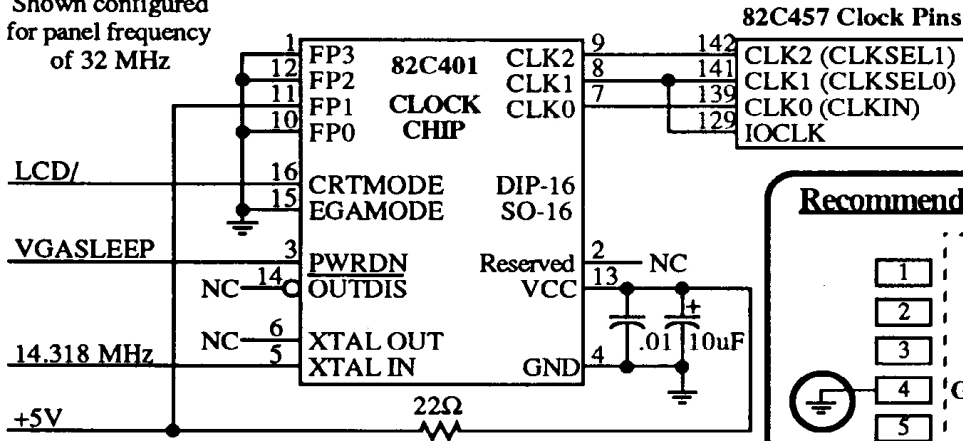


**82C457 Clock Circuit Example - Minimum Oscillator Configuration**



**82C457 Clock Circuit Example - Oscillator Configuration For High Res CRT Mode Support**

Shown configured for panel frequency of 32 MHz



**82C457 Clock Circuit Example - 82C401 Clock Chip Configuration**

# Electrical Specifications

## ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Units
$P_D$	Power Dissipation	–	1	W
$V_{CC}$	Supply Voltage	–0.5	7	V
$V_I$	Input Voltage	–0.5	$V_{CC}+0.5$	V
$V_O$	Output Voltage	–0.5	$V_{CC}+0.5$	V
$T_{OP}$	Operating Temperature (Ambient)	–25	85	°C
$T_{STG}$	Storage Temperature	–40	125	°C

**Note:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

## NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage	4.75	5.25	V
$T_A$	Ambient Temperature	0	70	°C
$T_C$	Case Temperature	0	85	°C

**Note:** Electrical specifications contained herein are preliminary and subject to change without notice.

## DC CHARACTERISTICS

(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
$I_{CC1}$	Power Supply Current	Normal @ 25 MHz CLK, 0°C	–	150	mA
$I_{CC2}$	Power Supply Current	(Retire Mode @ 25 MHz CLK, 0°C)	–	6	mA
$I_{IL}$	Input Leakage Current		–10	+10	uA
$I_{OZ}$	Output Leakage Current	High Impedance	–10	+10	uA
$V_{IL}$	Input Low Voltage		–0.5	0.8	V
$V_{IH}$	Input High Voltage	(All pins except clocks)	2.0	$V_{CC}+0.5$	V
		(CLK0, CLK1, CLK2, MCLK)	2.8	$V_{CC}+0.5$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 8$ mA (Note 1)	–	0.4	V
		$I_{OL} = 4$ mA (Note 2)	–	0.4	V
		$I_{OL} = 2$ mA (Note 3)	–	0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -8$ mA (Note 1)	2.4	–	V
		$I_{OH} = -4$ mA (Note 2)	2.4	–	V
		$I_{OH} = -2$ mA (Note 3)	2.4	–	V

**Note 1:** RDY, IRQ, TRAP/, ERMEN/, IOCS16/

**Note 2:** MEM16/, ERMEN/, M[3:0]D[7:0], WE/, CLK[2:0], PCLK, PALRD, PALWR, SHFCLK

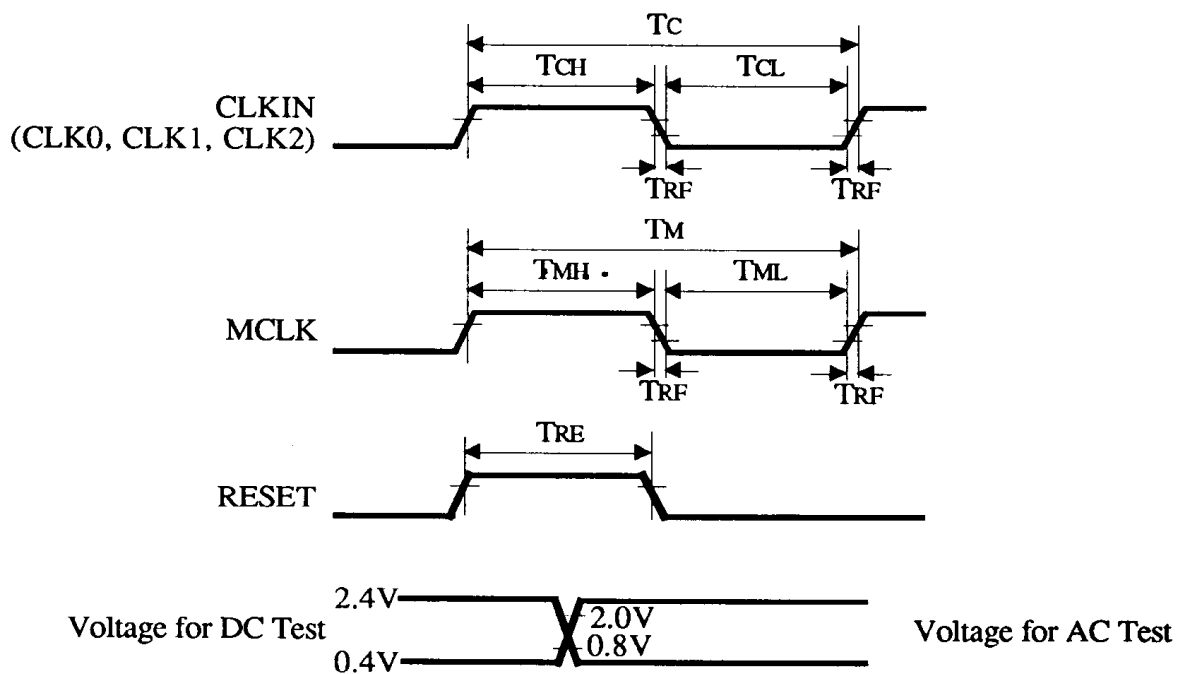
**Note 3:** ROMCS/, ADREN, RDLO, RDHI, AD[15:0], AA[7:0], BA[7:0], CAS[3:0]/, P[7:0], PNL[15:0], HSYNC, VSYNC, ACDCLK, BLANK/

### AC TIMING CHARACTERISTICS - CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
$T_C$	CLKIN Period	Panel Mode	31	–	–	ns
		CRT Mode	25	–	–	ns
$T_{CH}$	CLKIN High Time		$0.45T_C$	–	$0.55T_C$	ns
$T_{CL}$	CLKIN Low Time		$0.45T_C$	–	$0.55T_C$	ns
$T_M$	MCLK Period		30	35	40	ns
$T_{MH}$	MCLK High Time		$0.45T_M$	–	$0.55T_M$	ns
$T_{ML}$	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	ns
$T_{RF}$	CLKIN Rise/Fall		–	–	5	ns

### AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
$T_{RE}$	RESET High Time		$64 T_C$	–	–	ns



**Clock Timing**

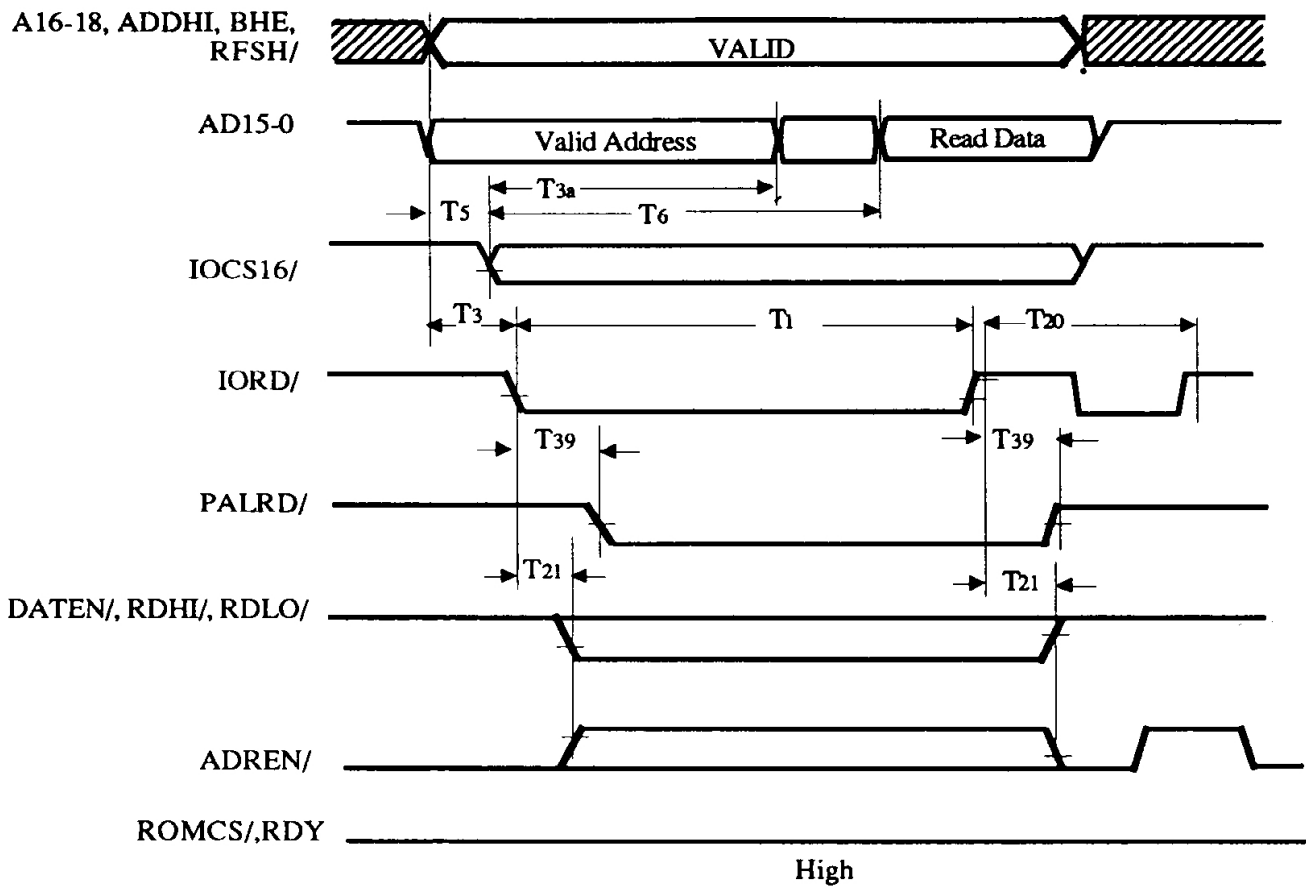
## AC TIMING CHARACTERISTICS - ISA (PC/AT) Bus Timing

Symbol	Parameter	Notes	Min	Typ	Max	Units
T <sub>1</sub>	IORD/, IOWR/ Pulse Width	Notes 4 & 5	175	–	–	ns
T <sub>2</sub>	MEMR/, MEMW/ Pulse Width	Note 5	175	–	–	ns
T <sub>3</sub>	Address setup to Read/Write		5	–	–	ns
T <sub>3a</sub>	Address hold from Read/Write Signal		10	–	–	ns
T <sub>5</sub>	IOCS16/ Delay from valid address		–	–	30	ns
T <sub>4</sub>	MEMR/, MEMW/ hold from RDY (Memory)		0	–	–	ns
T <sub>6</sub>	Data delay from IORD/		–	–	30	ns
T <sub>7</sub>	Data hold from IORD/		5	–	30	ns
T <sub>8</sub>	Data setup to IOWR/		5	–	–	ns
T <sub>9</sub>	Data hold from IOWR/		10	–	–	ns
T <sub>10</sub>	Data hold from MEMR/		5	–	30	ns
T <sub>11</sub>	Data hold from MEMW/		0	–	–	ns
T <sub>12</sub>	MEMR/, MEMW/ to RDY Low delay		–	–	25	ns
T <sub>13</sub>	Data setup to RDY		25	–	–	ns
T <sub>14</sub>	Data setup to RDY		40	–	–	ns
T <sub>15</sub>	RDY width		7T <sub>C</sub>	–	128T <sub>C</sub>	ns
T <sub>20</sub>	IORD/,IOWR/,MEMR/,MEMW/ cycle		7T <sub>M</sub>	–		ns
T <sub>21</sub>	ADREN/, DATEN/, RDHI/, RDLO/ I/O delay			–	16	ns
T <sub>39</sub>	PALRD/, PALWR/ delay from IORD/, IOWR/		–	–	25	ns

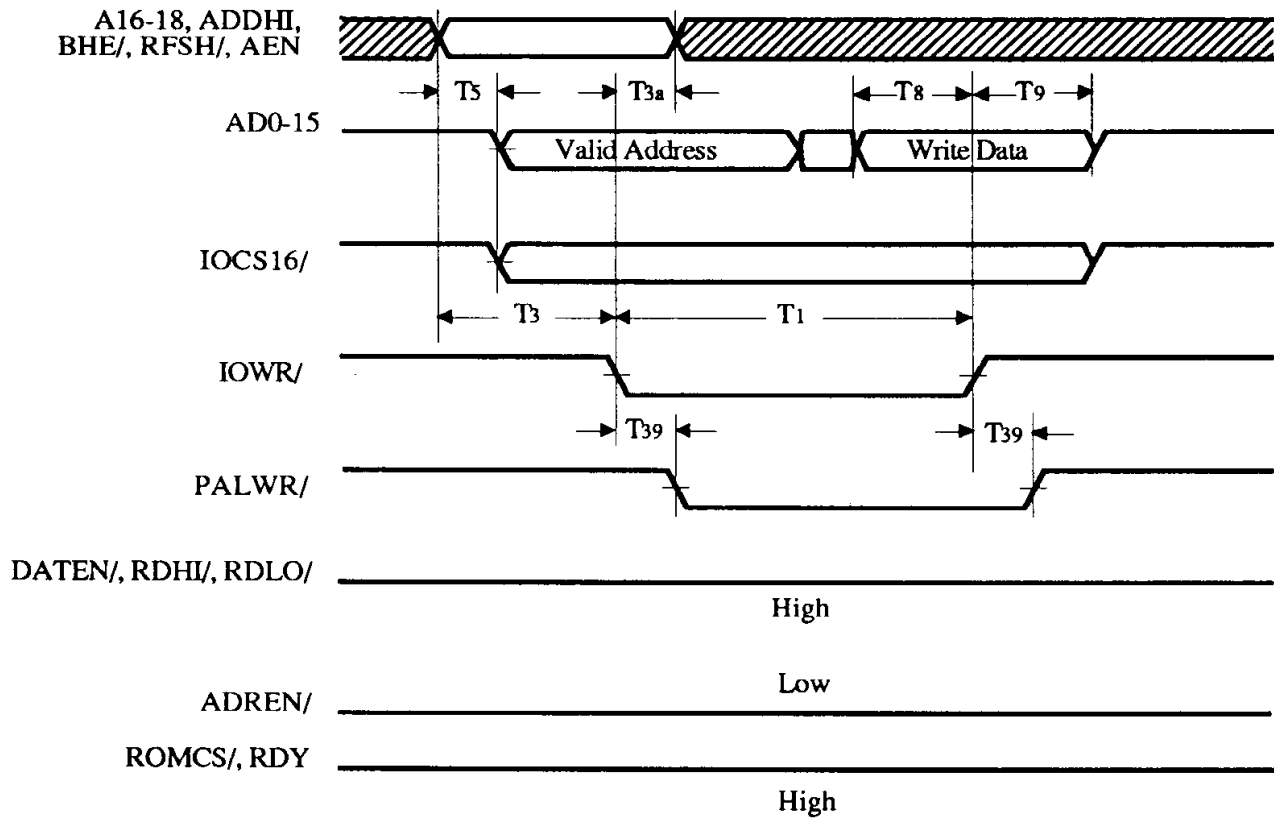
**Note 4:** A minimum IOWR pulse width of 3 MCLKs is required for access to an indexed register (ie. SR, CR, AR, GR, XR.)

**Note 5:** A minimum of 6 MCLKs is required from the falling edge of IOWR to the falling edge of MEMR/ or MEMW/.

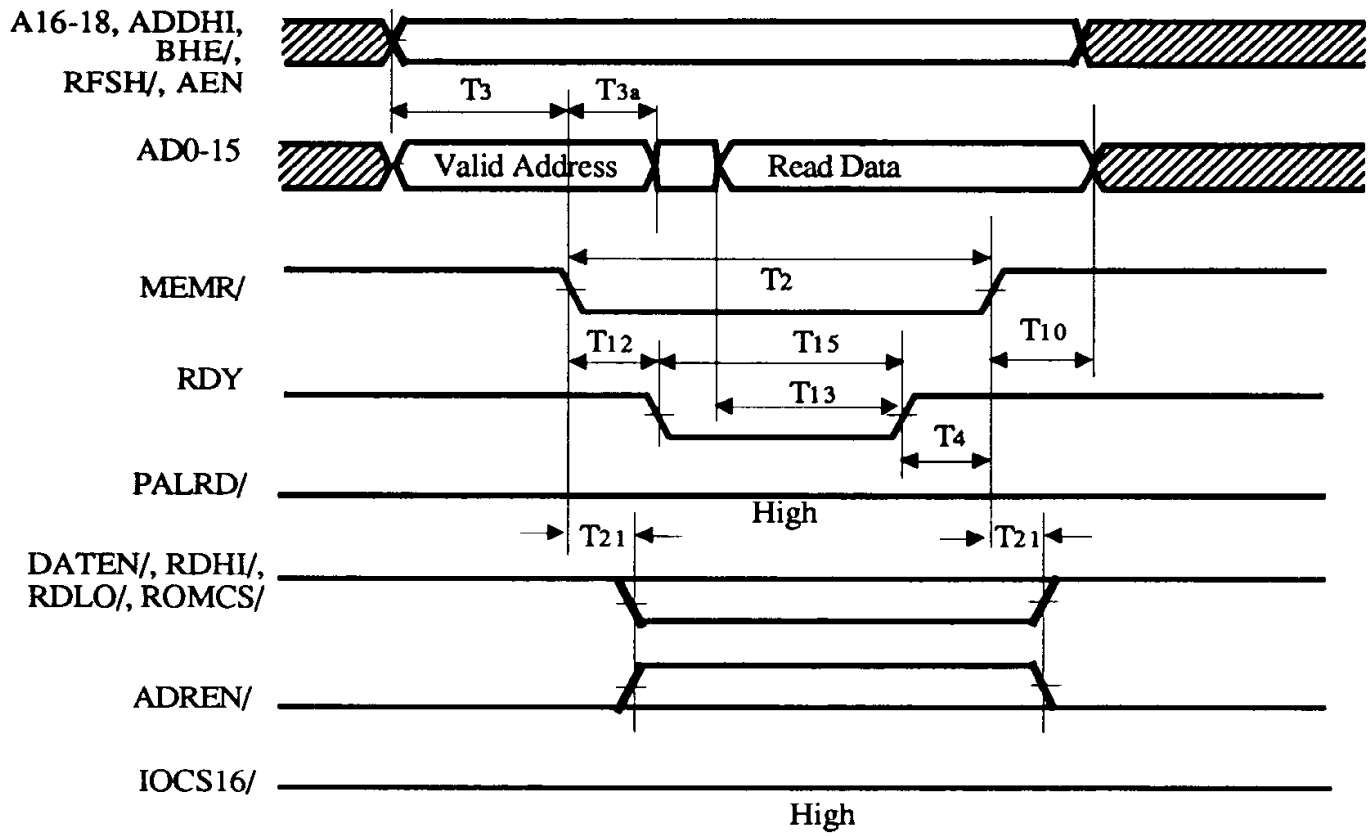




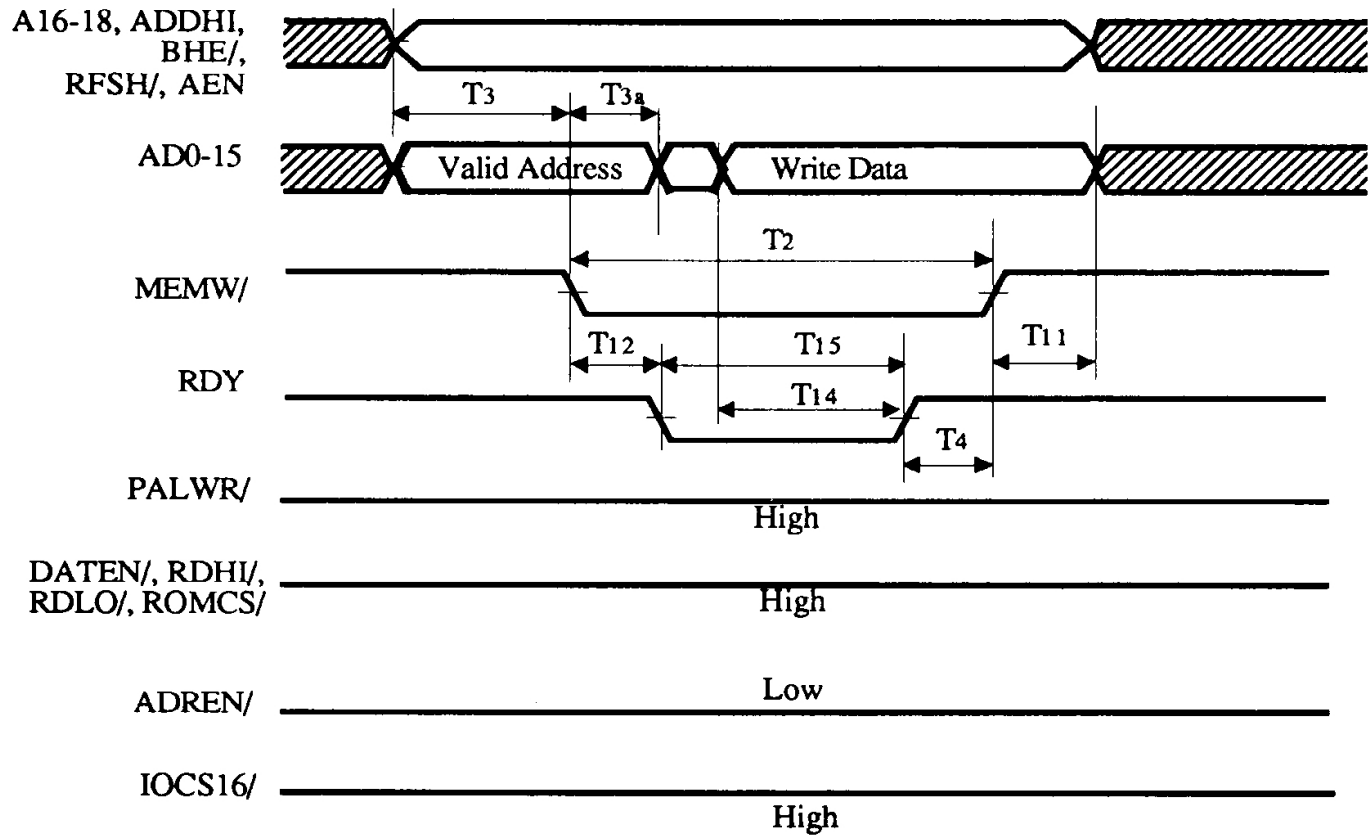
**Bus I/O Read Cycle Timing**



**Bus I/O Write Cycle Timing**



**Bus Memory Read Cycle Timing**



**Bus Memory Write Cycle Timing**

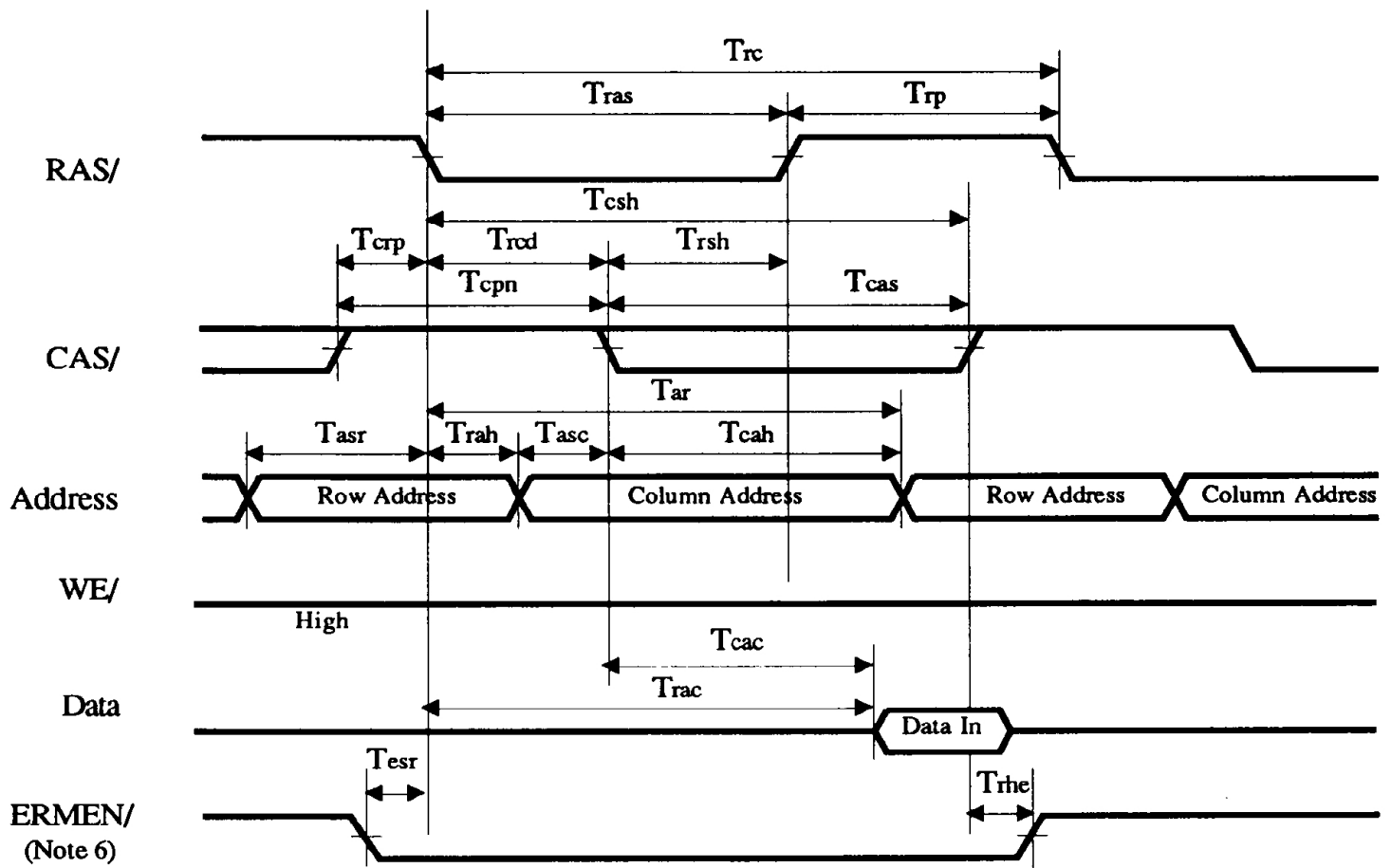
## AC TIMING CHARACTERISTICS - DRAM TIMING

Symbol	Parameter	8-dot Mode		9-dot Mode		Units
		Min	Max	Min	Max	
$T_{rc}$	Read/Write Cycle Time	$7T_c$	–	$8T_c$	–	ns
$T_{ras}$	RAS/ Pulse Width	$4T_c$	–	$4T_c$	–	ns
$T_{ar}$	Column Address Hold from RAS/	$5T_c$	–	$5T_c$	–	ns
$T_{rp}$	RAS/ Precharge	$3T_c$	–	$4T_c$	–	ns
$T_{crp}$	CAS/ to RAS/ precharge	$1T_c$	–	$2T_c$	–	ns
$T_{csh}$	CAS/ Hold from RAS/	$6T_c$	–	$6T_c$	–	ns
$T_{rcd}$	RAS/ to CAS/ delay	$2T_c$	–	$2T_c$	–	ns
$T_{rsh}$	RAS/ Hold from CAS/	$2T_c - 2$	–	$2T_c - 2$	–	ns
$T_{cpn}$	CAS/ Precharge	$3T_c$	–	$4T_c$	–	ns
$T_{cas}$	CAS/ Pulse Width	$4T_c$	–	$4T_c$	–	ns
$T_{asr}$	Row Address Setup to RAS/	$2T_c$	–	$3T_c$	–	ns
$T_{asc}$	Column Address Setup to CAS/	$1T_c$	–	$1T_c$	–	ns
$T_{rah}$	Row Address Hold from RAS/	$1T_c$	–	$1T_c$	–	ns
$T_{cah}$	Column Address Hold from CAS/	$3T_c$	–	$3T_c$	–	ns
$T_{cac}$	Data Access Time from CAS/	--	$3T_c$	–	$3T_c$	ns
$T_{rac}$	Data Access Time from RAS/	--	$5T_c$	–	$5T_c$	ns
$T_{wp}$	WE/ Pulse Width	$7T_c - 5$	–	$8T_c - 5$	–	ns
$T_{ds}$	Write Data Setup to CAS/	$2T_c$	–	$2T_c$	–	ns
$T_{dh}$	Write Data Hold from CAS/	$5T_c$	–	$6T_c$	–	ns
$T_{dhr}$	Write Data Hold from RAS/	$7T_c$	–	$8T_c$	–	ns
$T_{wch}$	WE/ Hold from CAS/	$5T_c - 5$	–	$6T_c - 5$	–	ns
$T_{wcs}$	WE/ Setup to CAS/	$2T_c$	–	$2T_c$	–	ns
$T_{rwl}$	WE/ Lead to RAS/	$4T_c$	–	$4T_c$	–	ns
$T_{cwl}$	WE/ Lead to CAS/	$6T_c$	–	$6T_c$	–	ns
$T_{wcr}$	WE/ Hold from RAS/	$7T_c$	–	$8T_c$	–	ns

## AC TIMING CHARACTERISTICS - DRAM REFRESH TIMING

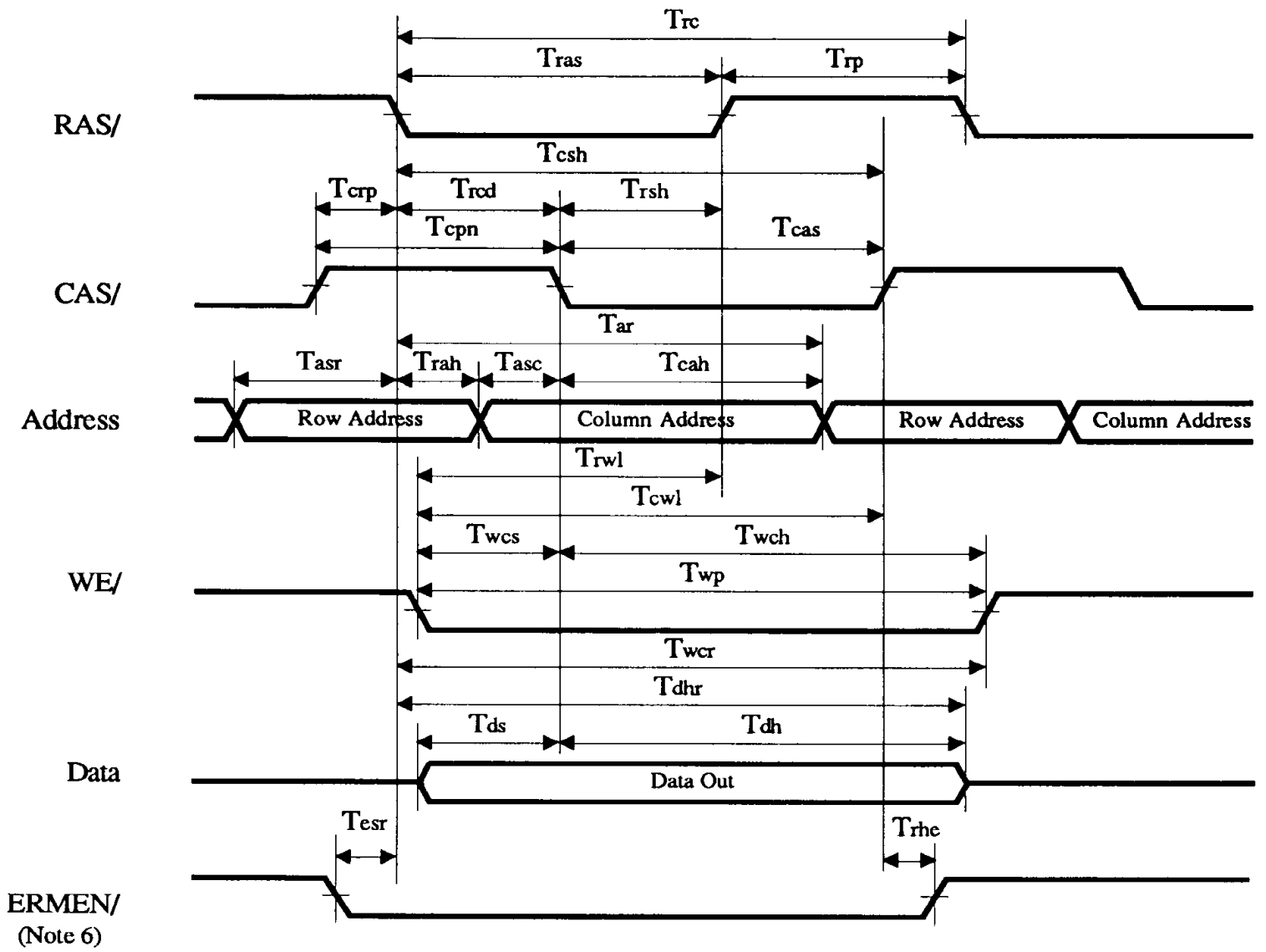
Symbol	Parameter	Max	Units
–	DRAM Refresh interval	$85000/(VR*VL)$	ns

**Note:** VR = Vertical refresh rate (in Hz.)  
 VL = Total number of lines per frame (including retrace)



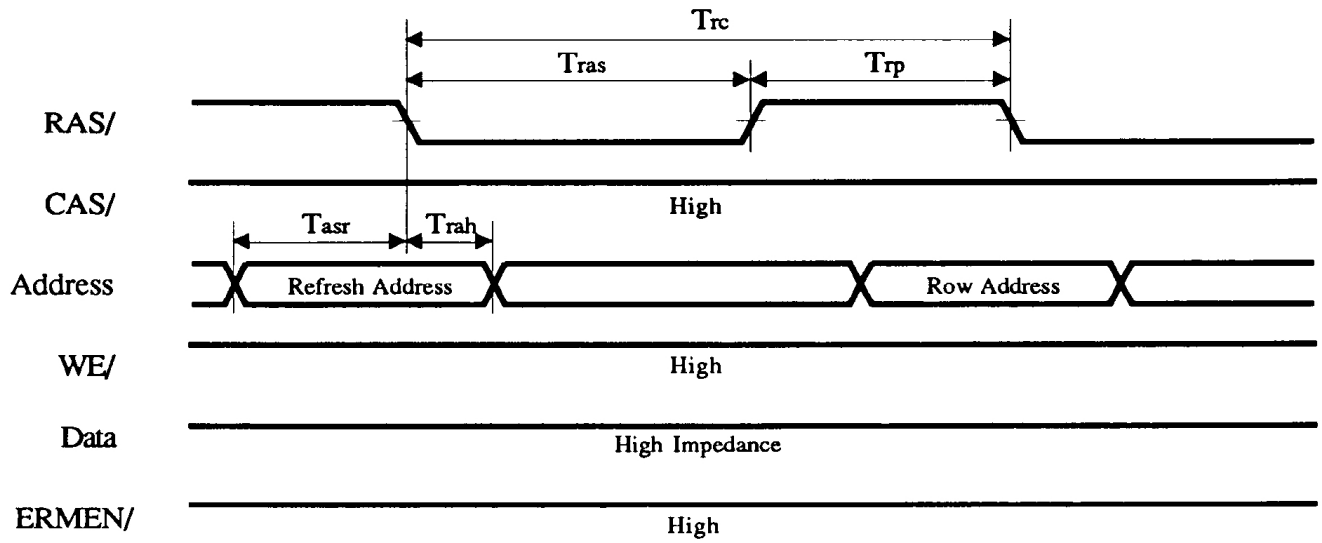
**Note 6:** ERMEN/ is active (low) only during CPU memory cycles

**DRAM Read Cycle Timing**



**Note 6:** ERMEN/ is active (low) only during CPU memory cycles

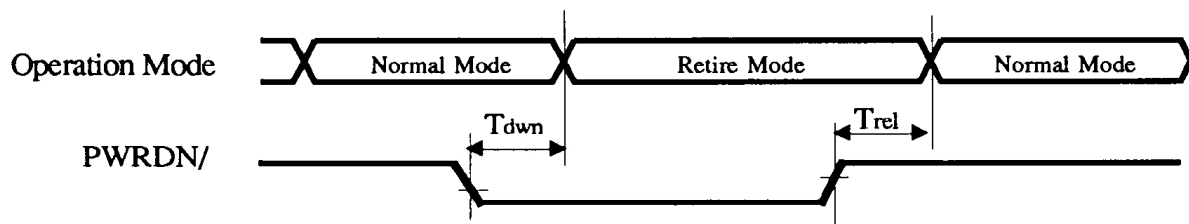
**DRAM Write Cycle Timing**



### DRAM Refresh Cycle Timing

### AC TIMING CHARACTERISTICS - POWERDOWN

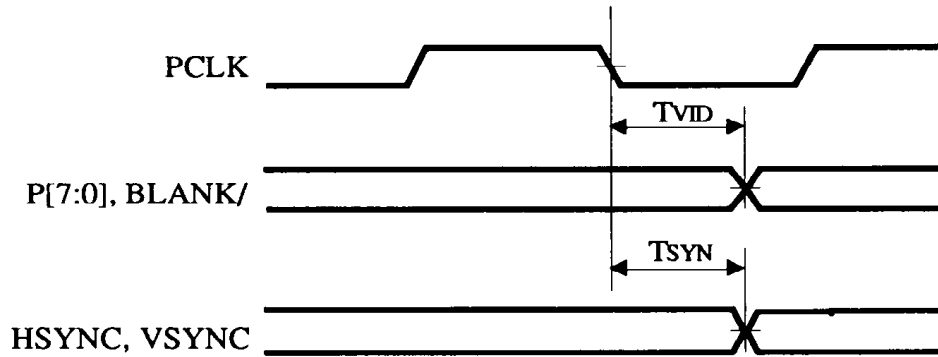
Symbol	Parameter	Min	Max	Units
$T_{dwn}$	PWRDN setup into Retire mode	$3T_c$	$10T_c$	ns
$T_{rel}$	PWRDN setup into Normal mode	$2T_c$	1 refresh cycle	ns



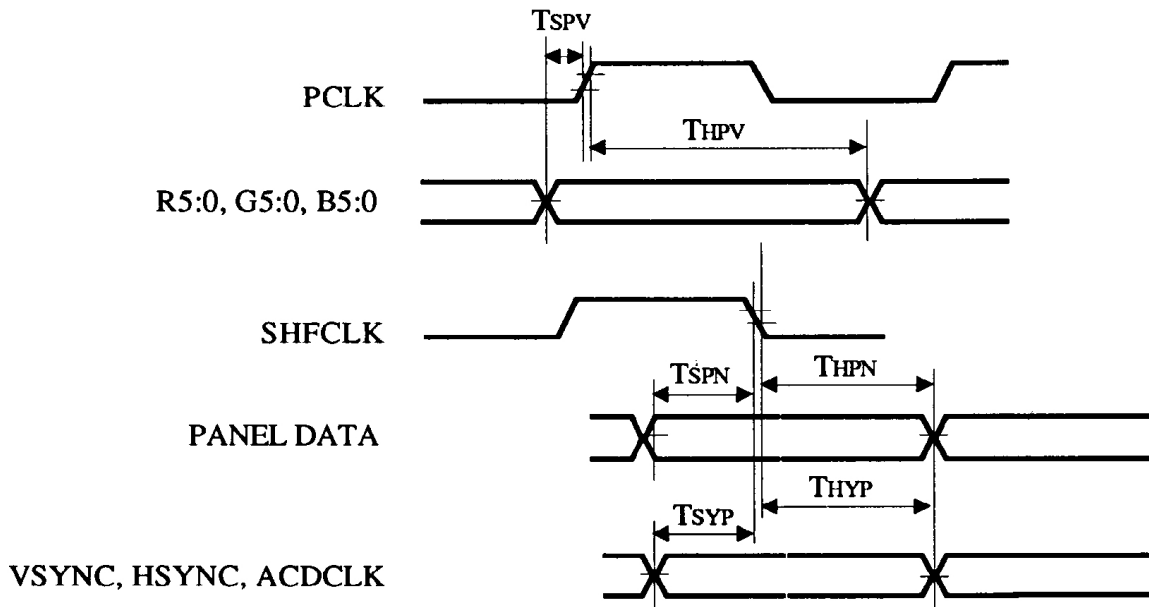
### Retire Mode Timing

## AC TIMING CHARACTERISTICS - VIDEO TIMING

Symbol	Parameter	Notes	Min	Max	Units
$T_{VID}$	Video delay from PCLK		–	25	ns
$T_{SYN}$	HSYNC, VSYNC, BLANK/ delay from PCLK	CRT mode	–	20	ns
$T_{SPV}$	R5:0, G5:0, B5:0 setup to PCLK rising edge	FP mode	2	–	ns
$T_{HPV}$	R5:0, G5:0, B5:0 hold to PCLK rising edge	FP mode	10	–	ns
$T_{SPN}$	PNL[15:0] setup to SHFCLK	FP mode	5	–	ns
$T_{HPN}$	PNL[15:0] hold to SHFCLK	FP mode	10	–	ns
$T_{SYP}$	HSYNC, VSYNC, ACDCLK setup to SHFCLK	FP mode	5	–	ns
$T_{HYP}$	HSYNC, VSYNC, ACDCLK hold to SHFCLK	FP mode	10	–	ns



**CRT Display Mode Timing**



**Flat Panel Display Mode Timing**





## **Chips & Technologies 82C455, 82C456, and 82C457 Related Document Files**

(Extracted)

- [82C455 Datasheet](#)
- [82C456 Datasheet](#)
- [Development History](#) of 82C455, 82C456, and 82C457
- 82C457 [TDL Netlist](#)
- 82C457 [TDL Macrocells](#)
- 82C457 [Demo System](#)