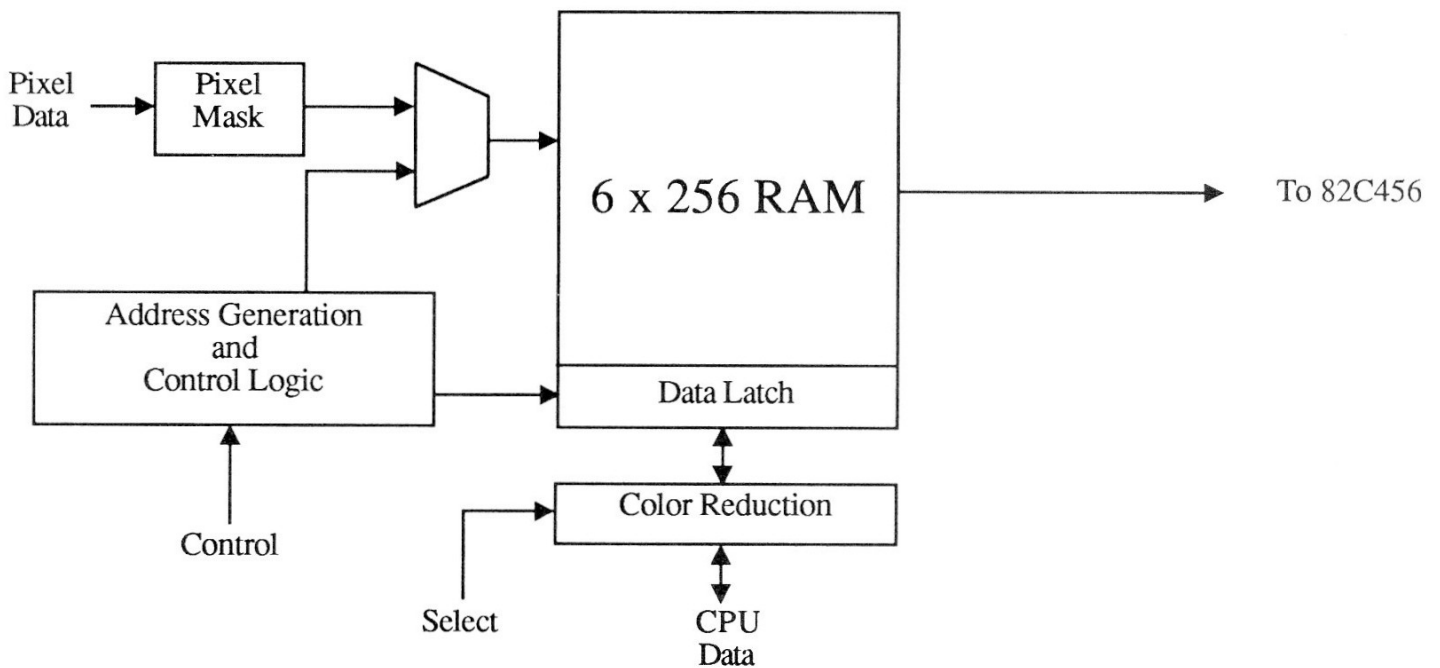# 82C460
Flat Panel Color Palette

- Flat Panel Digital Palette

- Provides full VGA compatibility on flat panels

- Direct connection to Chips & Technologies 82C456 Enhanced Flat Panel/CRT VGA controller

- Three RGB to Grayscale reduction techniques

- 64 Gray levels for monochrome panels

- 64 Colors for color panels

- All Flat Panel palette functions integrated in a single package

- Supports LCD, Plasma, and Electro Luminescent flat panels

82C460 BLOCK DIAGRAM

Introduction

The 82C460 Flat Panel Palette is designed to provide the external color palette data to the 82C456 for processing and display on the flat panel. The CPU interface is identical to that of an Inmos IMSG176 style RAMDAC. The 82C460 is used in parallel with the standard RAMDAC. All CPU address and data information is monitored by the 82C460.

The palette read and write signals pass through the 82C460 allowing selective reading and writing of the two palettes. Separate write enables are provided for each palette. A single read select is provided to determine which palette is read by the CPU.

During CPU writes to the external color palette, the 82C460 latches the color data as it is written to the color palette. After the blue data is written to the storage latch, the 82C460 reduces the data to 6 bits (64 color or gray levels) and then writes it to the palette RAM.

During display, the pixel input data is used as an address to the palette RAM. The RAM data is then output for processing by the 82C456.

Reduction Techniques

Four reduction algorithms are provided to reduce the 18 bit RGB data to 6 bits. The reduction algorithms are as follows:
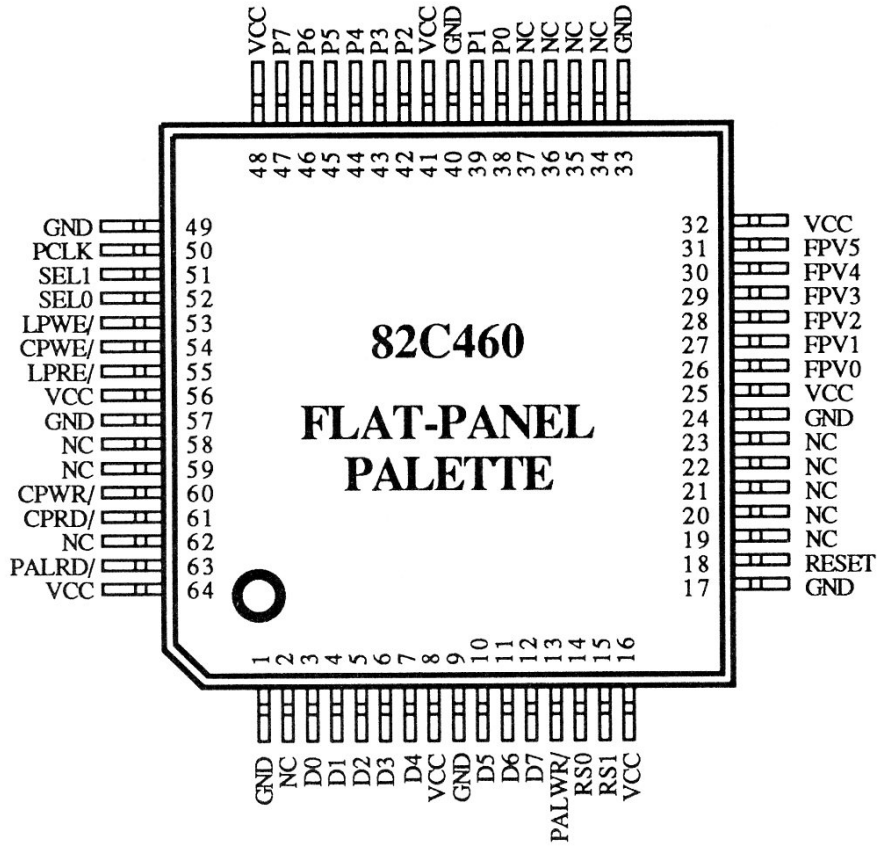
NTSC: This is the industry standard technique for reducing RGB color information to gray levels. The weighting is $5/16R + 9/16G + 1/8B$. The data is reduced in a two stage adder and the 6 most significant bits are stored. This technique is selected when the select bits are both 0 (SEL1:0=00).

EQUAL: In this technique the RGB values are equally weighted. The reduction is $5/16R + 3/8G + 5/16B$. This technique is used when SEL1:0 = 01

GREEN only: This reduction type stores only the green (G) value. This produces the same display as an IBM monochrome CRT. This is used when SEL1:0 = 10.

COLOR: When SEL1:0 = 11, the two most significant bits of each color are stored without modification. This is used for displaying 64 colors on RGB color panels.

82C460 Pinouts

82C460
FLAT-PANEL
PALETTE

Left side (top to bottom):
GND — 49
PCLK — 50
SEL1 — 51
SEL0 — 52
LPWE/ — 53
CPWE/ — 54
LPRE/ — 55
VCC — 56
GND — 57
NC — 58
NC — 59
CPWR/ — 60
CPRD/ — 61
NC — 62
PALRD/ — 63
VCC — 64

Right side (top to bottom):
32 — VCC
31 — FPV5
30 — FPV4
29 — FPV3
28 — FPV2
27 — FPV1
26 — FPV0
25 — VCC
24 — GND
23 — NC
22 — NC
21 — NC
20 — NC
19 — NC
18 — RESET
17 — GND

Top (pins 48–33): VCC, P7, P6, P5, P4, P3, P2, VCC, GND, P1, P0, NC, NC, NC, NC, GND

Bottom (pins 1–16): GND, NC, D0, D1, D2, D3, D4, VCC, GND, D5, D6, D7, PALWR/, RS0, RS1, VCC

82C460 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
50	PCLK	In	Both	PIXEL CLOCK. The rising edge samples and latches the Pixel Address inputs. It controls progress of the data through the four stage pipeline to the Flat Panel Palette to the outputs.
47	P7	In	Both	PIXEL DATA. The input address to the Flat Panel Palette RAM.
46	P6	In	Both	
45	P5	In	Both	
44	P4	In	Both	
43	P3	In	Both	
42	P2	In	Both	
39	P1	In	Both	
38	P0	In	Both	
31	FPV5	Out	Both	FLAT PANEL VIDEO. The outputs of the Flat Panel Palette RAM as addressed by the Pixel Address.
30	FPV4	Out	Both	
29	FPV3	Out	Both	
28	FPV2	Out	Both	
27	FPV1	Out	Both	
26	FPV0	Out	Both	
13	PALWR/	In	Low	PALETTE WRITE ENABLE. This signal is used for CPU writes to the external color palette. RS 1:0 are latched on the falling edge and D7:0 on the rising edge during an CPU write operation.
63	PALRD/	In	Low	PALETTE READ ENABLE. This signal is used for CPU reads from the external color palette. RS 1:0 are latched on the falling edge. The data is presented when this signal is low.
15	RS1	In	Both	REGISTER SELECT 1 & 0. These two lines are sampled during the falling edges of the enable signals (PALWR/ or PALRD/) and select one of the three internal registers.
14	RS0	In	Both	

RS1	RS0	REGISTER
0	0	Address Register (RAM Write Mode)
1	1	Address Register (RAM Read Mode)
0	1	Palette RAM
1	0	Pixel Mask Register

82C460 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
12	D7	I/O	Both	PALETTE DATA. Read/write data to the internal
11	D6	I/O	Both	registers. During the write cycle, the rising edge of
10	D5	I/O	Both	PALWR/ latches the data into the selected register.
7	D4	I/O	Both	When PALRD/ is inactive (high) the data I/O lines will
6	D3	I/O	Both	be 3-stated.
5	D2	I/O	Both	
4	D1	I/O	Both	
3	D0	I/O	Both	
51	SEL1	In	Both	SELECT 1 & 0. These signals select the algorithm used
52	SEL0	In	Both	to reduce the RGB data before it is stored in the Flat Panel Palette RAM. The four algorithms are:

SEL1	SEL0	RAM Data Mode
0	0	NTSC Weighting
0	1	Equivalent
1	0	GREEN only
1	1	Color

Pin #	Pin Name	Type	Active	Description
53	FPWE/	In	Low	FLAT PANEL PALETTE WRITE ENABLE. This signal, when low, allows writes to occur to the Flat Panel Palette RAM.
54	CPWE/	In	Low	COLOR PALETTE WRITE ENABLE. This signal, when low, allows the CPWR/ output to go active (low) during palette write cycles (PALWR/ low)
55	FPRE/	In	Low	FLAT PANEL PALETTE READ ENABLE. This signal, when low, selects reads to occur from the Flat Panel Palette. If the signal is low, the CPRD/ is not active and read cycles are handled by the 82C460. When high, the 82C460 does not arrive data on the data outputs and the CPRD/ signal will be active for palette read cycles.
61	CPRD/	Out	Low	COLOR PALETTE READ. This signal is active during palette read cycles if the FPRE/ pin is high.
60	CPWR/	Out	Low	COLOR PALETTE WRITE. This signal is active during palette write cycles if the CPWE/ pin is low.

82C460 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
18	RESET	In	High	RESET. The RESET signal should be brought high after power is applied.
8 16 25 37 41 48 56 64	VCC	In	-	POWER
1 9 17 24 33 40 49 57	GND	In	-	GROUND
2 19 20 21 22 23 34 35 36 37 58 59 62	NC	-	-	NO CONNECTION. These pins are reserved for future expansion. They should be left floating.

Application Schematic Example

Read / Write Strobes
To Color Palette DAC

82C456 VGA		82C460		
	61	CPRD	FPRE	55 — +5V
	60	CPWR	FPWE	53
			CPWE	54
PALRD/	107 63	PALRD		
PALWR/	106 13	PALWR		
PCLK	98 50	PCLK		
P7	101 47	P7	SEL1	51 — +5V
P6	100 46	P6	SEL0	52
P5	99 45	P5		
P4	97 44	P4		
P3	96 43	P3		
P2	95 42	P2		
P1	94 39	P1		
P0	93 38	P0		
FPV5	89 31	FPV5		
FPV4	88 30	FPV4		
FPV3	87 29	FPV3		
FPV2	86 28	FPV2		
FPV1	85 27	FPV1		
FPV0	84 26	FPV0		

BD7 (Buffered PC Data Bus)	12	D7
BD6 (Buffered PC Data Bus)	11	D6
BD5 (Buffered PC Data Bus)	10	D5
BD4 (Buffered PC Data Bus)	7	D4
BD3 (Buffered PC Data Bus)	6	D3
BD2 (Buffered PC Data Bus)	5	D2
BD1 (Buffered PC Data Bus)	4	D1
BD0 (Buffered PC Data Bus)	3	D0

| A1 (PC Bus) | 15 | RS1 |
| A0 (PC Bus) | 14 | RS0 |

| RESET (PC Bus) | 18 | RESET |

SEL1	SEL0	Mode
0	0	NTSC
0	1	Equal Weighting
1	0	Green Only
1	1	Color

Note: NTSC generally works best for most applications.

82C456 Video Circuit Example - 82C460 Support Chip

82C460 Electrical Specifications

82C460 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power Dissipation	P_D	--	500	mW
Supply Voltage	V_{CC}	-0.5	7.0	V
Input Voltage	V_I	-0.5	V_{CC}+0.5	V
Output Voltage	V_O	-0.5	V_{CC}+0.5	V
Operating Temperature (Ambient)	T_{OP}	-25	85	°C
Storage Temperature	T_{STG}	-55	150	°C
Output Current	I_0	-20	20	mA

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C460 Normal Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C
Case Temperature	T_C	0	85	°C

82C460 DC Characteristics   (Under Normal Operating Conditions Unless Noted Otherwise)

Parameter	Notes	Symbol	Min	Typ	Max	Units
Power Supply Current		I_{CC}	--	20	--	mA
Input Leakage Current		I_{IL}	−10	--	+10	uA
Output Leakage Current	(High Impedance)	I_{OZ}	−10	--	+10	uA
Input Low Voltage		V_{IL}	--	--	$V_{CC} * 0.3$	V
Input High Voltage		V_{IH}	$V_{CC} * 0.7$	--	--	V
Output Low Voltage	I_{OL} = - 4mA	V_{OL}	--	--	0.4	V
Output High Voltage	I_{OH} = 4mA	V_{OH}	V_{CC}-0.6	--	--	V
Capacitance, Input or Output		C	--	10	20	pF

Electrical specifications contained herein are preliminary and subject to change without notice.
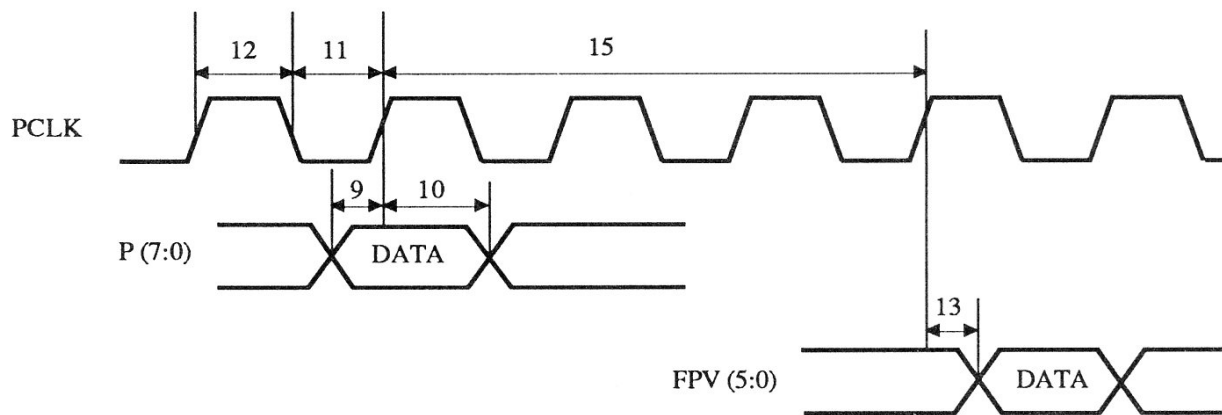
82C460 AC Timing Characteristics - CPU Interface

Parameter	Symbol	Min(ns)	Max(ns)
RS0, RSI Setup Time	1	10	--
RS0, RSI, Hold Time	2	10	--
PALRD/ to Data Valid	3	--	45
PALRD/ Negated to Data Bus 3-Stated	4	5	--
Write Data Setup Time	5	10	--
Write Data Hold Time	6	10	--
PALRD/, PALWR/ Pulse Width Low	7	50	--
PALRD/ Pulse Width High	8	4 * PCLK	--
PALWR/ Pulse Width High	14	5 * PCLK	--
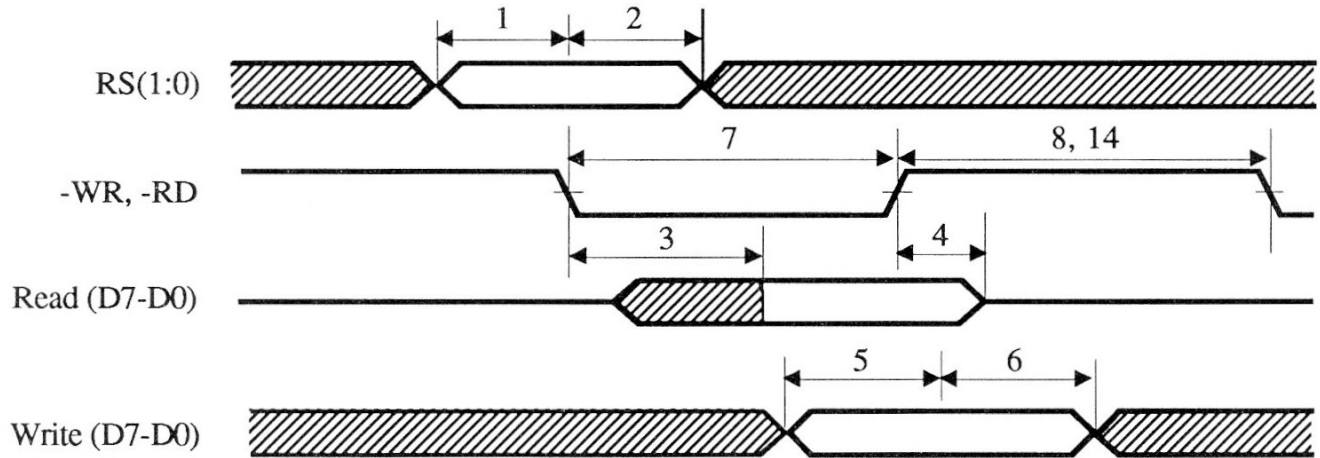
82C460 CPU Timing

82C460 AC Timing Characteristics - Output Timing

Parameter	Symbol	Min(ns)	Max(ns)
Pixel Setup Time	9	4	--
Pixel Hold Time	10	4	--
Clock Pulse Width Low Time	11	16	--
Clock Pulse Width High Time	12	16	--
PCLK to Valid FPV-out	13	5	21
P-in to FPV-out delay	15	4*PCLK	4*PCLK

82C460 Output Timing

82C460 Mechanical Specifications

64-Pin Plastic Flat Pack
82C460

Lead Pitch
1.016 (0.04)

Lead Width
0.4 ±0.1
(0.016 ±0.004)

Lead Length
0.85 ±0.3
(0.033 ±0.012)

Pin 1

Body Size
18.0 ±0.2 (0.709 ±0.008)

Footprint 22.0 ±0.4
(0.866 ±0.016)

Body Size
18.0 ±0.2 (0.709 ±0.008)

Footprint 22.0 ±0.4
(0.866 ±0.016)

Lead Length
0.85 ±0.3
(0.033 ±0.012)

DIMENSIONS:
mm (in)

Clearance
0.1 ± 0.1
(0.004 ±0.004)

Max Height
2.8 (0.110)

Seating Plane