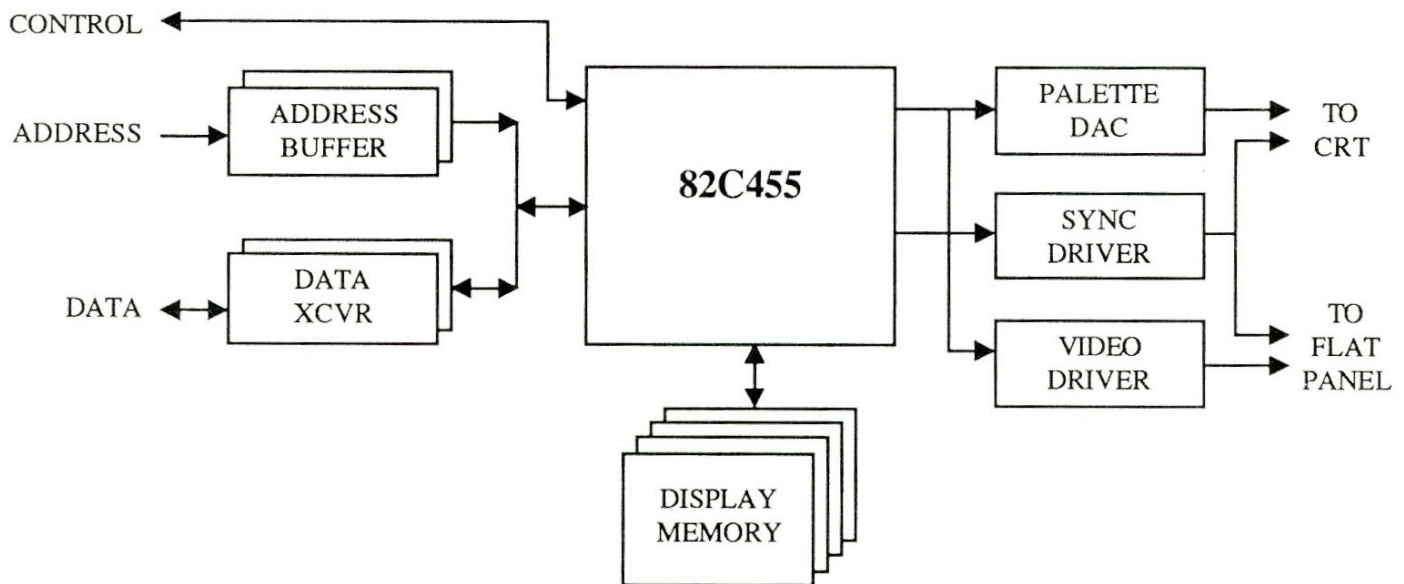# 82C455
Flat Panel/CRT
VGA Controller

- 100% IBM VGA-compatible

- Supports analog/digital CRT monitors and LCD, Plasma, and Electro Luminescent panels of varying resolutions

- Up to 16 gray levels on monochrome panels

- Integrates full support of color panels

- Programmable vertical compensation techniques increase usable display area

- SMARTMAP™ intelligent color to gray level conversion

- Advanced SLEEP modes minimize power consumption

- Single chip implementation tightly couples to the CHIPS/280 and interfaces with 8- and 16-bit PC bus and MCA (an interface compatible with MicroChannel™)

- Can utilize an external palette DAC with up to 16 million colors

- Full backwards compatibility with IBM EGA, CGA, MDA and Hercules graphics standards

82C455 System Implementation

Introduction

The 82C455 VGA Flat Panel/CRT controller provides a single-chip solution for a VGA, EGA, CGA, MDA, or Hercules compatible display system. The 82C455 supports a wide variety of flat panel displays and CRT monitors.

By providing a high level of integration, the 82C455 minimizes the total chip count for VGA display subsystems. The 82C455's power-down features reduce power consumption of the display subsystem and extend battery life in portable applications. The 82C455 provides a variety of programmable features, such as Vertical Compensation, SMARTMAP™ and Alternate Registers to enhance the flat panel display.

FLAT PANEL DISPLAYS

There is currently no standard interface for flat panel displays. Interface signals and timing requirements vary between panel technologies and manufacturers. The 82C455 provides register programmable features to allow interfacing to the widest possible range of flat panel display units.

The 82C455 interfaces directly to monochrome, grayscale or color panels. A proprietary Frame Rate Control algorithm generates 16 gray levels on monochrome panels. (Frame Rate Control generates gray levels on monochrome panels by turning the pixels on and off over several frames.) The 82C455 outputs 16 level grayscale for panels which internally generate gray levels and drives color panels with up to 64 colors.

The 82C455 supports all flat panel display technologies including plasma, electroluminescent (EL) and liquid crystal displays (LCD). LCD panel interfaces are provided for single panel-single drive (SS), dual panel-single drive (DS), and dual panel dual drive (DD) configurations. A single panel sequences data similar to a CRT. In contrast, a dual panel requires video data sequence from separate locations in memory. In addition, a dual drive panel requires the sequence to occur simultaneously. The 82C455 handles the display data sequencing transparent to the application software providing full compatibility on both CRT and flat panel displays.

The 82C455 can support the popular panel resolutions of 640x200, 640x350, 640x400 and 640x480. For non-standard applications additional resolutions are supported. The 82C455 provides a direct interface to panels from vendors such as Sharp,

Sanyo, Epson, Oki, Toshiba, Hitachi, Fujitsu, NEC, Matsushita and Finlux.

CRT MONITOR

The 82C455 supports both fixed and variable frequency analog monitors, including IBM PS/2™ and Multisync™ or Multi-Scan monitors. With the addition of a single CMOS PAL and required oscillators, the 82C455 supports digital TTL monitors for CGA, MDA and EGA standards. High resolution support is provided on both fixed and variable frequency monitors. When booting a system, the BIOS determines the monitor type and whether to boot on the CRT or flat panel. Programming a single register switches the display between the CRT and flat panel.

COMPATIBILITY

The 82C455 is fully compatible with the IBM VGA standard. The 82C455 also provides compatibility with IBM's EGA, CGA and MDA standard and the Hercules graphics adapter. The 82C455 includes a variety of features to provide compatibility on flat panel displays. Internal compensation techniques ensure that industry-standard software designed for different displays can be executed on the single flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software.

EXTENSION REGISTERS

The 82C455 employs an "Extension" Register set to control its enhanced features. These Extension Registers provide control of the flat panel interface, flat panel timing, vertical compensation, SMARTMAP™ and Backwards Compatibility.

Flat Panel Interface Registers

The Flat Panel Interface characteristics are controlled by a subset of the Extension Registers. These Registers select the panel type, data formatting, panel configuration, panel size, clock selection and video polarity. Since the 82C455 is designed to support a wide range of panel types and sizes, the control of these features is fully programmable. The video polarity of text and graphics modes is independently settable to allow black text on a white background and still provide normal graphics images.

Flat Panel Timing Registers

Flat panel displays usually require sync signal timing that is different from a CRT. To provide full compatibility with IBM VGA standard, alternate timing registers are used to allow independent timing of the sync signals for flat panel displays. Unlike the values programmed into the standard CRT timing registers, the value programmed into the alternate timing registers is dependent on the panel type used and is independent of the display mode.

VERTICAL COMPENSATION

Vertical Compensation is a programmable feature that increases the usable display area when running lower resolution software on a higher resolution panel. Unlike CRT monitors, flat panels have a fixed number of scan lines (e.g., 200, 350, 400 or 480 lines). Lower resolution software run on a higher resolution panel only partially fills the usable display area. For instance, 350-line EGA software displayed on a 480-line panel would leave 130 blank lines at the bottom of the display. The 82C455 offers the following three Vertical Compensation techniques to increase the useable screen area:

First, border insertion (referred to as "centering") adjusts the Display Start and Display End addresses to center the display, leaving a border of unused area at the top and bottom of the panel. Border insertion can be used in text and graphics modes.

Second, line replication (referred to as "stretching") duplicates every Nth display line (where N is programmable), thus stretching text characters and graphic images an adjustable amount. The display can be stretched to completely fill the flat panel area. Double scanning, a form of line replication where every line is replicated, is useful for running 200 line software on a 400 line panel. Line replication can be used in text and graphics modes.

Third, blank line insertion, inserts N blank lines (where N is programmable) between each line of text characters. Thus text can be evenly spaced to fill the entire panel display area without altering the height and shape of the text characters. Blank line insertion can be used in text mode only.

Each of these Vertical Compensation techniques can be controlled by programming the 82C455's Extension Registers. A combination of centering and stretching or blank line insertion may also be used.

SMARTMAP™

SMARTMAP™ is a proprietary feature that can be invoked to intelligently map colors to gray levels in text mode. SMARTMAP improves the legibility of flat panel displays by solving a common problem:

Most application programs are optimized for color CRT monitors using multiple colors. For example, a word processor might use a blue background with white characters for normal text, underlined text could be display in green, italicized text in yellow, and so on. This variety of colors, which is quite distinct on a color CRT monitor, can be illegible on a monochrome flat panel display if the colors are mapped to adjacent grayscale values. In the example, underlined and italicized text would be illegible if yellow is mapped to grayscale 4, green to grayscale 6 with the blue background mapped to grayscale 5.

SMARTMAP compares and adjusts the foreground and background grayscale values to produce adequate display contrast on flat panel displays. The minimum contrast value and the foreground/background grayscale adjustment values are programmed in the 82C455's Extension Registers. This feature can also be disabled completely.

VIDEO BIOS

In typical applications, the 82C455 is placed on the CPU board and the video BIOS is integrated with the system BIOS. A signal (ROMCS/) is provided for implementing a separate 8-bit ROM VIDEO BIOS. Chips and Technologies supplies a video BIOS that is optimized for the 82C455 hardware. The BIOS supports the extension functions of the 82C455, such as switching between the flat panel and the CRT, SMARTMAP™, Vertical Compensation, and palette load/save. The BIOS Modification Program (BMP) enables OEMs to tailor their feature set by programming the extension functions. Chips offers the BIOS as a standard production version, a customized version or as source code.

POWER-SAVING MODES

The 82C455 supports two power-down modes to reduce power consumption and extend battery-based operation. The first mode is the Relax mode, during which the display is blanked and the backlight (if used) can be turned off. While in the Relax mode, the 82C455 continues to generate video memory re-

fresh cycles and all display timing signals for the flat panel. The CPU has complete access to all the internal registers and to display memory. This mode is useful when the CPU is manipulating video data and updating display memory but no other user activity is occurring. Because the CRT Controller does not execute any DRAM cycles for the purpose of updating the display, power consumption in the DRAM is reduced. As an added benefit, the CPU can utilize the full display memory bandwidth while in this mode.

The second mode is the Retire mode, during which the 82C455 is invisible to the system. While in the Retire mode, the display is blanked, the display timing signals are halted and the flat panel should be turned off. The CPU cannot access any internal registers or display memory. During Retire, the 82C455 continues to refresh the DRAMs at a programmable rate, to conserve power in the display memory while preventing data loss. This mode is useful when system operation is suspended.

BUS INTERFACE

The 82C455 directly interfaces to 8-bit PC and PC/XT, 16-bit PC/AT and 8 or 16-bit MCA buses. All operations necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations, and generation of the necessary control signals.

The 82C455 interfaces directly to the CHIPS/250 and CHIPS/280, providing a simple, cost-effective solution for PS/2 compatible systems. When used with one of these CHIPSets, the 82C455 can execute FAST memory cycles at a speed greater than that normally available on the MCA bus.

DISPLAY MEMORY

The 82C455 supports a total of 256 Kbytes of display memory. The 82C455 serves as a DRAM controller for the system's display memory. It handles DRAM refresh, fetches data from display memory as required to refresh the screen, interfaces the CPU to display memory, and supplies all necessary DRAM control signals. The display memory is arranged as four planes of 64 Kbytes each. Each plane is eight bits wide for a total of 32 bits. Planes 0 and 1 share a common address bus, as do Planes 2 and 3. Each plane has a separate CAS signal and share a common RAS and write enable. Supported DRAMS include two 64Kx16 (with separate CAS or write enable signals), four 64Kx8 or eight 64Kx4. 120ns DRAMS are required

for clock inputs up to 30MHz. Pseudo-Static and SRAMs can be supported with external address latches.

82C455 ARCHITECTURE

The 82C455 integrates four major internal modules:

Graphics Controller

The Graphics Controller interfaces the 8- or 16-bit CPU data bus to the 32-bit data bus used by the four planes (Maps) of display memory. It also latches and supplies display memory data to the Attribute Controller for use in refreshing the screen image. For text modes, this data is supplied in parallel form (character generator data and attribute code); for graphics modes, it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller also performs any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Sequencer

The Sequencer generates all CPU and display memory timing signals. It controls CPU access of display memory by inserting cycles dedicated to CPU access. It also contains mask registers which can prevent writes to individual display memory planes.

Attribute Controller

The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and 16 color graphic modes the 4-bit pixel data acts as an index into a set of internal color look-up registers which generate a 6-bit stream. Two additional bits of color data are added to provide an 8-bit address to the external color palette. In 256 color modes, two 4-bit values are passed through the color look-up registers and assembled into an 8-bit value. Text and cursor blink, underline and horizontal scrolling are also the responsibility of the Attribute Controller.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

MODES OF OPERATION

The 82C455 addresses the specific requirements of laptop design by providing different modes of operation to optimize power usage. The table at the bottom of the page summarizes these modes and display memory access in each.

Test Mode

This mode is entered when the RESET pin is low and the TEST pin is high. It is used for factory test purposes.

Reset mode

When this mode is activated by pulling the RESET pin high, the 82C455 is forced to VGA-compatible mode and the CRT is selected as the active display. In addition, the 82C455 is disabled; it must be enabled after deactivating the RESET pin by writing to the Global Enable Register (102h in Setup Mode). Access to all Extension Registers is also disabled. They must be explicitly enabled via the Extension Enable Register (103h in Setup Mode) following a reset. The RESET pin must be active for at least 64 clock cycles.

Setup Mode

In this mode, only the configuration registers are accessible (these include the Global Enable, Extension Enable and Global ID). In an MCA configuration, Setup mode is entered when the SETUP/ pin is low. This pin is typically controlled by bit-5 of port 94h and is implemented in system logic external to the 82C455. In a PC-bus implementation, Setup mode is entered by writing a 1 to bit-4 of port 46E8h. This port is incorporated in the 82C455. While in Setup mode, the video output is active if it was active prior to entering Setup mode and inactive if it was inactive prior to entering Setup mode.

Normal Operating Mode

In this mode all functions of the 82C455 are enabled except that the configuration registers are not accessible.

Relax and Retire Modes

The 82C455 supports two power-down modes to reduce power consumption and extend battery-based operation. The first mode is the Relax mode, during which the display is blanked and the backlight (if used) can be turned off. While in the Relax mode, the 82C455 continues to generate video memory refresh cycles and all display timing signals for the flat panel. The CPU has complete access to all the internal registers and to display memory. This mode is useful when the CPU is manipulating video data and updating display memory but no other user activity is occurring. Because the CRT Controller does not execute any DRAM cycles for the purpose of updating the display, power consumption in the DRAM is reduced. As an added benefit, the CPU can utilize the full display memory bandwidth while in this mode.

The second mode is the Retire mode, during which the 82C455 is invisible to the system. While in the Retire mode, the display is blanked, the display timing signals are halted and the flat panel should be turned off. The CPU cannot access any internal registers or display memory. During Retire, the 82C455 continues to refresh the DRAMs at a programmable rate to conserve power in the display memory while preventing data loss. This mode is useful when system operation is suspended.

Mode of Operation	RESET Pin	TEST Pin	PWRDN1 Pin	PWRDN2 Pin	Display Memory Access by CPU	Display Memory Access for Display Refresh
Test	Low	High	xxx	xxx	-----	-----
Reset	High	xxx	xxx	xxx	-----	-----
Setup	-----	-----	-----	-----	No	Yes
Normal	Low	Low	Low	Low	Yes	Yes
Relax	Low	Low	High	Low	Yes	No
Retire	Low	Low	Low	High	No	No

Note: Combinations of pin levels not shown in the table above are illegal and should not be used.

GENERAL PURPOSE OUTPUTS

The 82C455 provides two general purpose output pins. This feature relies on redefinition of the TRAP/ and ERMEN/ pins with the General Purpose Output Registers (XR08 and XR09). These pins can be defined to serve their normal function or can be individually 3-stated, forced low, or forced high. In most applications, the trap pin is used as a CRT / LCD control signal.

SCREEN BLANKING

The 82C455 permits blanking of the display by writing to bit-5 of the Sequencer Clocking Mode Register (SR01) or by pulling the PWRDN1 pin high. With the screen blanked, all memory cycles are available to the CPU except those used for display memory refresh. In addition, the video output can be forced to a pre-defined color (the default video) whenever the BLANK/ pin is asserted. This color is written to the Default Video Register (XR2B) (an Extension Register).

INTERNAL AND EXTERNAL PALETTES

The 82C455 contains 16 color look-up registers (in the Attribute Controller), each of which is 6 bits wide. These are used in 16 color modes to select 16 active colors from a palette of 64.

The 82C455 also supports an external palette DAC (Inmos IMSG176 or equivalent). CPU access to this device is controlled by the 82C455, which decodes CPU accesses and generates the PALRD/ and PALWR/ signals for the external palette. I/O addresses 3C6-3C9h are valid external palette addresses.

The internal color look-up table is always used in CRT modes and can be optionally used in the flat panel modes. The external palette is used only with analog CRTs. It is not used with digital CRTs and flat panels.

LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter are saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space at indices 10h and 11h. This allows simulation of a light pen hit in CGA and Hercules modes.

SYSTEM TRAPS

The 82C455 supports generation of traps (NMIs) on one or more conditions. The Trap Enable and Trap Status Registers (XR16 and XR17) are utilized to implement this feature. Note: the use of traps with OS/2™ and other operating environments may cause problems.

FRAME INTERRUPTS

The 82C455 supports frame interrupts in a manner compatible to either the PC bus or MCA bus. For compatibility with the IBM VGA adapter in the PC bus, frame interrupts may also be disabled through the Emulation Mode register (XR14).

DIP SWITCH INPUTS

The 82C455 supports up to 7 DIP switch inputs. These can be read through the Dip Switch Register (XR01). To implement this feature, the A16, A17, A18, BHE/, ADDHI, AEN (MIO/) and RFSH/ (VGAENAB) pins are connected to the 7 DIP switches through a multiplexer. These inputs can be used to define initialization conditions. Note: the standard CHIPS BIOS does not require that any DIP switches be connected to these inputs.

CONTEXT SWITCHING

For support of multi-tasking, windowing and context switching operating environments, the entire state of the 82C455 (internal registers) is read- and write-able. This feature is 100% compatible with IBM's VGA.

WRITE PROTECTION

A Feature of the 82C455 is the ability to write protect most of the standard VGA registers. This feature is used to provide backwards compatibility with software written for older generation display types. The write protection is grouped into register sets and controlled by the Write Protect Register (XR15).

82C455 FLAT-PANEL VGA

Note:
Pin names shown indicate ISA bus connections
Pin names in brackets [...] indicate MCA bus connections
Pin names in parenthese (...) indicate alternate function

Top pins (108–73):

Pin	Signal	Alternate
108	SENSE	
107	Reserved	
106	Reserved	
105	CLK0	
104	CLK1	
103	CLK2	
102	GND	
101	MCLK	
100	PALRD/	
99	PALWR/	
98	VSYNC	(FLM)
97	HSYNC	(LP)
96	BLANK/	(DE)
95	P7	
94	P6	
93	P5	
92	SHFCLK	
91	GND	
90	VCC	
89	P4	
88	P3	
87	P2	
86	P1	
85	P0	
84	PCLK	
83	WGTCLK	(DE)
82	PTMC	[MCA/]
81	GND	
80	RFSH/	[VGAENAB]
79	IOWR/	[SETUP/]
78	IOCS16/	[VGAREQ/]
77	MEN16/	[DS16/]
76	ROMCS/	
75	WR46E8/	[CSFB/]
74	RDY	
73	VCC	

Left side pins (109–144):

Pin	Signal	Alternate
109	Reserved	
110	Reserved	
111	PWRDN1	
112	TRAP/	(CRT / LCD)
113	IRQ	[IRQ/]
114	RESET	
115	M2D0	
116	M3D0	
117	GND	
118	M2D1	
119	M3D1	
120	M2D2	
121	M3D2	
122	M2D3	
123	M3D3	
124	M2D4	
125	M3D4	
126	VCC	
127	GND	
128	M2D5	
129	M3D5	
130	M2D6	
131	M3D6	
132	M2D7	
133	M3D7	
134	CAS0/	
135	CAS1/	
136	CAS2/	
137	CAS3/	
138	GND	
139	WE/	
140	ERMEN/	(GPOUT)
141	BA0	
142	M0D0	
143	AA0	
144	M1D0	

Right side pins (72–37):

Pin	Signal	Alternate
72	BHE/	[MCA/]
71	AEN	[MIO/]
70	MEMR/	[S1/]
69	MEMW/	[S0/]
68	IORD/	[CMD/]
67	ADREN/	
66	GND	
65	RDLO/	
64	RDHI/	
63	AD0	
62	AD1	
61	AD2	
60	AD3	
59	AD4	
58	AD5	
57	AD6	
56	AD7	
55	GND	
54	VCC	
53	AD8	
52	AD9	
51	AD10	
50	AD11	
49	AD12	
48	AD13	
47	AD14	
46	AD15	
45	GND	
44	A16	
43	A17	
42	A18	
41	ADDHI	
40	PWRDN2	
39	DATEN/	
38	TEST	
37	Reserved	

Bottom pins (1–36):

Pin	Signal	Alternate
1	VCC	
2	BA1	
3	M0D1	
4	AA1	
5	M1D1	
6	BA2	
7	M0D2	
8	AA2	
9	GND	
10	M1D2	
11	BA3	
12	M0D3	
13	AA3	
14	M1D3	
15	BA4	
16	M0D4	
17	ACDCLK	(M)
18	VCC	
19	GND	
20	RAS/	
21	AA4	
22	M1D4	
23	BA5	
24	M0D5	
25	AA5	
26	M1D5	
27	BA6	
28	M0D6	
29	AA6	
30	GND	
31	M1D6	
32	BA7	
33	M0D7	
34	AA7	
35	M1D7	
36	Reserved	

Pin #	Pin Name		Type	Active	Description
71	AEN	[MIO/]	In	Both	ADDRESS ENABLE or MEMORY/IO and AUXILIARY DATA BIT 5. In PC-Bus interfaces, this input is named AEN. When low, it indicates a valid I/O address. In MCA interfaces, MIO/ high selects a memory cycle and low selects an I/O cycle. When defined as MIO/, it must be valid when the ADREN/ input is low. The AEN [MIO/] signal is latched internally. In both MCA and PC-Bus environments this pin serves as an auxiliary data bit input. It is read into bit 5 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.
69	MEMW/	[S0/]	In	Low	MEMORY WRITE or STATE 0/. In PC-Bus interface applications, this input is named MEMW/. It must be low for CPU writes to display memory. S0/ is the memory and I/O write input from the MCA bus.
70	MEMR/	[S1/]	In	Low	MEMORY READ or STATE 1/. In PC-Bus interface applications, this input must be low to permit the CPU to read display memory. S1/ is the memory and I/O read input from the MCA bus.
79	IOWR/	[SETUP/]	In	Low	I/O WRITE or VGA SETUP. In PC-BUS interface applications, this input is named IOWR/. It must be low to permit the CPU to write to an 82C455 I/O register. In an MCA environment the active low SETUP/ input allows configuration registers at I/O Addresses 100-104h to be accessed. All other memory and I/O functions are disabled.
68	IORD/	[CMD/]	In	Low	I/O READ or VGA COMMAND. In a PC-Bus environment this input is named IORD/. It must be low to permit the CPU to read an I/O register. In an MCA environment this active low signal indicates a command bus cycle. CMD/ must not be asserted during system memory refresh cycles.
80	RFSH/	[VGAENAB]	In	Both	REFRESH or VGA ENABLE and AUXILIARY DATA BIT 6. In the PC-Bus interface, RFSH/ high indicates a valid memory cycle. In an MCA environment this active high input signal enables memory and I/O accesses. This pin also serves as an auxiliary data bit input which is read into bit 6 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.
82	PTMC	[MCA/]	In	Both	PTMC. This input selects the type of CPU interface. PTMC low selects an MCA interface and high selects a PC-Bus (ISA) interface. This input must always be valid.

Pin #	Pin Name		Type	Active	Description
78	IOCS16/	[VGAREQ/]	Out	Low	I/O SELECT 16 or VGA REQUEST. In a PC-Bus environment this active low signal indicates a valid 16 bit I/O cycle. IOCS16/ is driven when the VGA is accessed and 3-stated when the VGA is inactive. In an MCA environment this output indicates that a FAST memory cycle can be executed. (This feature can be disabled through a register).
74	RDY	[DS16/] [VGARDY]	Out	High	VGA READY. When low, this output indicates that the current CPU read/write cycle must be extended with wait states. RDY is driven when the VGA is accessed; it is 3-stated when the VGA is inactive.
77	MEN16/	[DS16/]	Out	Low	MEMORY ENABLE 16 or VGA ADDRESS SELECT 16. In a PC-Bus environment this active low signal indicates 16-bit memory cycle transfers are enabled. This signal should be used by external logic to enable decode of high order addresses and generation of MEMCS16/ for the PC-AT bus. In an MCA environment this active low output indicates that a 16-bit memory or I/O transfer cycle is occurring.
75	WR46E8/	[CSFB/]	Out	Low	WRITE 46E8h or CARD SELECT FEEDBACK (VGA Acknowledge). In a PC-Bus environment this active low signal indicates a valid I/O write to address 46E8h. In an MCA environment this active low output indicates a valid CPU access (memory or I/O) to the 82C455.
76	ROMCS/		Out	Low	ROM CHIP Select. In a PC-Bus environment this active low signal indicates a valid memory read in the range C0000h-C7FFFh. It is used to generate the enable for 8-bit BIOS ROMs.
113	IRQ	[IRQ/]	Out	Both	VGA INTERRUPT. An interrupt can be generated whenever the vertical sync signal goes active. For the PC-Bus, this pin may be logically disconnected (3-stated) through the Emulation Mode register (XR14D7) independent of whether interrupts are enabled or disabled. Clearing XR14D7 emulates the function of the IBM PC-Bus VGA board interrupt output. In the MCA bus, this pin is always functional.

Interrupt State	XR14D7=0 PC Bus	XR14D7=0 MCA Bus	XR14D7=1
Disabled	3-state	3-state	3-state
Enabled & Inactive	3-state	3-state	Low
Enabled & Active	3-state	Low	High

Pin #	Pin Name	Type	Active	Description
114	RESET	In	High	RESET. An active high input which resets the 82C455.
38	TEST	In	High	TEST. This input is used for factory testing only. It must be tied low for normal operation.
40 111	PWRDN2 PWRDN1	In In	High High	POWER DOWN 2,1. The Power Down input pins select the Normal, Relax, and Retire modes of operation as follows:

PWRDN2	PWRDN1	Operation
0	0	Normal Operation
0	1	Relax Mode
1	0	Retire Mode
1	1	Illegal

Pin #	Pin Name	Type	Active	Description
108	SENSE	In	Both	SENSE. The state of this input pin can be read at Input Status Register 0, Bit 4.
100	PALRD/	Out	Low	PALETTE READ. This output is active low during I/O reads from addresses in the range 3C6h or 3C8-3C9h (I/O reads from 3C7h are handled directly by the 82C455). This output is normally connected to the Read input of an external Palette/DAC (Brooktree BT475 or equivalent).
99	PALWR/	Out	Low	PALETTE WRITE. This output is active low during I/O writes to addresses in the range 3C6-3C9h and is normally connected to the Write input of an external Palette/DAC (Brooktree BT475 or equivalent).
41	ADDHI	In	High	ADDRESS HIGH and AUXILIARY DATA BIT 4. This high order memory address enable input is generated external to the 82C455 by decoding system addresses A19-A23. As an address, it must be valid when ADREN/ is low, is latched internally and specifies that the current memory address is valid for the 82C455. This pin is an auxiliary data bit read into bit 4 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This input pin is ignored during I/O cycles.
72	BHE/	In	Low	BYTE HIGH ENABLE and AUXILIARY DATA BIT 3. BHE/ low indicates that the high order byte at the current word address is being accessed. If active, BHE/ must be valid when ADREN/ is low. This pin is also an auxiliary data input which is read into bit 3 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This data bit is latched internally on the falling edge of the command signal.

Pin #	Pin Name	Type	Active	Description
67	ADREN/	Out	Low	ADDRESS ENABLE. The ADREN/ output controls external multiplexing of the system address/data bus. ADREN/ low selects address and ADREN/ high selects data. In a PC or PC/AT bus interface, ADREN/ is low when MEMR/, MEMW/, IORD/, and IOWR/ are all high. ADREN/ is high when any one of MEMR/, MEMW/, IORD/ or IOWR/ is low. In an MCA interface, ADREN/ is low when CMD/ is high and ADREN/ is high when CMD/ is low.
39	DATEN/	Out	Low	DATA ENABLE. Inverse of ADREN/. This pin is 3-stated during RESET.
65	RDLO/	Out	Low	READ LOW. This output controls the direction of the external data transceivers on the low order byte (Bits 0-7) of the address/data bus. It is low when data is read from the 82C455 and high when data is written to the 82C455. DATEN/ can be used to enable the external transceiver. This pin is 3-stated during RESET.
64	RDHI/	Out	Low	READ HIGH. This output operates identically to the RDLO/ output except that it controls the direction for the high order byte (Bits 8-15) of the address/data bus. RDHI/ is low when data is read from the 82C455 and high when data is written to the 82C455. This pin is 3-stated during RESET.
63	AD0	I/O	Both	SYSTEM ADDRESS and DATA BITS 15-0. These bits are used to address display memory and the I/O mapped 82C455 internal registers. They also transfer data between the CPU bus and display memory and 82C455 registers. Addresses must be valid when output signal ADREN/ is low and data must be held while DATEN/ is low. Addresses are latched internally.
62	AD1	I/O	Both	
61	AD2	I/O	Both	
60	AD3	I/O	Both	
59	AD4	I/O	Both	
58	AD5	I/O	Both	
57	AD6	I/O	Both	
56	AD7	I/O	Both	
53	AD8	I/O	Both	
52	AD9	I/O	Both	
51	AD10	I/O	Both	
50	AD11	I/O	Both	
49	AD12	I/O	Both	
48	AD13	I/O	Both	
47	AD14	I/O	Both	
46	AD15	I/O	Both	
44	A16	In	Both	SYSTEM ADDRESS BITS 18-16 and AUXILIARY DATA BITS 2-0. These bits transfer a high-order address when ADREN/ is low. The auxiliary data bits on pins A16, A17, and A18 respectively are read into bits 0-2, respectively, of the DIP Switch register when that register is accessed by the CPU. The address bits are latched internally and are ignored for I/O cycles.
43	A17	In	Both	
42	A18	In	Both	

Pin #	Pin Name	Type	Active	Description
142	M0D0	I/O	Both	MEMORY 0 DATA. Display memory data bus for
3	M0D1	I/O	Both	Plane 0 (Map 0).
7	M0D2	I/O	Both	
12	M0D3	I/O	Both	
16	M0D4	I/O	Both	
24	M0D5	I/O	Both	
28	M0D6	I/O	Both	
33	M0D7	I/O	Both	
144	M1D0	I/O	Both	MEMORY 1 DATA. Display memory data bus for
5	M1D1	I/O	Both	Plane 1 (Map 1).
10	M1D2	I/O	Both	
14	M1D3	I/O	Both	
22	M1D4	I/O	Both	
26	M1D5	I/O	Both	
31	M1D6	I/O	Both	
35	M1D7	I/O	Both	
115	M2D0	I/O	Both	MEMORY 2 DATA. Display memory data bus for
118	M2D1	I/O	Both	Plane 2 (Map 2).
120	M2D2	I/O	Both	
122	M2D3	I/O	Both	
124	M2D4	I/O	Both	
128	M2D5	I/O	Both	
130	M2D6	I/O	Both	
132	M2D7	I/O	Both	
116	M3D0	I/O	Both	MEMORY 3 DATA. Display memory data bus for
119	M3D1	I/O	Both	Plane 3 (Map 3).
121	M3D2	I/O	Both	
123	M3D3	I/O	Both	
125	M3D4	I/O	Both	
129	M3D5	I/O	Both	
131	M3D6	I/O	Both	
133	M3D7	I/O	Both	

Pin #	Pin Name	Type	Active	Description
143	AA0	Out	Both	ADDRESS PLANES 1,0. Display memory address
4	AA1	Out	Both	bus for DRAM planes 0 and 1.
8	AA2	Out	Both	
13	AA3	Out	Both	
21	AA4	Out	Both	
25	AA5	Out	Both	
29	AA6	Out	Both	
34	AA7	Out	Both	
141	BA0	Out	Both	ADDRESS PLANES 3,2 Display memory address bus
2	BA1	Out	Both	for DRAM Planes 2 and 3.
6	BA2	Out	Both	
11	BA3	Out	Both	
15	BA4	Out	Both	
23	BA5	Out	Both	
27	BA6	Out	Both	
32	BA7	Out	Both	
20	RAS/	Out	Low	ROW ADDRESS STROBE. Row address strobe for all DRAM memory banks.
134	CAS0/	Out	Low	COLUMN ADDRESS STROBE 0. Active low column address strobe for Memory Plane 0.
135	CAS1/	Out	Low	COLUMN ADDRESS STROBE 1. Active low column address strobe for Memory Plane 1.
136	CAS2/	Out	Low	COLUMN ADDRESS STROBE 2. Active low column address strobe for Memory Plane 2.
137	CAS3/	Out	Low	COLUMN ADDRESS STROBE 3. Active low column address strobe for Memory Plane 3.
139	WE/	Out	Low	WRITE ENABLE. Active low write enable signal for all display memory banks/planes.

Pin #	Pin Name		Type	Active	Description
97	HSYNC	(LP)	Out	Both	HORIZONTAL SYNC OUTPUT. HSYNC is active high if the horizontal polarity bit (Bit-6 of the Misc. Output register, 3C2h) is low. It is active low if the horizontal polarity bit is high. In flat panel mode the polarity is controlled by the Alt. Misc. Output Reg. (XR54).
98	VSYNC	(FLM)	Out	Both	VERTICAL SYNC OUTPUT. VSYNC is active high if the vertical polarity bit (Bit 7 of the Misc. Output register, 3C2h) is low. It is active low if the vertical polarity bit is high. In flat panel mode the polarity is controlled by the Alt. Misc. Output Reg. (XR54).
96	BLANK/	(DE)	Out	Both	BLANK or DISPLAY ENABLE. BLANK/ is a programmable output for blanking the CRT which is normally connected to the RAMDAC. It can be redefined as a Display Enable signal in systems where a RAMDAC is not required.
85	P0		Out	Both	VIDEO PIXEL DATA 7-0. Eight outputs to drive color or monochrome display devices. Color values for digital CRT interface are assigned as follows:
86	P1		Out	Both	
87	P2		Out	Both	
88	P3		Out	Both	
89	P4		Out	Both	P0 B Blue
93	P5		Out	Both	P1 G Green
94	P6		Out	Both	P2 R Red
95	P7		Out	Both	P3 BS/V Secondary Blue / Monochrome
					P4 GS/I Secondary Green / Intensity
					P5 RS Secondary Red
					P6 User Defined
					P7 User Defined
92	SHFCLK		Out	Both	SHIFT CLOCK. Output pixel clock to which video panel output data is synchronized.
84	PCLK		Out	Both	PIXEL CLOCK. Output pixel clock to which CRT Video output data is synchronized. This pin is 3-stated during RESET.
83	WGTCLK	(DE)	Out	High	WEIGHT CONTROL CLOCK or DISPLAY ENABLE. Grayscale reference clock for Panels with Pulse Width Modulation support. When clock masking is disabled (XR50D7=0), this pin is redefined as a Display Enable (DE) pin which qualifies the active display time.
17	ACDCLK	(M)	Out	Both	LCD CLOCK. A 50% duty cycle square-wave with programmable period. Used to time the back bias switching in LCD panels.

Pin #	Pin Name		Type	Active	Description
140	ERMEN/	(GPOUT)	Out	Low	EARLY MEMORY INDICATOR. This output indicates whether display memory is being accessed by the CPU or by the 82C455 to refresh the display. High indicates display access and low indicates CPU access. This signal can be redefined as a general purpose output.
112	TRAP/	(CRT / LCD)	Out	Low	TRAP. This active low output indicates a TRAP condition requiring special CPU assistance. This pin is open collector when used as a trap pin. It can be redefined as a general purpose output pin. The Chips BIOS redefines this as a CRT/$\overline{\text{LCD}}$ output. If this pin is high, the BIOS has programmed the part for CRT displays; if low, the BIOS has programmed the part for LCD displays.
103	CLK2		In	Both	CLOCK 2-0. Video Clock inputs. One of these dot clock inputs is selected by the Miscellaneous Output Register.
104	CLK1		In	Both	
105	CLK0		In	Both	
101	MCLK		In	Both	MASTER CLOCK. This clock input is used to sequence internal I/O cycles.
1	VCC		In	n/a	POWER
18	VCC				
54	VCC				
73	VCC				
90	VCC				
126	VCC				
9	GND		In	n/a	GROUND
19	GND				
30	GND				
45	GND				
55	GND				
66	GND				
81	GND				
91	GND				
102	GND				
117	GND				
127	GND				
138	GND				
36	Reserved				RESERVED. These pins are reserved and should be left unconnected.
37	Reserved				
106	Reserved				
107	Reserved				
109	Reserved				
110	Reserved				

82C455 Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register is used to enable or disable the VGA. It is also used to place the VGA in normal or setup mode. This register is used only in the PC-bus interface. In the MCA Bus interface these functions are performed by the VGAENAB and SETUP/ pins respectively.

The Global and Extension Enable Registers are accessible <u>only during Setup mode</u>. The Global ID Register contains the ID number that identifies the 82C455 as a Chips & Technologies product.

<u>Warning</u>: In setup mode, the Global Setup Registers actually occupy the *entire I/O space*. Only the lower 3 bits are used to decode and select these registers. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses. This decode is compatible with the IBM VGA.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE pin, pending CRT interrupt, display enable/HSYNC output, and vertical retrace/video output. The Feature Control Register selects the VSYNC function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video RAM, memory page, and video SYNC polarity.

CGA / HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

SEQUENCER REGISTERS

The Sequencer Index Register is a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4/16/32KBytes, Odd/Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register is a 6-bit index to the CRT Controller Registers. Twenty eight registers perform all display functions for modes: horizontal and vertical blanking and sync, panning and scrolling, cursor size and location, light pen, and underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register is a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND
EXTERNAL COLOR PALETTE REGISTERS

The Attribute Controller Index Register is a 5-bit index to the Attribute Controller Registers. A 6th bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen. External color palette registers handle CPU reads and writes to I/O address range 3C6h-3C9h. Some of the registers are located external to 82C455 in the external color palette. Inmos IMSG176 compatible registers are documented in this manual.

EXTENSION REGISTERS

The 82C455 defines a set of extension registers which are addressed with the 7-bit Extension Register Index. The I/O port address (3Bx/3Dxh)

and Read/Write access to the extension registers is controlled by the Extension Enable Register (103h). The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

1. Miscellaneous Registers include the 82C455 Version number, Dip Switch CPU interface and paging control, memory mode control, power down/refresh control and diagnostic functions.

2. General Purpose Registers allow the CPU to individually switch two outputs (ERMEN/ and TRAP/). They also handle video blanking interface and the video default color.

3. Backwards Compatibility Registers control Hercules, MDA, and CGA emulation modes. Trap Enable and Trap Status as well as Write Protect functions are provided to increase flexibility in providing backwards compatibility.

4. Alternate Horizontal and Vertical Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for both flat panels and backwards compatibility.

5. Panel Control Registers operate only in flat panel mode. The Panel Control Registers determine panel and video interface format display type and size, line drawing character function, and grayscale weighting and flat panel bias clocks.

6. Compensation Registers provide vertical centering, blank line insertion, and graphics stretching features. For 350 and 400 line display modes, registers are provided to control display start and end locations, blank line insertion in text modes and stretching in both graphics and text modes.

7. Color/Attributes Registers control Blink Rate, SmartMap™ threshold, and shift parameters. A Graphics Color Mapping register controls color to monochrome threshold, VGA 256-color mapping, color lookup table protection, and graphics video polarity.

The state of most of the Standard VGA Registers is undefined at reset. All registers specific to the 82C455 (Extension Registers) are summarized in the Extension Register Table.

82C455 Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
–	Setup Control	–	W	46E8h (PC-Bus only)	–	21
–	Global Enable	–	RW	102h & Setup mode	–	21
–	Extension Enable	–	RW	103h & Setup mode	–	22
–	Global ID	–	R	104h & Setup mode	–	22

## SETUP CONTROL REGISTER
Write only at I/O Address 46E8h
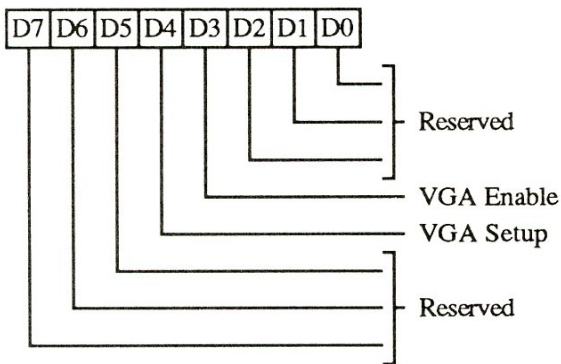
This register is used with the PC-Bus Interface only. It is cleared by RESET. In the MCA interface, the Setup mode and VGA Disable are controlled through the SETUP/ and VGAENAB pins, respectively.

2-0   Reserved (0)

3   VGA Enable

    0: VGA is disabled
    1: VGA is enabled

4   Setup Mode

    0: VGA is in Normal Mode
    1: VGA is in Setup Mode

7-5   Reserved (0)

GLOBAL ENABLE REGISTER
Read/Write at I/O Address 102h
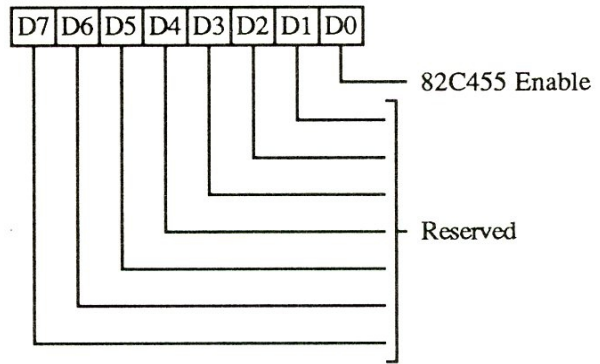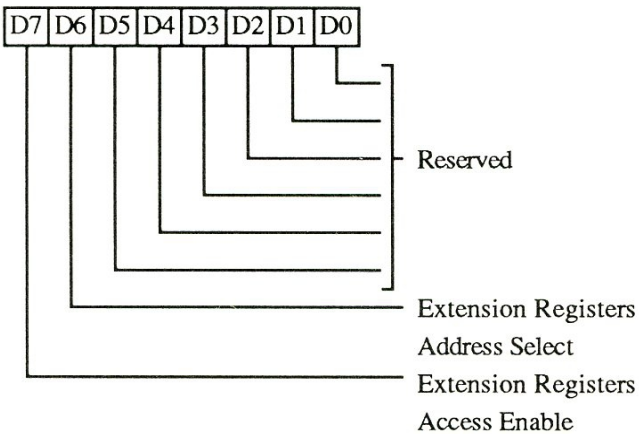

This register is only accessible in Setup Mode. It is cleared by RESET.

0   VGA Enable

    0: VGA is disabled
    1: VGA is enabled

7-1   Reserved (0)

EXTENSION ENABLE REGISTER
Read/Write at I/O Address 103h

D7	D6	D5	D4	D3	D2	D1	D0

— Reserved

— Extension Registers
Address Select

— Extension Registers
Access Enable

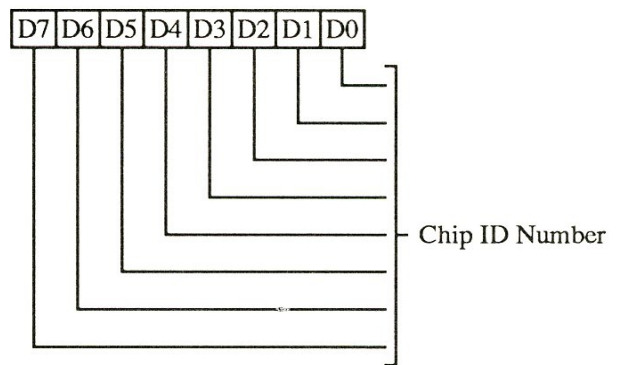This register is only accessible in Setup Mode. It is cleared by RESET.

3-0 Reserved (0)

4 Reserved (0) This bit must be set to zero for proper operation of the 82C455.

5 Reserved (0)

6 Address for Extension Registers

    0: Extension registers at
I/O Address 3D6/3D7h
    1: Extension registers at
I/O Address 3B6/3B7h.

7 Extension Registers Access Enable

This bit controls access to the extension registers at 3D6/7 or 3B6/7. It also allows access to all CGA, MDA and Hercules registers in non-emulation mode.

    0: Disable Access
    1: Enable Access

GLOBAL ID REGISTER
Read only at I/O Address 104h

D7	D6	D5	D4	D3	D2	D1	D0

— Chip ID Number

This register is only accessible in Setup Mode.

7-0 These bits contain the ID number (0A5h). This identifies the chip as a Chips and Technologies product.

82C455 General Control & Status Registers

| Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	23
ST01	Input Status 1	–	R	3BAh/3DAh	–	23
FCR	Feature Control	–	W	3BAh/3DAh	5	24
			R	3CAh		
MSR	Miscellaneous Output	–	W	3C2h	5	24
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)
Read only at I/O Address at 3C2h
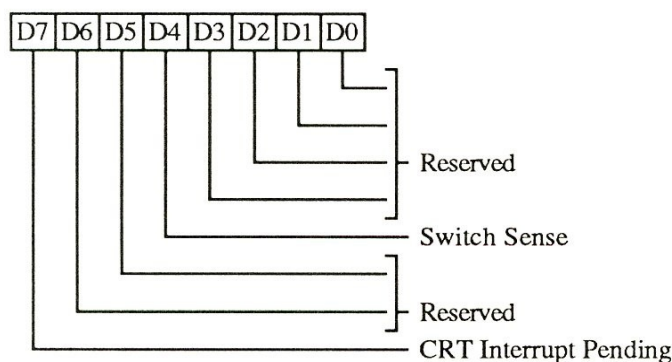
3-0 Reserved (0)

4 Switch Sense. This bit returns the Status of the SENSE pin.

6-5 Reserved. These bits read back 00 in an AT bus implementation and 11 in MCA implementation.

7 CRT Interrupt Pending

    0: Indicates no CRT interrupt is pending

    1: Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)
*Read only at I/O Address 3BAh/3DAh*
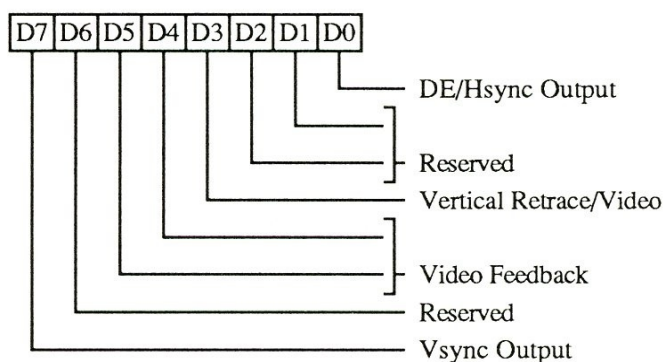
0 Display Enable/HSYNC Output. The functionality of this bit is controlled by the Emulation Mode register (XR14D4).

    0: Indicates DE or HSYNC <u>inactive</u>

    1: Indicates DE or HSYNC <u>active</u>

2-1 Reserved (0)

3 Vertical Retrace/Video. The functionality of this bit is controlled by the Emulation Mode register (XR14D5).

    0: Indicates VSYNC or video <u>inactive</u>

    1: Indicates VSYNC or video <u>active</u>

5-4 Video Feedback 1, 0. These are diagnostic video bits which are selected via the Color Plane Enable Register.

6 Reserved (0)

7 Vsync Output. The functionality of this bit is controlled by the Emulation Mode register (XR14D6). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

FEATURE CONTROL REGISTER (FCR)
Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection

D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

- D0–D1 — Reserved
- D2 — Vsync Control
- D4–D7 — Reserved
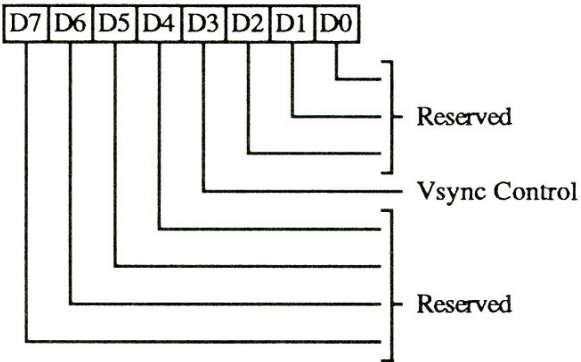
2-0 Reserved (0)

3 Vsync Control   This bit is cleared by RESET.

    0: VSync output on the VSYNC pin
    1: Logical 'OR' of VSync and
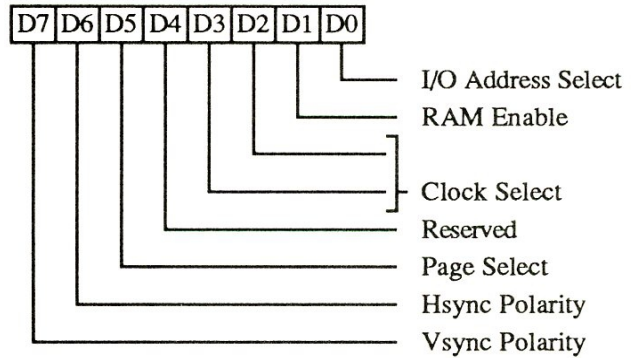   Display Enable output
       on the VSYNC pin

7-4 Reserved (0)

MISCELLANEOUS OUTPUT REGISTER (MSR)
Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection

D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0

- D0 — I/O Address Select
- D1 — RAM Enable
- D2–D3 — Clock Select
- D4 — Reserved
- D5 — Page Select
- D6 — Hsync Polarity
- D7 — Vsync Polarity

This register is effective in CRT mode.   The Alternate Miscellaneous Output register is used for bits 2,3,6 and 7 in flat panel mode. This register is cleared by RESET.

0 I/O Address Select. This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

    0: Select 3Bxh I/O address
    1: Select 3Dxh I/O address

1 Enable RAM. 0: Prevent CPU access to display memory; 1: Allow CPU access to display memory.

3-2 Clock Select. These bits select the dot clock source for the CRT interface:

    00 = Select CLK0
    01 = Select CLK1
    10 = Select CLK2
    11 = Reserved

4 Reserved (0)

5 Page Select. In Odd/Even Memory Map Mode 1 (GR06), this bit selects the upper or lower 64K byte page in display memory for CPU access: 1=select lower page; 0=select upper page.

6 CRT Hsync Polarity. 0=pos, 1=neg

7 CRT Vsync Polarity. 0=pos, 1=neg

(Blank pin polarity can be controlled via the Video Interface Register)

82C455 CGA / Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	RW	3D8h	–	25
COLOR	CGA Color Select	–	RW	3D9h	–	26
HCFG	Hercules Configuration	–	W	3BFh	–	27

CGA / HERCULES MODE CONTROL REGISTER (MODE)
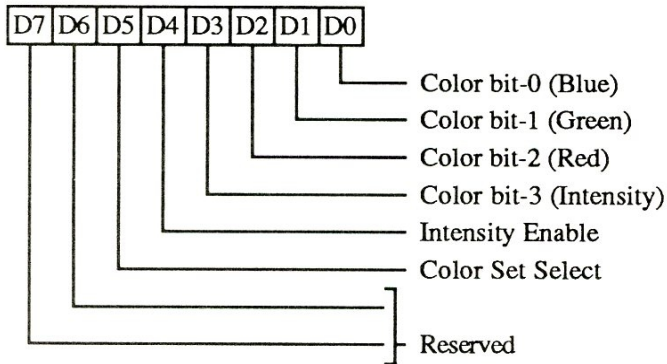*Read/Write at I/O Address 3B8h/3D8h*
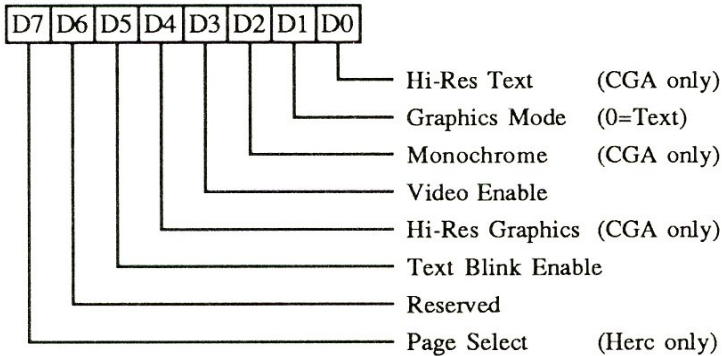
This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

0 CGA 80/40 Column Text Mode
  0: Select 40 column CGA text mode
  1: Select 80 column CGA text mode

1 CGA/Hercules Graphics/Text Mode
  0: Select text mode
  1: Select graphics mode

2 CGA Mono/Color Mode
  0: Select CGA color mode
  1: Select CGA monochrome mode

3 CGA/Hercules Video Enable
  0: Blank the screen
  1: Enable video output

4 CGA High Resolution Mode
  0: Select 320x200 graphics mode
  1: Select 640x200 graphics mode

5 CGA/Hercules Text Blink Enable
  0: Disable character blink attribute (blink attribute bit-7 used to control background intensity)
  1: Enable character blink attribute

6 Reserved (0)

7 Hercules Page Select
  0: Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode
  1: Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

CGA COLOR SELECT REGISTER
Read/Write at I/O Address 3D9h

```
D7 D6 D5 D4 D3 D2 D1 D0
                    └──── Color bit-0 (Blue)
                 └─────── Color bit-1 (Green)
              └────────── Color bit-2 (Red)
           └───────────── Color bit-3 (Intensity)
        └──────────────── Intensity Enable
     └─────────────────── Color Set Select
  └─┐
 └──┴──────────────────── Reserved
```

This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by RESET.

3-0   Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color: Foreground Color (color when the pixel value is 1)

The background color (color when the pixel value is 0) is black.

4   Intensity Enable

Text Mode: Enables intensified background colors

320x200 4-color: Enables intensified colors 0-3

640x200 2-color: Don't care

5   Color Set Select. This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:

Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

7-6   Reserved (0)

HERCULES CONFIGURATION REGISTER (HCFG)
Write only at I/O Address 3BFh

```
D7 D6 D5 D4 D3 D2 D1 D0
```
— Enable Graphics Mode
— Enable Memory Page 1

— Reserved
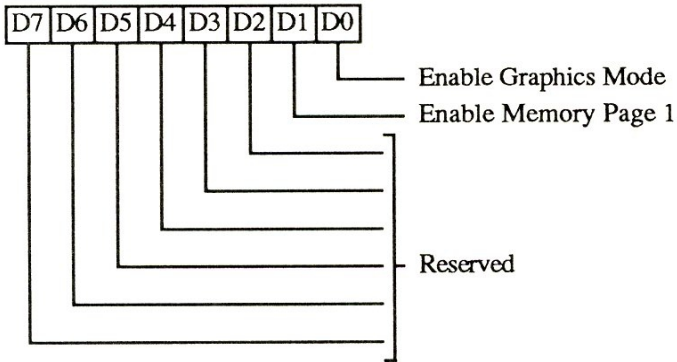
This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14D3&2. It is cleared by RESET.

0 Enable Graphics Mode

> 0: Lock the 82C455 in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh.

> 1: Permit entry to Hercules Graphics mode.

1 Enable Memory Page 1

> 0: Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.

> 1: The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.
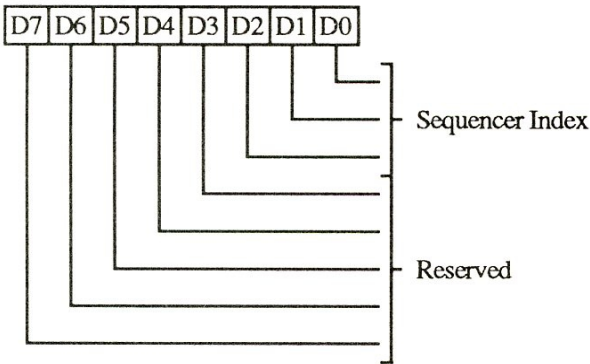
7-2 Reserved (0)

82C455 Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	RW	3C4h	1	29
SR00	Reset	00h	RW	3C5h	1	29
SR01	Clocking Mode	01h	RW	3C5h	1	30
SR02	Plane/Map Mask	02h	RW	3C5h	1	30
SR03	Character Font	03h	RW	3C5h	1	31
SR04	Memory Mode	04h	RW	3C5h	1	32
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	32

SEQUENCER INDEX REGISTER (SRX)
Read/Write at I/O Address 3C4h

This register is cleared by RESET.

2-0 These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

7-3 Reserved (0)

SEQUENCER RESET REGISTER (SR00)
Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection
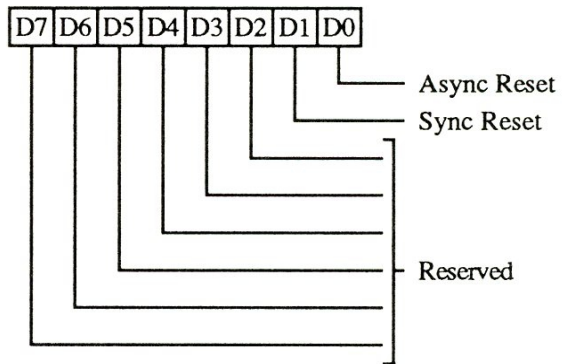
0 Asynchronous Reset

　　0: Force asynchronous reset
　　1: Normal operation

Display memory data will be corrupted if this bit is set to zero.

1 Synchronous Reset

　　0: Force synchronous reset
　　1: Normal operation

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tens of microseconds).

7-2 Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)
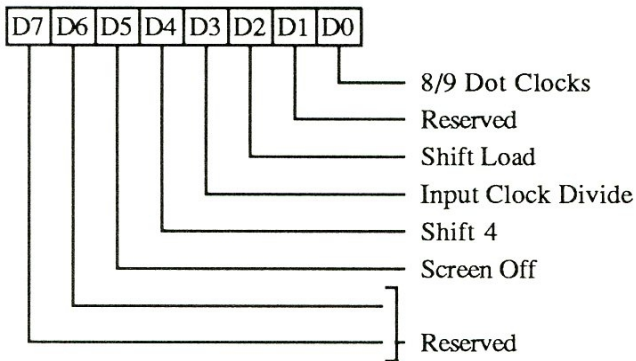*Read/Write at I/O Address 3C5h*
Index 01h
Group 1 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

8/9 Dot Clocks
Reserved
Shift Load
Input Clock Divide
Shift 4
Screen Off
Reserved

0　8/9 Dot Clocks.　This bit determines whether a character clock is 8 or 9 dot clocks long.

　　0:　Select 9 dots/character clock
　　1:　Select 8 dots/character clock

1　Reserved (0)

2　Shift Load

　　0:　Load video data shift registers <u>every</u> character clock
　　1:　Load video data shift registers <u>every other</u> character clock

Bit-4 of this register must be 0 for this bit to be effective.

3　Input Clock Divide

　　0:　Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
　　1:　Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

4　Shift 4

　　0:　Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register)
　　1:　Load shift registers every 4th character clock.

5　Screen Off

　　0:　Normal Operation
　　1:　Disable video output and assign all display memory bandwidth for CPU accesses

7-6　Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)
Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

Color Plane Enable
Reserved
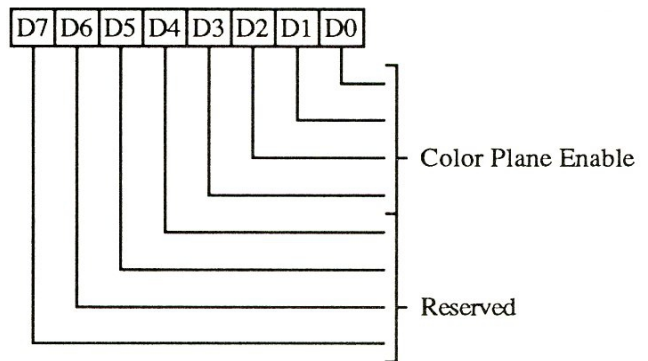
3-0　Color Plane Enable

　　0:　Write protect corresponding color plane
　　1:　Allow write to corresponding color plane.

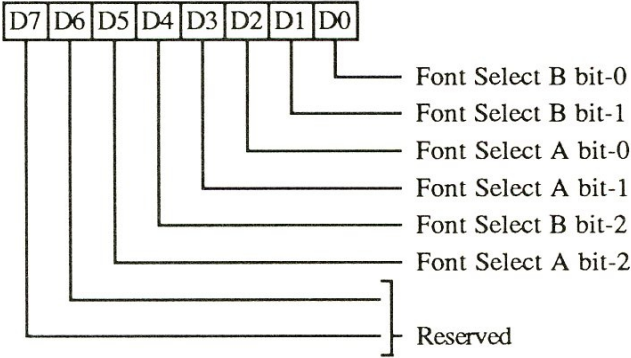In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.

7-4　Reserved (0)

CHARACTER FONT SELECT REGISTER (SR03)
Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                        └──── Font Select B bit-0
                     └─────── Font Select B bit-1
                  └────────── Font Select A bit-0
               └───────────── Font Select A bit-1
            └──────────────── Font Select B bit-2
         └─────────────────── Font Select A bit-2
      └──┐
   └─────┤ Reserved
```

In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04D1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0	Low order bits of Character Generator Select B
3-2	Low order bits of Character Generator Select A
4	High order bit of Character Generator Select B
5	High order bit of Character Generator Select A
7-6	Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

Code	Character Generator Table Location
0	First 8K of Plane 2
1	Third 8K of Plane 2
2	Fifth 8K of Plane 2
3	Seventh 8K of Plane 2
4	Second 8K of Plane 2
5	Fourth 8K of Plane 2
6	Sixth 8K of Plane 2
7	Eighth 8K of Plane 2

where 'code' is:

Character Generator Select A (bits 5, 3, 2) when bit-3 of the the attribute byte is one.
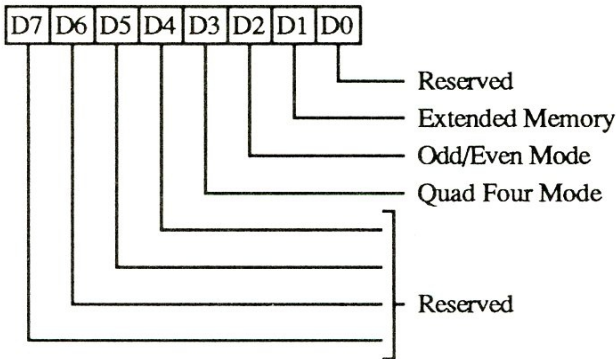
Character Generator Select B (bits 4, 1, 0) when bit-3 of the attribute byte is zero.

SEQUENCER MEMORY MODE REGISTER (SR04)
Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection

```
D7 D6 D5 D4 D3 D2 D1 D0
                     └──── Reserved
                  └─────── Extended Memory
               └────────── Odd/Even Mode
            └───────────── Quad Four Mode

                     └──── Reserved
```

0   Reserved (0)

1   Extended Memory

       0: Restrict CPU access to 4/16/32 Kby-
             tes
       1: Allow complete access to memory

     This bit should normally be 1.

2   Odd/Even Mode

       0   CPU accesses to Odd/Even addresses
           are directed to corresponding odd/even
           planes
       1   All planes are accessed simultaneously
           (IRGB color)

     Bit-3 of this register must be 0 for this bit to
     be effective. This bit affects only CPU <u>write</u>
     accesses to display memory.

3   Quad Four Mode

       0: CPU addresses are mapped to display
           memory as defined by bit-2 of this
           register
       1: CPU addresses are mapped to display
           memory modulo 4. The two low order
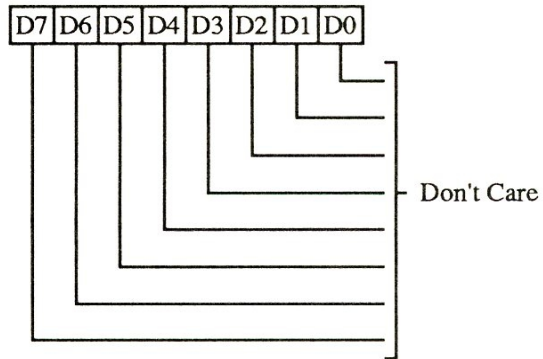   CPU address bits select the display
           memory plane.

     This bit affects both CPU reads and writes
     to display memory.

7-4   Reserved (0)

SEQUENCER HORIZONTAL CHARACTER COUNTER RESET REGISTER (SR07)
Read/Write at I/O Address 3C5h
Index 07h

```
D7 D6 D5 D4 D3 D2 D1 D0
                     └──── Don't Care
```

Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal and vertical counters will both be set to zero. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

This is a standard VGA register which was not documented by IBM.

82C455 CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	RW	3B4h/3D4h	–	34
CR00	Horizontal Total	00h	RW	3B5h/3D5h	0	34
CR01	Horizontal Display Enable End	01h	RW	3B5h/3D5h	0	34
CR02	Horizontal Blank Start	02h	RW	3B5h/3D5h	0	35
CR03	Horizontal Blank End	03h	RW	3B5h/3D5h	0	35
CR04	Horizontal Sync Start	04h	RW	3B5h/3D5h	0	36
CR05	Horizontal Sync End	05h	RW	3B5h/3D5h	0	36
CR06	Vertical Total	06h	RW	3B5h/3D5h	0	37
CR07	Overflow	07h	RW	3B5h/3D5h	0/3	37
CR08	Preset Row Scan	08h	RW	3B5h/3D5h	3	38
CR09	Maximum Scan Line	09h	RW	3B5h/3D5h	2/4	38
CR0A	Cursor Start Scan Line	0Ah	RW	3B5h/3D5h	2	39
CR0B	Cursor End Scan Line	0Bh	RW	3B5h/3D5h	2	39
CR0C	Start Address High	0Ch	RW	3B5h/3D5h	–	40
CR0D	Start Address Low	0Dh	RW	3B5h/3D5h	–	40
CR0E	Cursor Location High	0Eh	RW	3B5h/3D5h	–	40
CR0F	Cursor Location Low	0Fh	RW	3B5h/3D5h	–	40
CR10	Vertical Sync Start (See Note 2)	10h	W or RW	3B5h/3D5h	4	41
CR11	Vertical Sync End (See Note 2)	11h	W or RW	3B5h/3D5h	3/4	41
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	41
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	41
CR12	Vertical Display Enable End	12h	RW	3B5h/3D5h	4	42
CR13	Offset	13h	RW	3B5h/3D5h	3	42
CR14	Underline Row	14h	RW	3B5h/3D5h	3	42
CR15	Vertical Blank Start	15h	RW	3B5h/3D5h	4	43
CR16	Vertical Blank End	16h	RW	3B5h/3D5h	4	43
CR17	CRT Mode Control	17h	RW	3B5h/3D5h	3/4	44
CR18	Line Compare	18h	RW	3B5h/3D5h	3	45
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	46
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	46
CR3x	Clear Vertical Display Enable	3xh	W	3B5h/3D5h	–	46

Note 1: When MDA or Hercules emulation is enabled, the CRTC I/O address should be set to 3B0h-3B7h by setting the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh bit-0) to zero. When CGA emulation is enabled, the CRTC I/O address should be set to 3D0h-3D7h by setting Misc Output Register bit-0 to 1.

Note 2: In the EGA, all CRTC registers except the cursor (CR0C-CR0F) and light pen (CR10 and CR11) registers are write-only (i.e., no read back). In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03D7) of whether the vertical sync or light pen registers are readable at indices 10-11.

CRTC INDEX REGISTER (CRX)
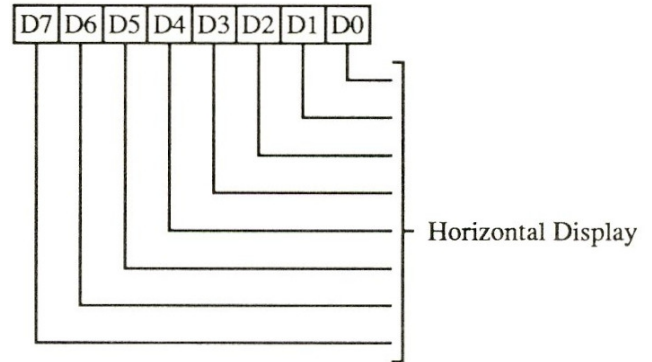*Read/Write at I/O Address 3B4h/3D4h*

D7	D6	D5	D4	D3	D2	D1	D0

— CRTC Index
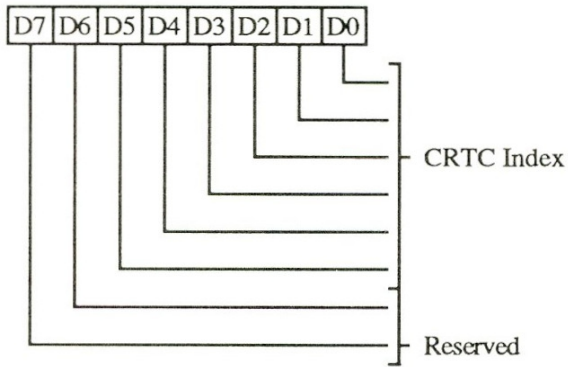
— Reserved

5-0   CRTC data register index

7-6   Reserved (0)

HORIZONTAL TOTAL REGISTER (CR00)
Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 protection
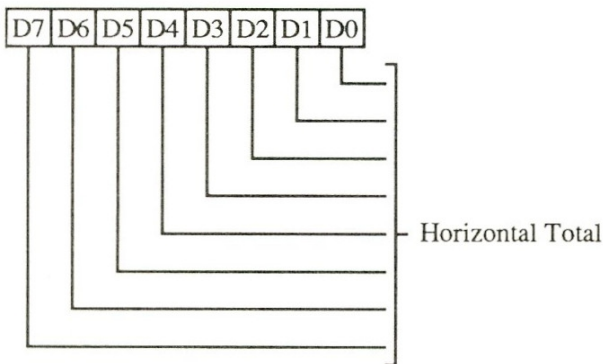
D7	D6	D5	D4	D3	D2	D1	D0

— Horizontal Total

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0   Horizontal Total. Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)
Read/Write at I/O Address 3B5h/3D5h
Index 01h
Group 0 protection

D7	D6	D5	D4	D3	D2	D1	D0

— Horizontal Display

This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0   Number of Characters displayed per scan line - 1.

HORIZONTAL BLANK START REGISTER (CR02)
Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 protection
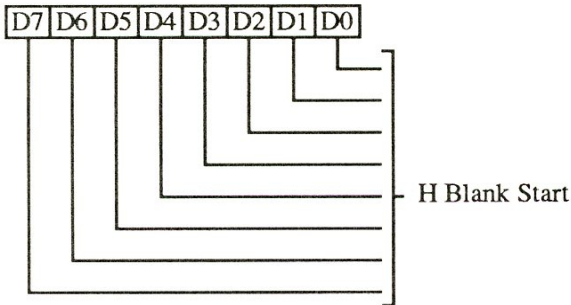
```
D7 D6 D5 D4 D3 D2 D1 D0
```
⊢ H Blank Start

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

HORIZONTAL BLANK END REGISTER (CR03)
Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 protection

```
D7 D6 D5 D4 D3 D2 D1 D0
```
⊢ H Blank End

⊢ DE Skew Control
⊢ Light Pen Reg. Enable

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.
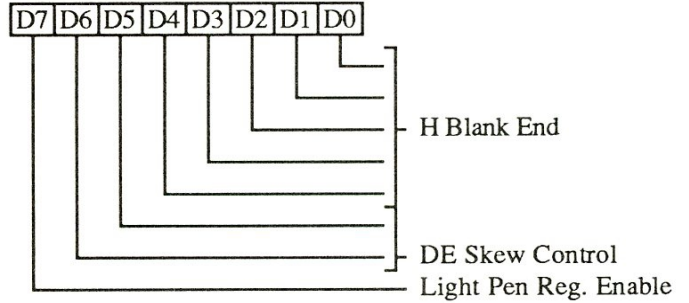
4-0 These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. If the horizontal blank width desired is W clocks, the 5-bit value programmed in this register = [contents of CR02 + W] and 1Fh. The most significant bit is programmed in CR05D7. This bit = [(CR02 + W) and 20h]/20h.

6-5 Display Enable Skew Control: Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Light Pen Reg. Enable: Must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.

HORIZONTAL SYNC START REGISTER (CR04)
Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 protection

Horizontal Sync Start

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.
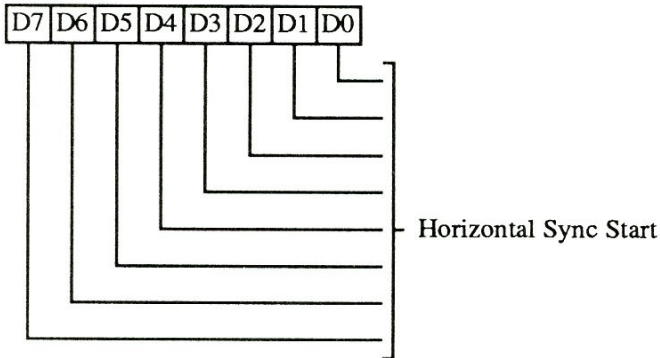
7-0 These bits specify the beginning of Hsync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

HORIZONTAL SYNC END REGISTER (CR05)
Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 protection
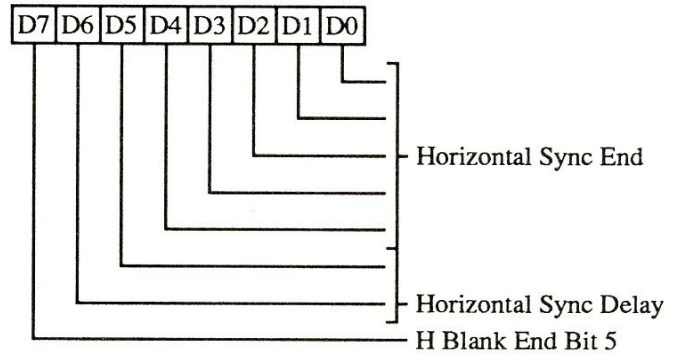
Horizontal Sync End

Horizontal Sync Delay

H Blank End Bit 5

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 Hsync End. Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. If the horizontal sync width desired is N clocks, then these bits = (N + contents of CR04) and 1Fh.

6-5 Horizontal Sync Delay. These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7 Horizontal Blank End Bit 5. Sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)
Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 protection
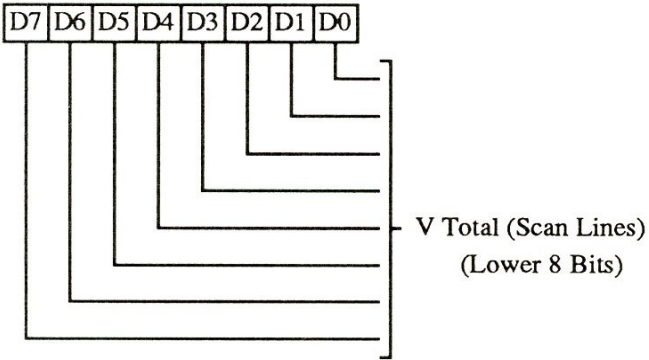
```
D7 D6 D5 D4 D3 D2 D1 D0
```

V Total (Scan Lines)
(Lower 8 Bits)

This register is used in all modes.

7-0   These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count − 2

OVERFLOW REGISTER (CR07)
Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 protection on bits 0-3 and bits 5-7
Group 3 protection on bit 4

```
D7 D6 D5 D4 D3 D2 D1 D0
```

V Total Bit 8
V D. E. End Bit 8
V Sync Start Bit 8
V Blank Start Bit 8
Line Compare Bit 8
V Total Bit 9
V D. E. End Bit 9
V Sync Start Bit 9
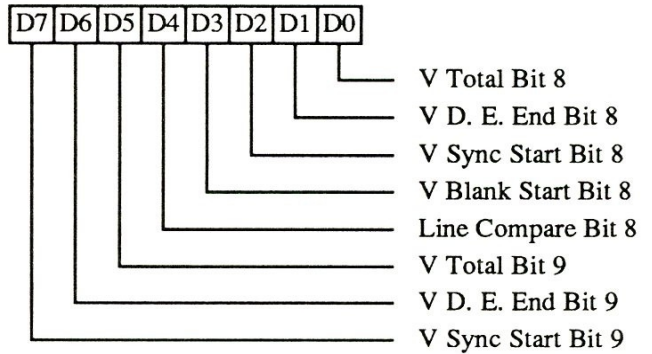
This register is used in all modes.

0   Vertical Total Bit 8
1   Vertical Display Enable End Bit 8
2   Vertical Sync Start Bit 8
3   Vertical Blank Start Bit 8
4   Line Compare Bit 8
5   Vertical Total Bit 9
6   Vertical Display Enable End Bit 9
7   Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)
Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

— Start Row Scan Count

— Byte Panning Control
— Reserved

4-0 These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

6-5 Byte Panning Control. These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.
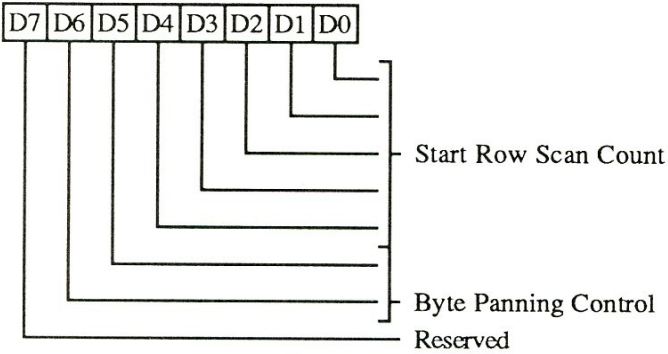
7 Reserved (0)

MAXIMUM SCAN LINE REGISTER (CR09)
Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 protection on bits 0-4
Group 4 Protection on bit 5-7

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

— Scan Lines Per Row

— V Blank Start Bit 9
— Line Compare Bit 9
— Double Scan
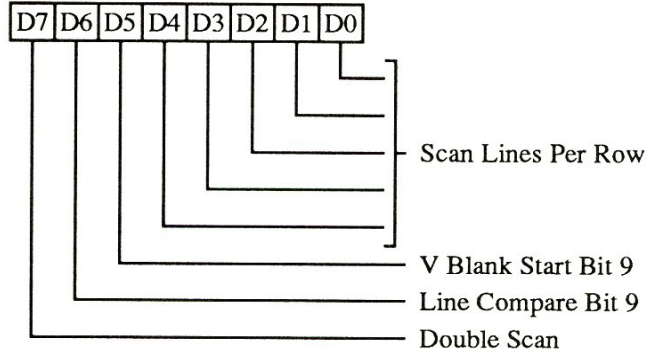
4-0 These bits specify the number of scan lines in a row: Number of scan lines per row = value + 1.

5 Bit 9 of the Vertical Blank Start register

6 Bit 9 of the Line Compare register

7 Double Scan

  0: Normal Operation
  1: Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

CURSOR START SCAN LINE REGISTER (CR0A)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection

D7	D6	D5	D4	D3	D2	D1	D0

- Cursor Start Scan Line
- Cursor off
- Reserved
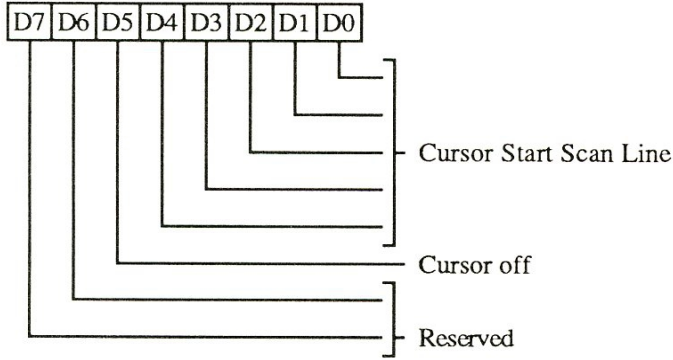
4-0 These bits specify the scan line of the char-
acter row where the cursor display begins.

5 Cursor Off

    0: Text Cursor On
    1: Text Cursor Off

7-6 Reserved (0)

CURSOR END SCAN LINE REGISTER (CR0B)
Read/Write at I/O Address 3B5h/3D5h
Index 0Bh
Group 2 protection

D7	D6	D5	D4	D3	D2	D1	D0

- Cursor End Scan Line
- Cursor Delay
- Reserved
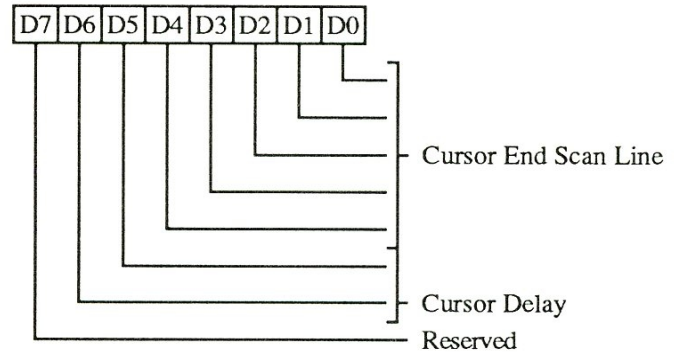
4-0 These bits specify the scan line of a character
row where the cursor display ends: Last
scan line for the block cursor = Value + 1.

6-5 These bits define the number of character
clocks that the cursor is delayed to compen-
sate for internal pipeline delay.

7 Reserved (0)

Note: If the Cursor Start Line is greater than the
Cursor End Line, then no cursor is generated.

START INDEX HIGH REGISTER (CR0C)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ch

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                    ├ Display Start Index High
                       (Upper 8 bits)
```

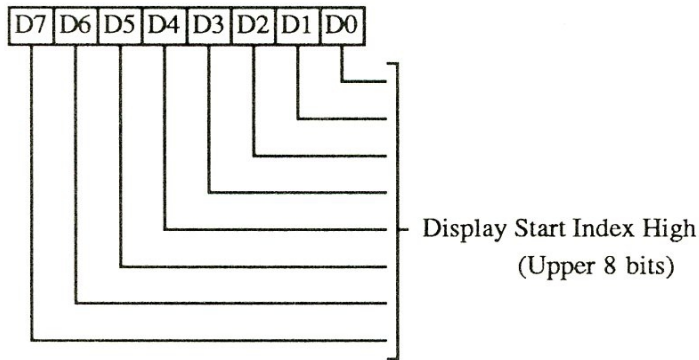**7-0** Upper 8 bits of display start address. In CGA/MDA/Hercules modes, this register wraps around at the 16, 32, and 64 K byte boundaries respectively.

CURSOR LOCATION HIGH REGISTER (CR0E)
Read/Write at I/O Address 3B5h/3D5h
Index 0Eh

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                    ├ Text Cursor Mem. Index
                       (Upper 8 bits)
```

7-0 Upper 8 bits of the memory address where the text cursor is active. In CGA/MDA/Hercules modes, this register wraps around at 16, 32, and 64 K byte boundaries respectively.

START INDEX LOW REGISTER (CR0D)
Read/Write at I/O Address 3B5h/3D5h
Index 0Dh

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                    ├ Display Start Index Low
                       (Lower 8 bits)
```

7-0 Lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

CURSOR LOCATION LOW REGISTER (CR0F)
Read/Write at I/O Address 3B5h/3D5h
Index 0Fh

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                    ├ Text Cursor Mem. Index
                       (Lower 8 bits)
```

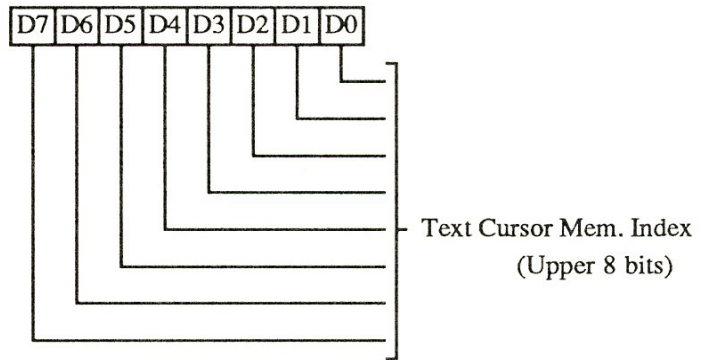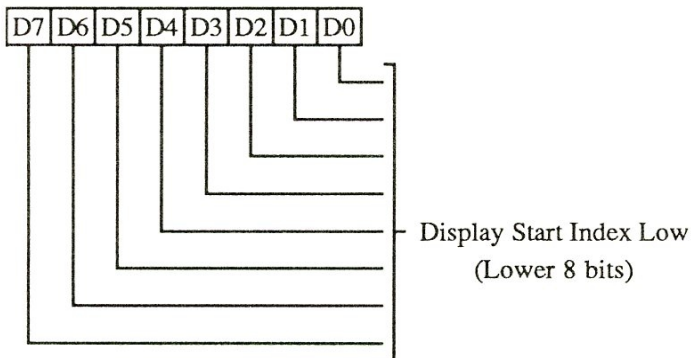**7-0** Lower 8 bits of the memory address where the text cursor is active. In CGA/MDA/Hercules modes, this register wraps around at 16, 32, and 64 K byte boundaries respectively.

LIGHTPEN HIGH REGISTER (CR10)
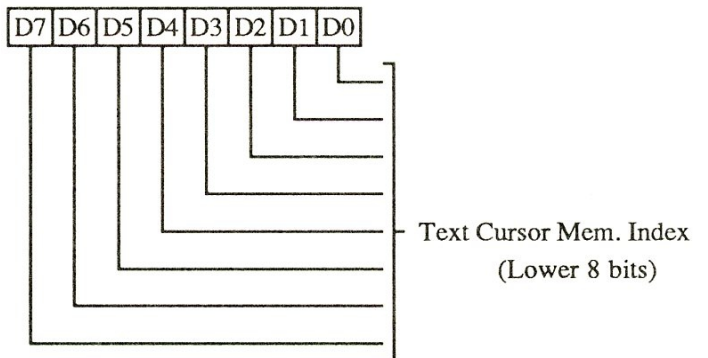*Read only at I/O Address 3B5h/3D5h*
Index 10h

Read-only Register. Effective only in MDA and Hercules modes or when CR03D7 = 0.

LIGHTPEN LOW REGISTER (CR11)
Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register. Effective only in MDA and Hercules modes or when CR03D7 = 0.

VERTICAL SYNC START REGISTER (CR10)
Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- V Sync Start
  (Lower 8 bits)
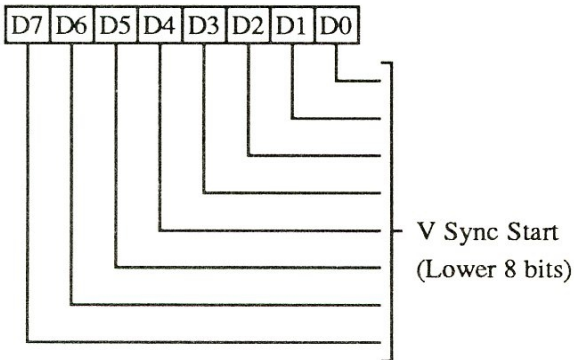
This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03D7=1.

7-0 The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

VERTICAL SYNC END REGISTER (CR11)
Read/Write at I/O Address 3B5h/3D5h
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6 and 7

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- V Sync End
- V Interrupt Clear
- V Interrupt Enable
- Select Refresh Type
- Protect CRTC (Group 0)

This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03D7=1.

3-0 Vertical Sync End. Lower 4 bits of the scan line count that defines the end of vertical sync. If the vertical sync width desired is N lines, then bits 3-0 of this register = (CR10 + N) AND 0Fh.

4 Vertical Interrupt Clear. 0=Clear vertical interrupt generated on the IRQ output; 1=Normal operation. This bit is cleared by RESET.

5 Vertical Interrupt Enable. 0: Enable vertical interrupt; 1: Disable vertical interrupt. This bit is cleared by RESET.

6 Select Refresh Type:

   0: 3 refresh cycles per scan line
   1: 5 refresh cycles per scan line

7 Group Protect 0. This bit is logically ORed with XR15D6 to determine the protection for group 0 registers. This bit is cleared by RESET.

   0: Enable writes to CR00-CR07
   1: Disable writes to CR00-CR07

CR07D4 (Line Compare bit-9) is not affected by this bit.

VERTICAL DISPLAY ENABLE END REGISTER (CR12)
Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

— V Display Enable End (Lower 8 bits)

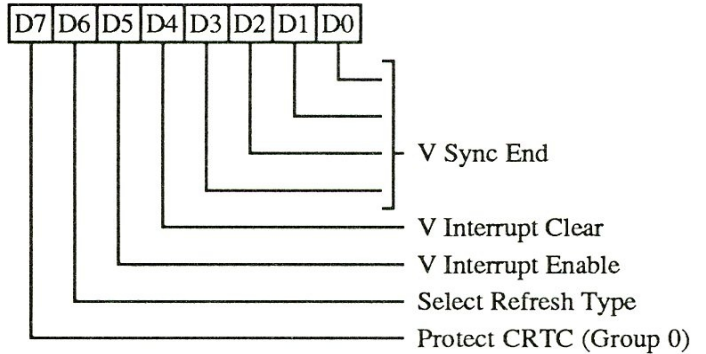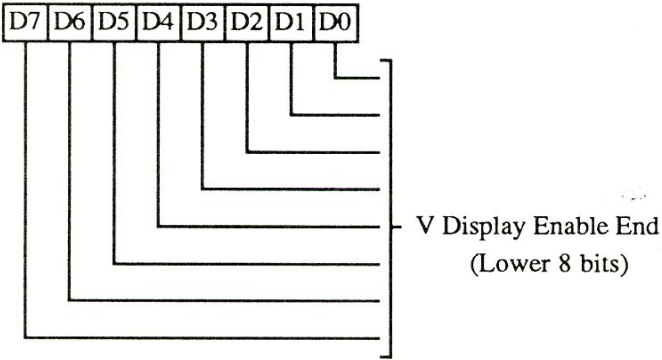**7-0** These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1.

OFFSET REGISTER (CR13)
Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

— Display Buffer Width
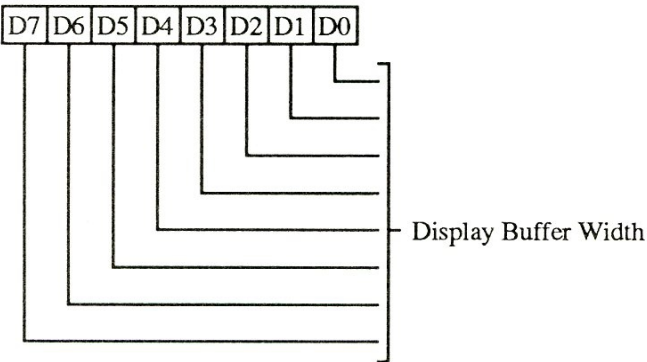
7-0 Display Buffer Width. The byte starting address of the next display row = Byte Start Address for current row + K* (CR13 + Z/2), where Z = bit defined in XR0D and K = 2 in byte mode, K = 4 in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)
Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

— Underline Position

— Count by 4
— Doubleword Mode
— Reserved
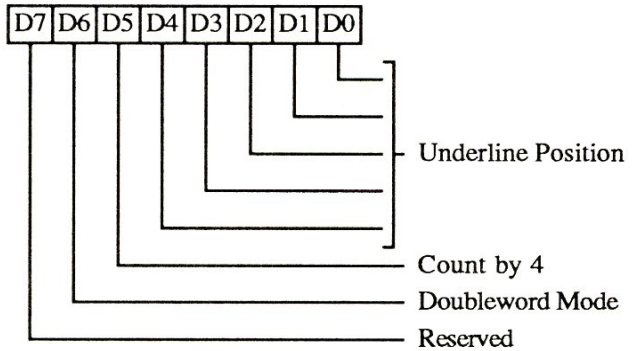
4-0 These bits specify the underline's scan line position within a character row. Value = Actual scan line number - 1.

5 Count by 4 for Doubleword Mode. 0: Frame Buffer Address is incremented by 1 or 2; 1: Frame Buffer Address is incremented by 4 or 2. See CR17D3 for further details.

6 Doubleword Mode. 0: Frame Buffer Address is byte or word address; 1: Frame Buffer Address is doubleword address. Used in conjunction with CR17D6 to select the display memory addressing mode.

7 Reserved (0)

VERTICAL BLANK START REGISTER (CR15)
Read/Write at I/O Address 3B5h/3D5h
Index 15h
Group 4 protection
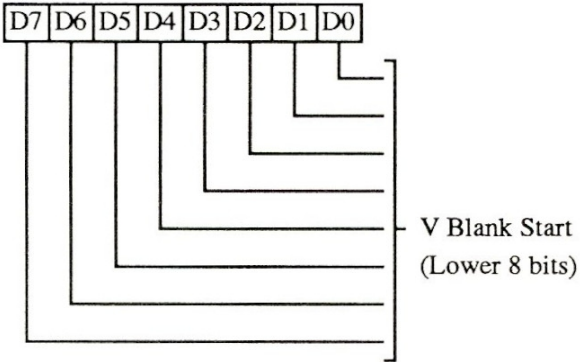
```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

─ V Blank Start

(Lower 8 bits)

This register is used in all modes.

7-0 These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

VERTICAL BLANK END REGISTER (CR16)
Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

─ V Blank End

(Lower 8 bits)
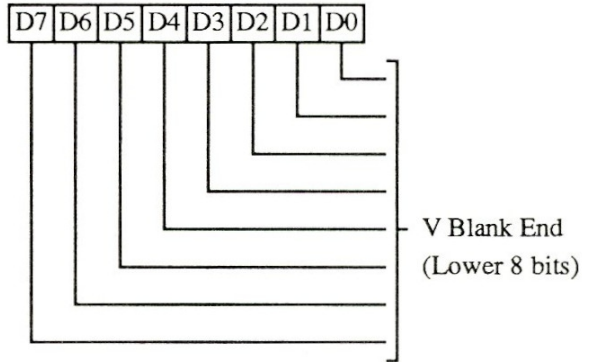
This register is used in all modes.

7-0 End Vertical Blank. These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. If the vertical blank width desired is Z lines these bits = (Vertical Blank Start + Z) and 0FFh.

CRT MODE CONTROL REGISTER (CR17)
Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0,1 and 3-7
Group 4 Protection for bit 2.

D7	D6	D5	D4	D3	D2	D1	D0

- Compatibility Mode
- Select Row Scan Ctr
- Vsync Select
- Count by 2
- Reserved
- Address Wrap
- Word/Byte Mode
- CRTC Reset
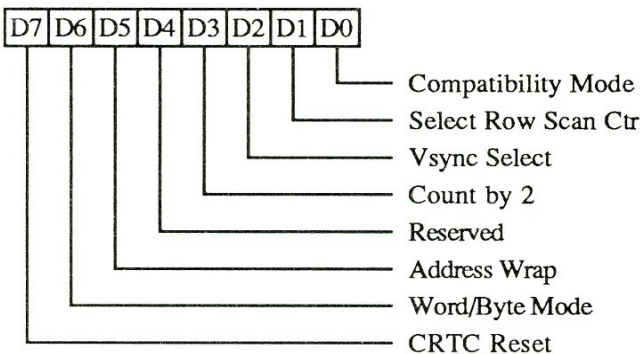
0 Compatibility Mode Support. This bit allows compatibility with the IBM CGA two-bank graphics mode.

> 0: The character row scan line counter bit 0 is substituted for memory address bit 13 during active display time.
> 1: normal operation, no substitution takes place.

1 Select Row Scan Counter. This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system.

> 0: Substitute character row scan line counter bit 1 for memory address bit 14 during active display time.
> 1: normal operation, no substitution takes place.

2 Vertical Sync Select. This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3 Count By Two

> 0: Memory address counter is incremented every character clock
> 1: Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

> **Note:** This bit is used in conjunction with CR14D5. The net effect is as follows:

CR14D5	CR17D3	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

> **Note:** In Hercules graphics and Hi-res CGA modes, the address inrements every two clocks.

4 Reserved (0)

5 Address Wrap (effective only in word mode.)

> 0: Wrap display memory address at 16 Kbytes. This is used in IBM CGA mode.
> 1: Normal operation (extended mode).

6 Word Mode or Byte Mode.

> 0: Word Mode is selected. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output.
> 1: Select byte mode.

> **Note:** This bit is used in conjunction with CR14D6 to select byte, word, or double word memory addressing as follows:

CR14D6	CR17D6	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

7 Hardware Reset (This bit is cleared by RESET)

> 0: Force HSYNC and VSYNC to be inactive. No other registers or outputs affected.
> 1: Normal Operation.

Display memory addresses are affected by CR17D6 as shown in the table below:

Logical Memory Address	Physical Memory Address		
	Byte Mode	Word Mode	Double Word Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * NOT CR17D5 + A15 * CR17D5
Note 2 = A12 xor (A14 * XR04D2)
Note 3 = A13 xor (A15 * XR04D2)

LINE COMPARE REGISTER (CR18)
Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 protection

Line Compare Target
(Lower 8 bits)
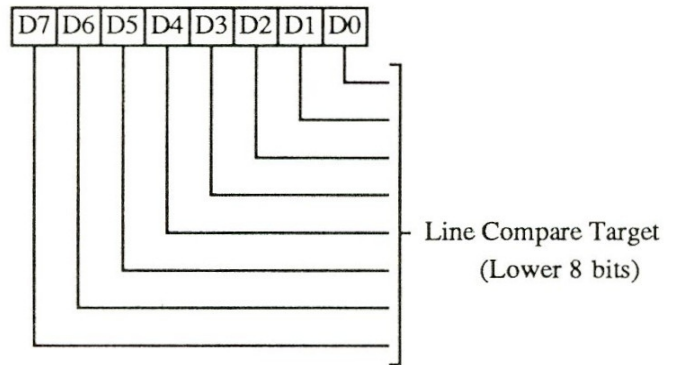
7-0 These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09D7).

MEMORY DATA LATCH REGISTER (CR22)
Read only at I/O Address 3B5h/3D5h
Index 22h

D7	D6	D5	D4	D3	D2	D1	D0

- Data Latch n Bit 7
- Data Latch n Bit 6
- Data Latch n Bit 5
- Data Latch n Bit 4
- Data Latch n Bit 3
- Data Latch n Bit 2
- Data Latch n Bit 1
- Data Latch n Bit 0
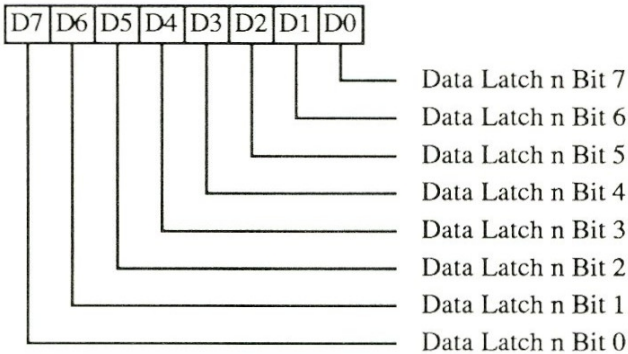
This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04D0&1) and is in the range 0-3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)
Read only at I/O Address 3B5h/3D5h
Index 24h

D7	D6	D5	D4	D3	D2	D1	D0

- Index (0) / Data (1)
- Reserved
- Palette Address Source

- Attribute
- Controller
- Index
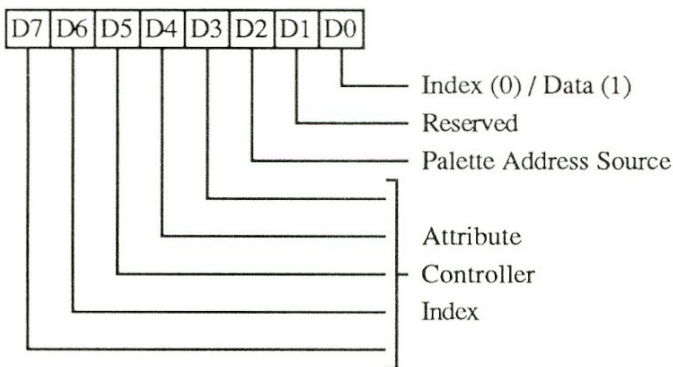
This register may be used to read back the state of the attribute controller index/data latch.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

CLEAR VERTICAL DISPLAY ENABLE FFh (CR3x)
Write only at I/O Address 3B5h/3D5h
Index 3xh

D7	D6	D5	D4	D3	D2	D1	D0

- Clear Vert Disp Ena FF

- Ignored
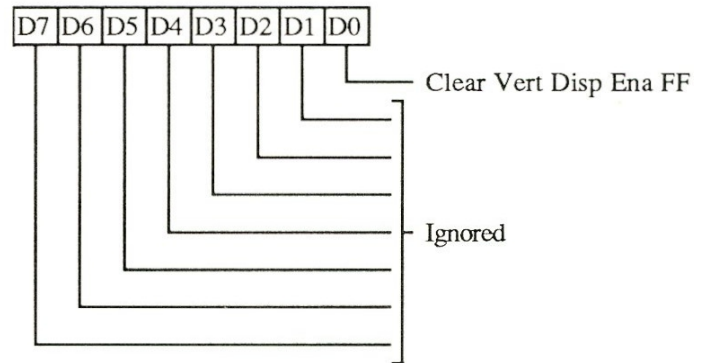
Writing odd data values to CRTC index 30-3Fh causes the vertical display enable flip-flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer vertical retrace period. There are two side effects of terminating vertical display enable early: first, the screen blanks early for one frame causing a minor visual disturbance and second, the sequencer gives more display memory cycles to the CPU because vertical display is not enabled.

Reads from this register are not decoded and will return indeterminate data.

This is a standard VGA register which was not documented by IBM.

82C455 Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	W	3CEh	1	47
GR00	Set/Reset	00h	RW	3CFh	1	47
GR01	Enable Set/Reset	01h	RW	3CFh	1	48
GR02	Color Compare	02h	RW	3CFh	1	48
GR03	Data Rotate	03h	RW	3CFh	1	49
GR04	Read Map Select	04h	RW	3CFh	1	49
GR05	Graphics mode	05h	RW	3CFh	1	50
GR06	Miscellaneous	06h	RW	3CFh	1	52
GR07	Color Don't Care	07h	RW	3CFh	1	52
GR08	Bit Mask	08h	RW	3CFh	1	52

GRAPHICS CONTROLLER INDEX REGISTER (GRX)
Write only at I/O Address 3CEh
Group 1 Protection

Index to Graphics Controller Data Registers
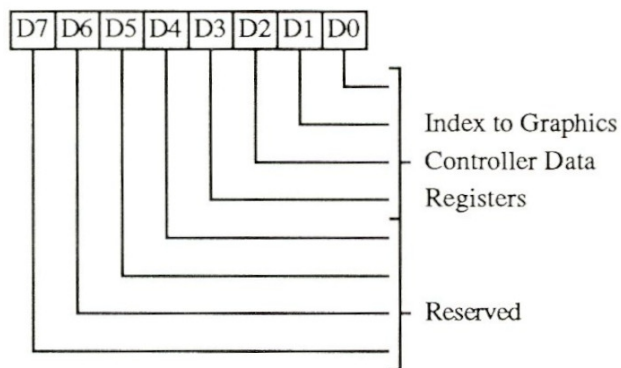
Reserved

3-2 4-bit index to Graphics Controller registers

7-4 Reserved (0)

SET/RESET REGISTER (GR00)
Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection

Set/Reset Bit 0
Set/Reset Bit 1
Set/Reset Bit 2
Set/Reset Bit 3

Reserved
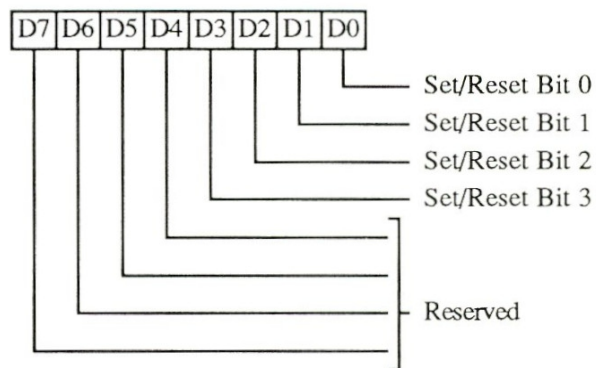
The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

3-0 When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Rest register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

7-4 Reserved (0)

ENABLE SET/RESET REGISTER (GR01)
Read/Write at I/O Address 3CFh
Index 01h
Group 1 Protection

D7	D6	D5	D4	D3	D2	D1	D0

- Enable Set/Reset Bit 0
- Enable Set/Reset Bit 1
- Enable Set/Reset Bit 2
- Enable Set/Reset Bit 3

- Reserved

3-0 This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

    0: The corresponding plane is written with the data from the CPU data bus

    1: The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4 Reserved (0)

COLOR COMPARE REGISTER (GR02)
Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection

D7	D6	D5	D4	D3	D2	D1	D0

- Color Compare (Plane 0)
- Color Compare (Plane 1)
- Color Compare (Plane 2)
- Color Compare (Plane 3)

- Reserved

3-0 This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit, a mis-match returns a logical 0.

7-4 Reserved (0)

DATA ROTATE REGISTER (GR03)
Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                    └─── Rotate Count 0
                 └────── Rotate Count 1
              └───────── Rotate Count 2
        ┤──────────────── Function Select
  ┤──────────────────── Reserved
```

2-0 These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

4-3 These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data, Latches are updated;
0	1	Logical 'AND' between Data and latched data;
1	0	Logical 'OR' between Data and latched data;
1	1	Logical 'XOR' between Data and latched data.

7-5 Reserved (0)

READ MAP SELECT REGISTER (GR04)
Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                    └─── Map Select 0
                 └────── Map Select 1
        ┤──────────────── Reserved
```

1-0 This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

The four memory maps are selected as follows:

Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2 Reserved (0)

GRAPHICS MODE REGISTER (GR05)
Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0
- Write Mode
- Reserved
- Read Mode
- Odd/Even Mode
- Shift Register Mode
- Reserved
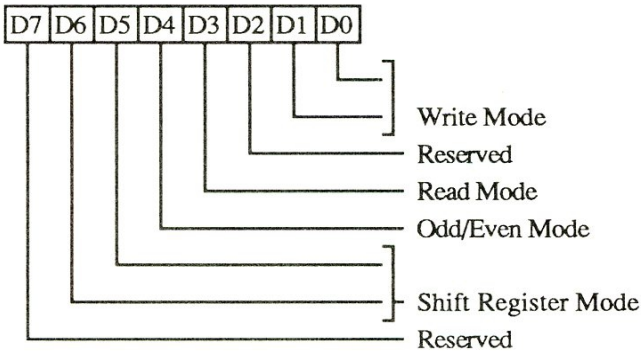
1-0 These bits specify the Write Mode as follows: (For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data).

D1	D0	Write Mode
0	0	**Write mode 0**. Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.
0	1	**Write mode 1**. Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.
1	0	**Write mode 2**. The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the

processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.

1	1	**Write mode 3**. The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value.

A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches.

A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register.

The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2 Reserved (0)

3 This bit specifies the Read Mode as follows:

0: The CPU reads data from one of the planes as selected in the Read Map Select register.

1: The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

4   Odd/Even Mode:

        0:    All CPU addresses sequentially access all planes

        1:    Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for IBM CGA-compatible memory organization.

6-5   Shift Register Mode. These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If the data bits in the memory planes (0-3) are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

65	Last Bit Shifted Out			Shift Direction →				1st Bit Shifted Out	Output to:
00:	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit3
01:	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit3
1x:	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit1
	M3D2	M2D2	M3D6	M2D6	M1D3	M1D6	M0D2	M0D6	Bit2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit3

Note: If the Shift Register is not loaded every character clock (see SR01D2&4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

7   Reserved (0)

MISCELLANEOUS REGISTER (GR06)
Read/Write at I/O Address 3CFh
Index 06h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

```
                              Graphics/Text Mode
                              Chain Odd/Even Planes

                              Memory Map Mode

                              Reserved
```

COLOR DON'T CARE REGISTER (GR07)
Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

```
                              Ignore Color Plane 0
                              Ignore Color Plane 1
                              Ignore Color Plane 2
                              Ignore Color Plane 3

                              Reserved
```
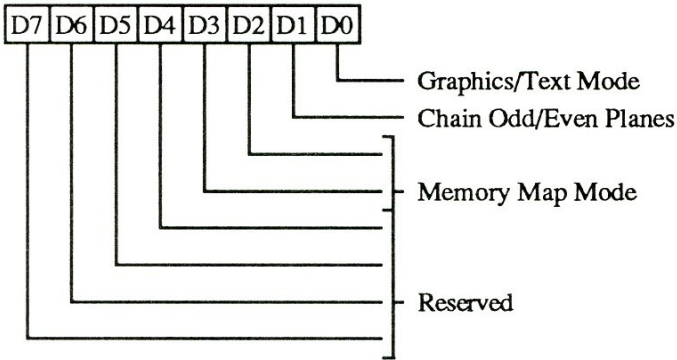
0 Graphics/Text Mode:

  0: Text Mode
  1: Graphics mode

1 Chain Odd/Even Planes. This mode can be used to double the address space into display memory.

  1: CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:

   A0 = 0: select planes 0 and 2
   A0 = 1: select planes 1 and 3

  0: A0 not replaced

3-2 Memory Map mode. These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

3-0 Ignore Color Plane (0-3):

  0: This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.

  1: The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)
Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection

D7	D6	D5	D4	D3	D2	D1	D0

0=Immune to change
1=Change permitted
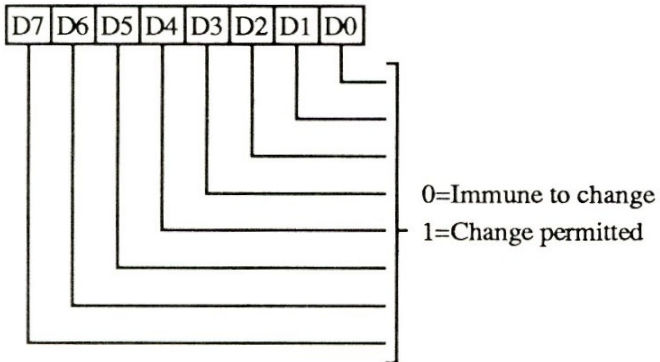
7-0   This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the 82C455), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

   0:   The corresponding bit in each of the four memory planes is written from the corresponding bit in the latches.

   1:   Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted.

82C455 Attribute Controller
and Color Palette Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	RW	3C0h	1	55
AR00-AR0F	Internal Color Palette Data	00-0Fh	RW	3C0h/3C1h	1	56
AR10	Mode Control	10h	RW	3C0h/3C1h	1	56
AR11	Overscan Color	11h	RW	3C0h/3C1h	1	57
AR12	Color Plane Enable	12h	RW	3C0h/3C1h	1	57
AR13	Horizontal Pixel Panning	13h	RW	3C0h/3C1h	1	58
AR14	Pixel Pad	14h	RW	3C0h/3C1h	1	58
DACMASK	External Color Palette Pixel Mask	–	RW	3C6h	6	59
DACSTATE	DAC State	–	R	3C7h	–	59
DACRX	External Color Palette Read-Mode Index	–	W	3C7h	6	60
DACX	External Color Palette Index (for 3C9h)	–	RW	3C8h	6	60
DACDATA	External Color Palette Data	00-FFh	RW	3C9h	6	60

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

ATTRIBUTE INDEX REGISTER (ARX)
Read/Write at I/O Address 3C0h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Index to Attribute Controller Data Registers

Video Enable

Reserved
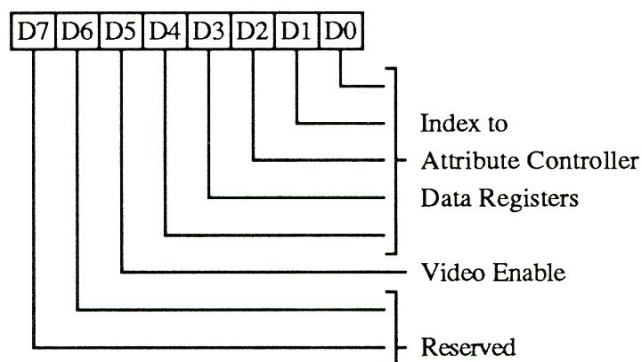
4-0 These bits point to one of the internal registers of the Attribute Controller.

5 Enable Video:

0: Disables the video, allowing the Attribute Controller color registers to be accessed by the CPU

1: Enables the video and causes the Attribute Controller Color registers (AR00-AR0F) to be inaccessible by the CPU.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER COLOR PALETTE DATA REGISTERS (AR00-AR0F)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection or XR63D6

```
D7 D6 D5 D4 D3 D2 D1 D0
                     └─── Blue
                  └────── Green
               └───────── Red
            └──────────── Secondary Blue
         └─────────────── Secondary Green
      └────────────────── Secondary Red
 └─┴────────────────────── Reserved
```
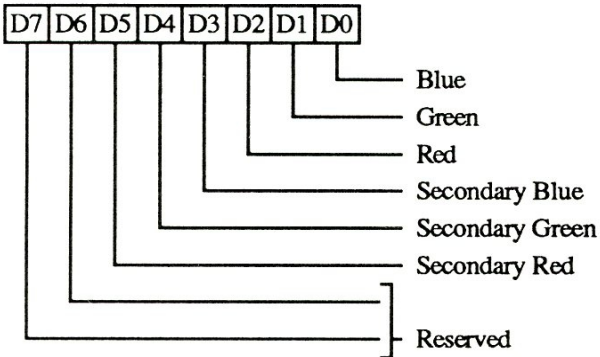
5-0 These bits are the color value in the respective palette register as pointed to by the index register.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection

```
D7 D6 D5 D4 D3 D2 D1 D0
                     └─── Text/Graphics Mode
                  └────── Mono/Color Display
               └───────── Enable Line Graphics
            └──────────── Select Background
         └─────────────── Reserved
      └────────────────── Horizontal Split Screen
   └───────────────────── 256 Color
└──────────────────────── Video Output 4-5 Select
```
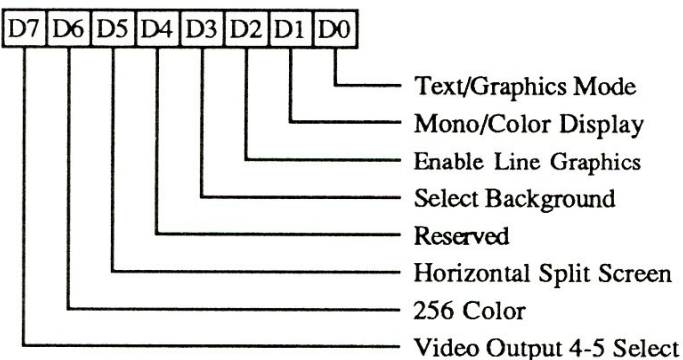
0 Text/Graphics Mode:

    0: Select text mode
    1: Select graphics mode

1 Monochrome/Color Display

    0 Select color display attributes
    1 Select mono display attributes

2 Enable Line Graphics Character Codes. This bit is dependent on bit 0 of the Override register.

    0: Make the ninth pixel appear the same as the background

    1: For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3 Enable Blink/Select Background Intensity. The blinking counter is clocked by the VSYNC signal. The Blink frequency is defined in the Blink Rate Control Register (XR60).

    0: Disable Blinking and enable text mode background intensity

    1: Enable the blink attribute in text and graphics modes.

4 Reserved (0)

5 Split Screen Horizontal Panning Mode

    0: Scroll both screens horizontally as specified in the Pixel Panning register

    1: Scroll horizontally only the top screen as specified in the Pixel panning register

6 256 Color Output Assembler

    0: 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock

    1: Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

7 Video Output 5-4 Select:

    0: Video bits 4 and 5 are generated by the internal Attribute Controller color palette registers

    1: Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14)

OVERSCAN COLOR REGISTER (AR11)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
— Overscan Color
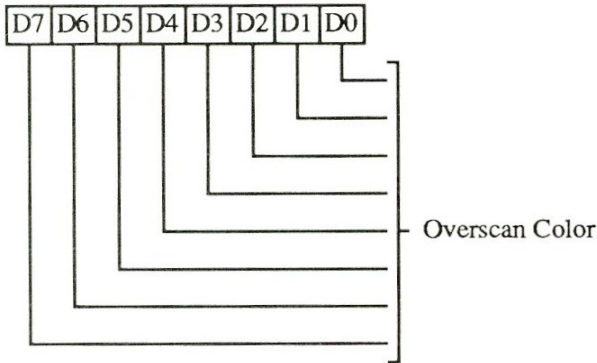
7-0 Overscan Color. These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
— Color Plane 0 Enable
— Color Plane 1 Enable
— Color Plane 2 Enable
— Color Plane 3 Enable
— Display Status Select
— Reserved
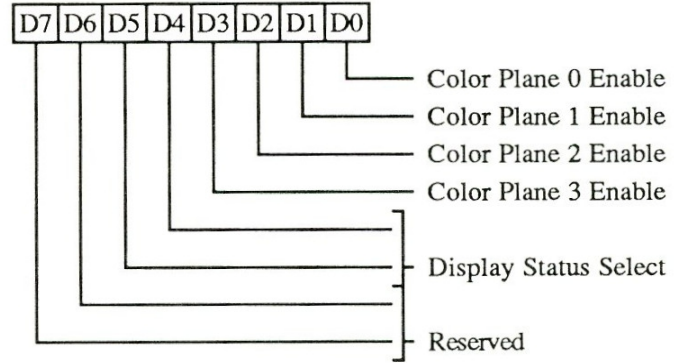
3-0 Color Plane (0-3) Enable

> 0: Force the corresponding color plane pixel bit to 0 before it addresses the color palette

> 1: Enable the plane data bit of the corresponding color plane to pass

5-4 Display Status Select. Select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

		Status Register 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6 Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)
Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 13h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Horizontal Pixel Panning
- Reserved
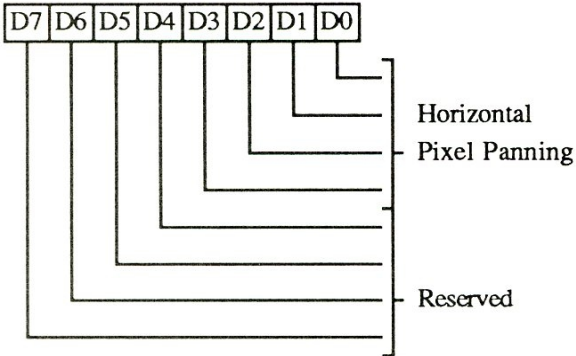
ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)
Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 14h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Video bit-4 if AR10D7=1
- Video bit-5 if AR10D7=1
- Video bit-6 if not 256-color
- Video bit-7 if not 256-color
- Reserved
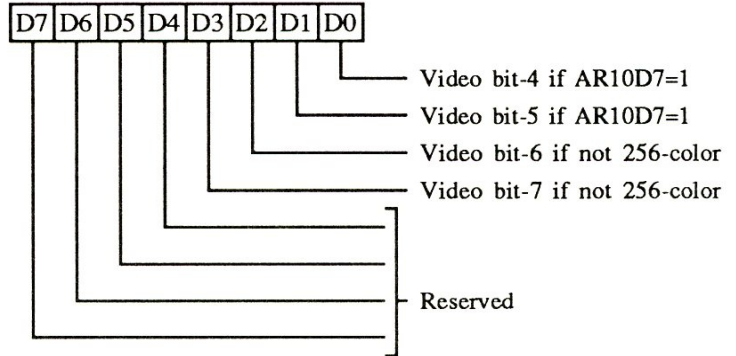
3-0   Horizontal Pixel Panning. These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixels/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixels/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10D6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

<div align="center">

Number of Pixels Shifted

AR13	9-dot mode	8-dot mode	256-color mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

</div>

7-4   Reserved (0)

1-0   These bits are output as video bits 4 and 5 when AR10D7 = 1. They are disabled in the 256 color mode.

3-2   These bits are output as video bits 6 and 7 in all modes except 256-color mode.

7-4   Reserved (0)

EXTERNAL COLOR PALETTE
PIXEL MASK REGISTER (DACMASK)
Read/Write at I/O Address 3C6h
Group 6 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

—————— Pixel Mask Bit-0
—————— Pixel Mask Bit-1
—————— Pixel Mask Bit-2
—————— Pixel Mask Bit-3
—————— Pixel Mask Bit-4
—————— Pixel Mask Bit-5
—————— Pixel Mask Bit-6
—————— Pixel Mask Bit-7
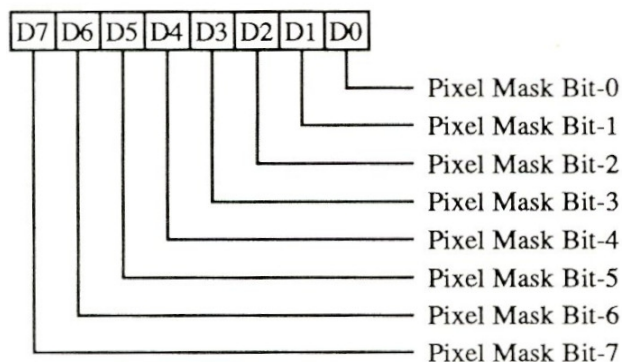
The contents of this register are logically ANDed with the 8 bits of video data coming into the external color palette. Zero bits in this register therefore cause the corresponding address input to the external color palette to be zero. For example, if this register is programmed with 7, only external color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

This register is physically located in the external color palette chip (used for displaying analog data to the CRT). Reads from this I/O location cause the PALRD/ pin to be asserted. Writes to this I/O location cause the PALWR/ pin to be asserted. The functionality of this port is determined by the external palette chip.

EXTERNAL COLOR PALETTE
STATE REGISTER (DACSTATE)
Read only at I/O Address 3C7h

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

—————— Palette State 0
—————— Palette State 1
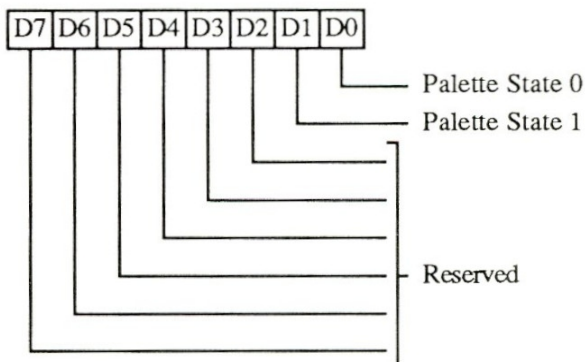
—————— Reserved

1-0 Status bits indicate the I/O address of the last CPU write to the external DAC/Color Palette:

    00   The last write was to 3C8h (write mode)

    11   The last write was to 3C7h (read mode)

7-2 Reserved (0)

To allow saving and restoring the state of the video subsystem, this register is required since the external color palette chip automatically increments its index register differently depending on whether the index is written at 3C7h or 3C8h.

This register is physically located in the 82C455 chip (PALRD/ is *not* asserted for reads from this I/O address).

EXTERNAL COLOR PALETTE
READ-MODE INDEX REGISTER (DACRX)
Write only at I/O Address 3C7h
Group 6 Protection

EXTERNAL COLOR PALETTE
INDEX REGISTER (DACX)
Read/Write at I/O Address 3C8h
Group 6 Protection

D7	D6	D5	D4	D3	D2	D1	D0

- Color Palette Index 0
- Color Palette Index 1
- Color Palette Index 2
- Color Palette Index 3
- Color Palette Index 4
- Color Palette Index 5
- Color Palette Index 6
- Color Palette Index 7

EXTERNAL COLOR PALETTE
DATA REGISTERS (DACDATA 00-FF)
Read/Write at I/O Address 3C9h
Index 00h-FFh
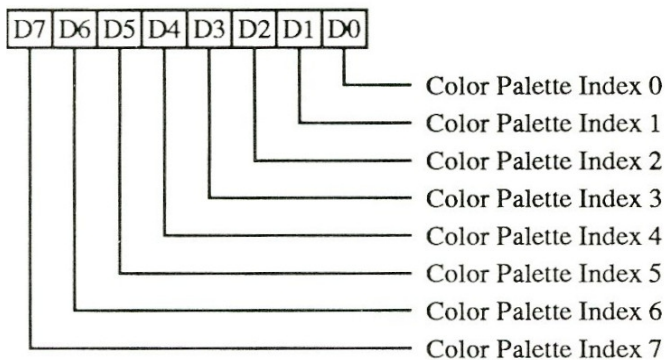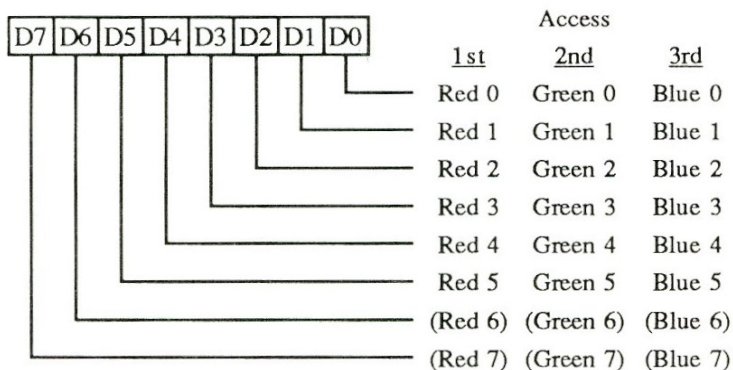*Group 6 Protection*

D7	D6	D5	D4	D3	D2	D1	D0

Access		
1st	2nd	3rd
Red 0	Green 0	Blue 0
Red 1	Green 1	Blue 1
Red 2	Green 2	Blue 2
Red 3	Green 3	Blue 3
Red 4	Green 4	Blue 4
Red 5	Green 5	Blue 5
(Red 6)	(Green 6)	(Blue 6)
(Red 7)	(Green 7)	(Blue 7)

The color palette index and data registers are physically located in the external color palette chip. The index register is used to point to one of 256 data registers. Each data register is either 18 or 24 bits in length depending on the type of palette chip used (6 or 8 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then repeated for the next

location if desired (the index is incremented automatically by the palette chip).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register internal to the color palette chip. The save register (not the index register) is used internally by the palette chip to point at the current data register. When the index value is written to 3C7h (**read mode**), it is written to both the index register and the save register, then the index register is <u>automatically incremented</u>. When the index value is written to 3C8h (**write mode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette chip. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment the palette chip internal RGB sequence counter.

The palette chip internal save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The 82C455 therefore saves the state of which port (3C7h or 3C8h) was last written and returns that information on reads from 3C7h (PALRD/ is only asserted on reads from 3C8h and <u>not</u> on reads from 3C7h). Writes to 3C7h or 3C8h cause the PALWR/ pin to be asserted.

The functionality of the index and data ports is determined by the external palette chip.
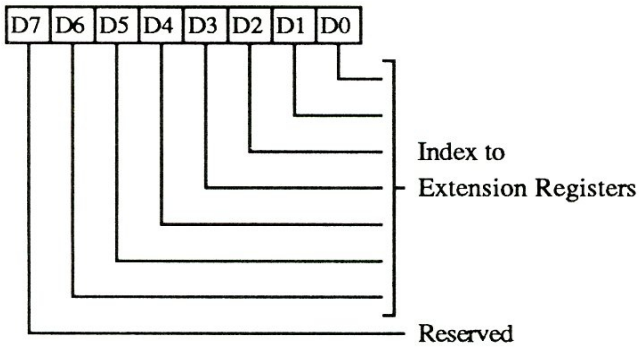
82C455 Extension Registers

Register Mnemonic	Register Group	Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	–	Extension Register Index	–	RW	3B6h / 3D6h	- x x x x x x x	62
XR00	Misc	Chip Version	00h	R	3B7h / 3D7h	0 0 1 0 r r r r	62
XR01	Misc	DIP Switch	01h	R	3B7h / 3D7h	- d d d d d d d	62
XR02	Misc	CPU Interface	02h	RW	3B7h / 3D7h	x x 0 0 0 0 0 0	63
XR03	Misc	ROM Decode	03h	RW	3B7h / 3D7h	- - - - - - - 0	63
XR04	Misc	Memory Mode	04h	RW	3B7h / 3D7h	- - - - 0 0 0 0	63
XR0B	Misc	CPU Paging	0Bh	RW	3B7h / 3D7h	- - - - - - 0 0	65
XR5F	Misc	Power Down Mode Refresh	5Fh	RW	3B7h / 3D7h	x x x x x x x x	81
XR7F	Misc	Diagnostic	7Fh	RW	3B7h / 3D7h	x x 0 0 0 0 0 0	86
XR08	General	General Purpose Output Select B	08h	RW	3B7h / 3D7h	- - - - - - 0 0	64
XR09	General	General Purpose Output Select A	09h	RW	3B7h / 3D7h	- - - - - - 0 0	64
XR0D	General	Auxiliary Offset	0Dh	RW	3B7h / 3D7h	- - - - - - 0 0	65
XR28	General	Video Interface	28h	RW	3B7h / 3D7h	- - - - 0 0 0 0	72
XR2B	General	Default Video	2Bh	RW	3B7h / 3D7h	0 0 0 0 0 0 0 0	72
XR14	Compatibility	Emulation Mode	14h	RW	3B7h / 3D7h	0 0 0 0 x x 0 0	66
XR15	Compatibility	Write Protect	15h	RW	3B7h / 3D7h	- 0 0 0 0 0 0 0	67
XR16	Compatibility	Trap Enable	16h	RW	3B7h / 3D7h	- - 0 0 0 0 0 0	68
XR17	Compatibility	Trap Status	17h	RW	3B7h / 3D7h	- - 0 0 0 0 0 0	68
XR7E	Compatibility	CGA Color Select	7Eh	RW	3B7h / 3D7h	- - x x x x x x	86
XR18	Alternate	Alternate H Display End	18h	RW	3B7h / 3D7h	x x x x x x x x	69
XR19	Alternate	Alternate H Sync Start	19h	RW	3B7h / 3D7h	x x x x x x x x	69
XR1A	Alternate	Alternate H Sync End	1Ah	RW	3B7h / 3D7h	- - - x x x x x	70
XR1B	Alternate	Alternate H Total	1Bh	RW	3B7h / 3D7h	x x x x x x x x	70
XR1C	Alternate	Alternate H Blank Start or End	1Ch	RW	3B7h / 3D7h	x x x x x x x x	71
XR1D	Alternate	Alternate H Blank End or Start	1Dh	RW	3B7h / 3D7h	x x x x x x x x	71
XR1E	Alternate	Alternate Offset	1Eh	RW	3B7h / 3D7h	x x x x x x x x	72
XR54	Alternate	Alternate Miscellaneous Output	54h	RW	3B7h / 3D7h	x x - - 1 0 - 0	75
XR64	Alternate	Alternate Vertical Total	64h	RW	3B7h / 3D7h	x x x x x x x x	83
XR65	Alternate	Alternate Overflow	65h	RW	3B7h / 3D7h	x x x - - x x x	83
XR66	Alternate	Alternate Vertical Sync Start	66h	RW	3B7h / 3D7h	x x x x x x x x	84
XR67	Alternate	Alternate Vertical Sync End	67h	RW	3B7h / 3D7h	- - - - x x x x	84
XR68	Alternate	Alternate Vertical Display Enable End	68h	RW	3B7h / 3D7h	x x x x x x x x	84
XR50	Panel Control	Panel Format	50h	RW	3B7h / 3D7h	x - x x x x x x	73
XR51	Panel Control	Display Type	51h	RW	3B7h / 3D7h	0 0 x x 0 1 0 0	74
XR52	Panel Control	Panel Size	52h	RW	3B7h / 3D7h	- x x x x x x x	74
XR53	Panel Control	Line Graphics Override	53h	RW	3B7h / 3D7h	- - - - - - x x	75
XR5C	Panel Control	Weight Control Clock A	5Ch	RW	3B7h / 3D7h	- - x x x x x x	79
XR5D	Panel Control	Weight Control Clock B	5Dh	RW	3B7h / 3D7h	- - x x x x x x	80
XR6C	Panel Control	Weight Control Clock C	6Ch	RW	3B7h / 3D7h	- - x x x x x x	86
XR5E	Panel Control	ACDCLK Control	5Eh	RW	3B7h / 3D7h	1 x x x x x x x	80
XR55	Compensation	Text Mode 350_A Compensation	55h	RW	3B7h / 3D7h	- - - 1 x x x x	76
XR56	Compensation	Text Mode 350_B Compensation	56h	RW	3B7h / 3D7h	- - - 1 x x x x	76
XR57	Compensation	Text Mode 400 Compensation	57h	RW	3B7h / 3D7h	- - - 1 x x x x	77
XR58	Compensation	Graphics Mode 350 Compensation	58h	RW	3B7h / 3D7h	- x x 0 x x x x	77
XR59	Compensation	Graphics Mode 400 Compensation	59h	RW	3B7h / 3D7h	- x x 0 x x x x	78
XR5A	Compensation	Flat Panel Vertical Display Start 400	5Ah	RW	3B7h / 3D7h	x x x x x x x x	78
XR5B	Compensation	Flat Panel Vertical Display End 400	5Bh	RW	3B7h / 3D7h	x x x x x x x x	79
XR69	Compensation	Flat Panel Vertical Display Start 350	69h	RW	3B7h / 3D7h	x x x x x x x x	84
XR6A	Compensation	Flat Panel Vertical Display End 350	6Ah	RW	3B7h / 3D7h	x x x x x x x x	85
XR6B	Compensation	Flat Panel Vertical Overflow 2	6Bh	RW	3B7h / 3D7h	x x x x x x x x	85
XR60	Color/Attribute	Blink Rate Control	60h	RW	3B7h / 3D7h	1 0 0 0 0 0 1 1	81
XR61	Color/Attribute	Text Color Mapping Control	61h	RW	3B7h / 3D7h	- x x x x x x x	82
XR62	Color/Attribute	Text Color Shift Parameter	62h	RW	3B7h / 3D7h	x x x x x x x x	82
XR63	Color/Attribute	Graphics Color Mapping Control	63h	RW	3B7h / 3D7h	0 0 0 x x x x x	83

Note: These registers can be accessed only if enabled through the Extension Enable register (port 103h during setup).

EXTENSION REGISTER INDEX (XRX)
Read/Write at I/O Address 3B6h/3D6h

```
D7 D6 D5 D4 D3 D2 D1 D0
```

Index to
Extension Registers

Reserved

6-0   Index value used to access the extension registers

7   Reserved (0)

DIP SWITCH REGISTER (XR01)
Read only at I/O Address 3B7h/3D7h
Index 01h

```
D7 D6 D5 D4 D3 D2 D1 D0
```

DIP Switches Status
(read only)
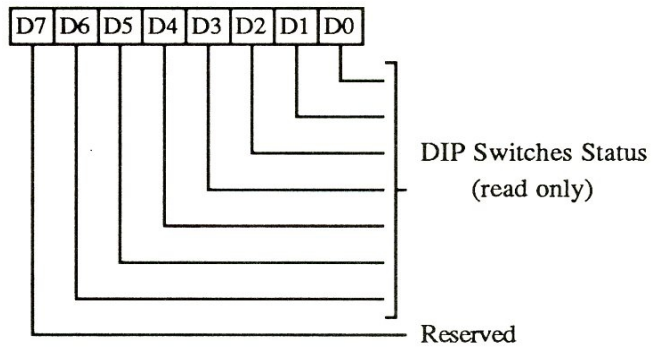
Reserved

6-0   These bits give the state of the DIP switches which are multiplexed with address/data/control signals on pins RFSH/, AEN, ADDHI, BHE/ and A18-A16.

7   Reserved (0)

This register is not related to the EGA Dip Switches.

CHIPS VERSION REGISTER (XR00)
Read only at I/O Address 3B7h/3D7h
Index 00h

```
D7 D6 D5 D4 D3 D2 D1 D0
```
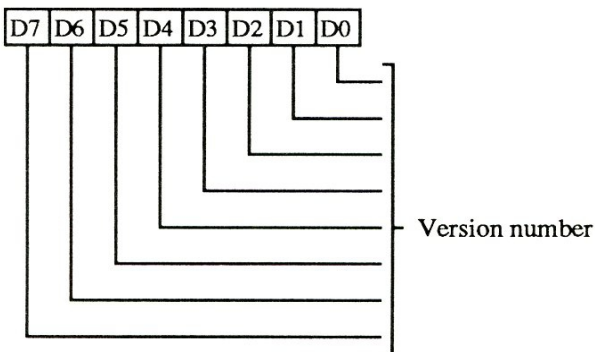
Version number

7-0   This register contains the version number for the 82C455. Values start at 40h and are incremented for every silicon step.

CPU INTERFACE REGISTER (XR02)
Read/Write at I/O Address 3B7h/3D7h
Index 02h

```
D7 D6 D5 D4 D3 D2 D1 D0     16-bit Memory
                             Access Enable
                             Reserved
                             Fast Cycles
                             Attribute Controller
                             Mapping
                             I/O Address Decoding
                             Reserved
                             Attribute FF Status (R/O)
```

0   16-bit Memory Access Enable

      0: Disabled
      1: Enabled

1   Reserved (0)

2   Fast Cycles Enable. Default is disabled (0) on Reset. The Fast option works only with a 16-bit MCA interface (bit-0 =1 and input signal pin PTMC = Low).

4-3   Attribute Controller Mapping

      00: Write Index at 3C0h and Data at 3C0h (8-bit access only). (Default on Reset; VGA type mapping).

      01: Write Index at 3C0h and Data at 3C1h (8 or 16-bit access), the attribute flip-flop is always reset in this mode (16-bit mapping);

      10: Write Index and Data at 3C0h/3C1h (8-bit access only EGA type mapping).

      11: Reserved

5   I/O Address Decoding. This bit affects 3B4/5h, 3D4/5h, 3C0-2h, 3C4/5h, 3CE/Fh, 3BAh, 3BFh and 3D8h. 0: Decode all 16 bits of I/O address (Default on Reset); 1: Decode only the lower 10 bits.

6   Reserved (0)

7   Attribute Flip-flop Status (read only)

      0: Index; 1: Data

ROM DECODE REGISTER (XR03)
Read/Write at I/O Address 3B7h/3D7h
Index 03h

```
D7 D6 D5 D4 D3 D2 D1 D0     ROM Enable
                             Reserved
```
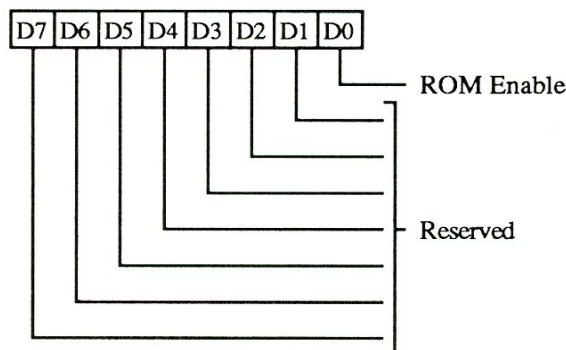
0   ROM Decode Enable

      1: ROM space decode disabled. ROMCS/ always high.
      0: ROM space decode enabled. ROMCS/ active (low) for CPU reads to C0000h-C7FFFh.
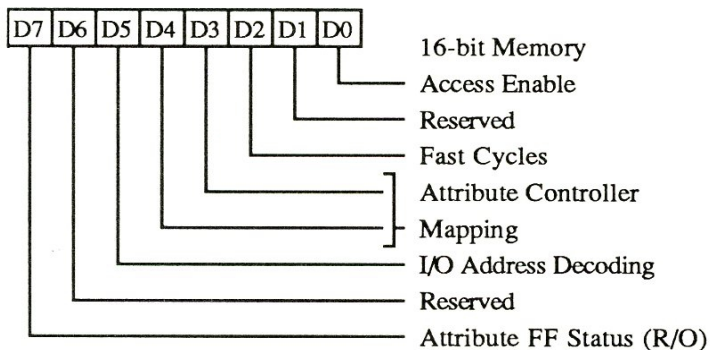
7-1   Reserved (0)

MEMORY MODE REGISTER (XR04)
Read/Write at I/O Address 3B7h/3D7h
Index 04h

```
D7 D6 D5 D4 D3 D2 D1 D0     Reserved
                             Memory Mode
                             Reserved
```
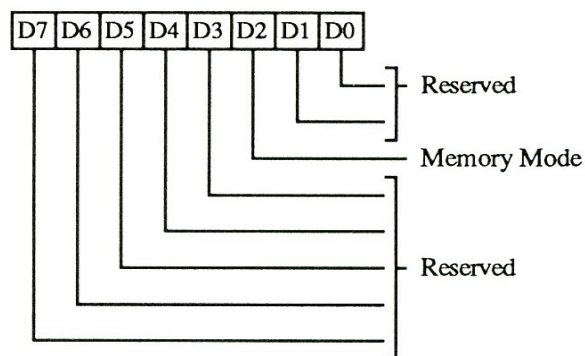
1-0   Reserved (0)

2   Memory mode

      0: Select VGA compatible memory mode (default on reset).
      1: Select extended "Quad Mode". In this mode, display memory is mapped to the CPU address space as 4 pages of 64 K bytes each (or 2 pages of 128 K bytes each). The paging is controlled through the CPU Paging register (XR0B).

7-3   Reserved (0)

General Purpose Output Select Registers

The General Purpose Output Select A and Select B registers contain 2 bits each. Together they allow the CPU to individually switch two 82C455 outputs (ERMEN/ and TRAP/) from their normal function to a software controlled output level (3-state, low, or high).

Each pin's function is selected by 2 bits, one each in the same position in the General Purpose Output Select A Register and the General Purpose Output Select B Register.

Select Bits		
B	**A**	**Pin Function**
0	0	Normal
0	1	3-State
1	0	Force low
1	1	Force high

GENERAL PURPOSE OUTPUT SELECT B REGISTER (XR08)
I/O Address 3B7h/3D7h
Index 08h

D7	D6	D5	D4	D3	D2	D1	D0

— Select Bit B for ERMEN/ pin
— Select Bit B for TRAP/ pin
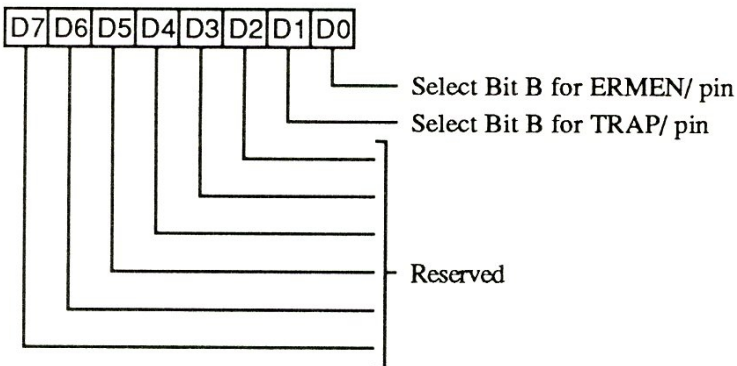
Reserved

Select bit B determines if the pin should be a general purpose output or perform its normal function:

0 Select bit B for ERMEN/ pin

1 Select bit B for TRAP/ pin

7-2 Reserved (0)

GENERAL PURPOSE OUTPUT SELECT A REGISTER (XR09)
I/O Address 3B7h/3D7h
Index 09h

D7	D6	D5	D4	D3	D2	D1	D0

— Select Bit A for ERMEN/ pin
— Select Bit A for TRAP/ pin
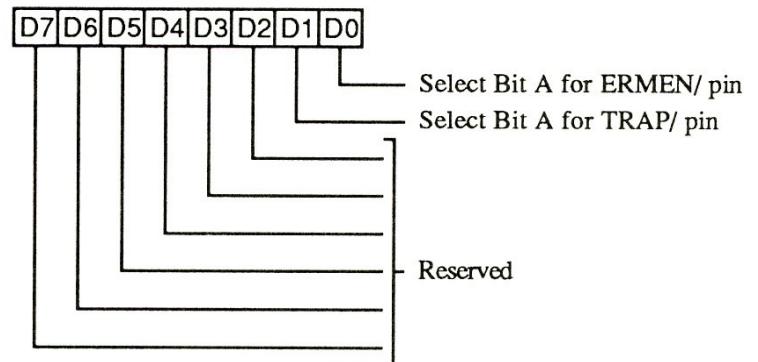
Reserved

If configured as a general purpose output per XR08, select bit A determines if the corresponding pin is high or low:

0 Select bit A for ERMEN/ pin

1 Select bit A for TRAP/ pin

7-2 Reserved (0)

CPU PAGING REGISTER (XR0B)
Read/Write at I/O Address 3B7h/3D7h
Index 0Bh

```
D7 D6 D5 D4 D3 D2 D1 D0
```

— CPU Page Number
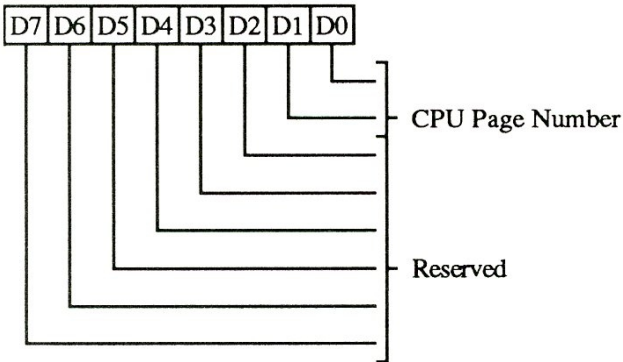
— Reserved

1-0 CPU Page Number. Display memory page number for CPU accesses in Quad mode with extended memory enabled.

7-2 Reserved (0)

AUXILIARY OFFSET REGISTER (XR0D)
Read/Write at I/O Address 3B7h/3D7h
Index 0Dh

```
D7 D6 D5 D4 D3 D2 D1 D0
```

— Lsb of Offset (CR13)
— Lsb of Alt Offset (XR1E)

— Reserved
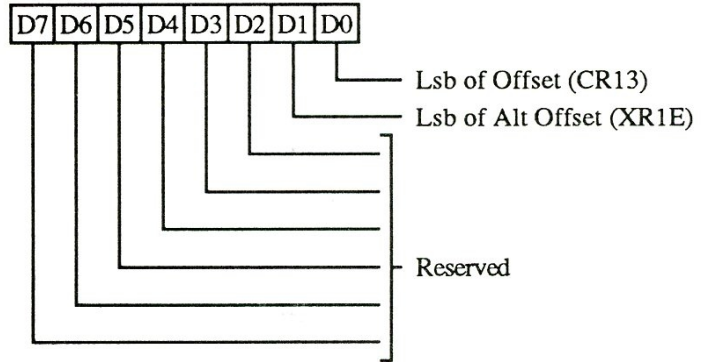
0 This bit provides finer granularity to the Offset when the word and double word modes are used. This bit is used with the regular Offset register (CR13).

1 This bit provides finer granularity to the Offset when the word and double word modes are used. This bit is used with the alternate Offset register (XR1E).

7-2 Reserved (0)

EMULATION MODE REGISTER (XR14)
Read/Write at I/O Address 3B7h/3D7h
Index 14h

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Emulation Mode
- Herc Config (read only)
- DE Status Mode
- V Retrace Status Mode
- Vsync Status Mode
- Interrupt Polarity
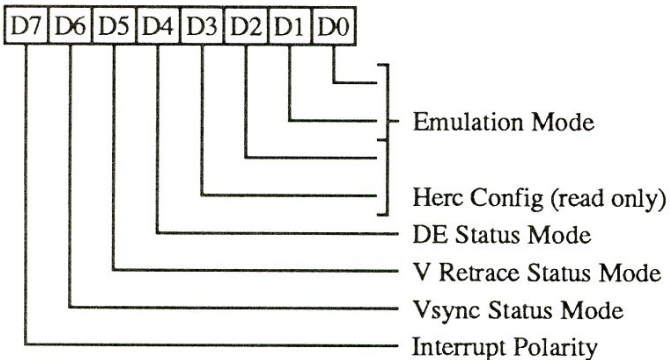
1-0 Emulation Mode

    00 = VGA/EGA
    01 = CGA
    10 = MDA
    11 = Hercules

3-2 Hercules Configuration Register (3BFh) readback (read only).

4 Display Enable Status Mode

    0: Select <u>Display Enable</u> status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes)

    1: Select <u>Hsync</u> status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes).

5 Vertical Retrace Status Mode

    0: Select <u>Vertical Retrace status</u> to appear at bit 3 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes)

    1: Select <u>Video</u> to appear at bit 3 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes).

6 Vsync Status Mode

    0: Enable Vsync status to appear at bit 7 of Input Status register 1 (I/O Address 3xAh in MDA and Hercules modes)

    1: Prevent Vsync status from appearing at bit 7 of Input Status register 1 (I/O Address 3xAh in CGA and VGA modes).

7 Interrupt Output Function

This bit controls the function of the IRQ/ output in both MCA-bus and PC-bus.

| | XR14D7 | XR14D7=0 | |
Interrupt State	PC Bus	MCA Bus	XR14D=1
Disabled	3-state	3-state	3-state
Enabled, Inactive	3-state	3-state	Low
Enabled, Active	3-state	Low	High

WRITE PROTECT REGISTER (XR15)
Read/Write at I/O Address 3B7h/3D7h
Index 15h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

Wr Protect Group 1 regs
Wr Protect Group 2 regs
Wr Protect Group 3 regs
Wr Protect Group 4 regs
Wr Protect Group 5 regs
Wr Protect Group 6 regs
Wr Protect Group 0 regs
Reserved
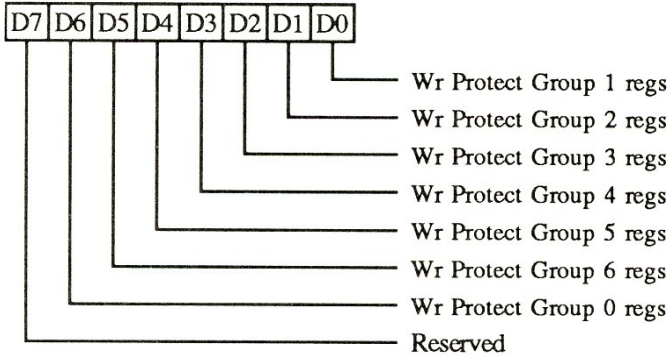
This register controls write protection for various groups of registers as shown. 0 = unprotected, 1= protected.

0   Write Protect Group 1 Registers

 Sequencer (SR00-SR04)
 Graphics Controller (GR00-GR08)
 Attribute Controller (AR00-AR14)

1   Write Protect Group 2 Registers

 Cursor Size register (CR09) bits 0-4
 Character Height regs (CR0A, CR0B)

2   Write Protect Group 3 Registers

 CRT Controller CR07 bit-4
 CRT Controller CR08
 CRT Controller CR11 bits 4 and 5
 CRT Controller CR13 and CR14
 CRT Controller CR17 bits 0,1 & 3-7
 CRT Controller CR18

 (Split screen, smooth scroll, & CRTC Mode)

3   Write Protect Group 4 Registers

 CRT Controller CR09 bits 5-7
 CRT Controller CR10
 CRT Controller CR11 bits 0-3 & 6-7
 CRT Controller CR12, CR15, CR16
 CRT Controller CR17 bit-2

4   Write Protect Group 5 Registers

 Miscellaneous Output (3C2h)
 Feature Control (3BA/3DAh)

5   Write Protect Group 6 Registers. (I/O Addresses 3C6-3C9h). The PALRD/ and PALWR/ output signals are disabled and the 82C455 DAC state register is write protected.

6   Write Protect Group 0 Registers. Auxiliary Write Protect for CRT Controller registers CR00-CR07 except CR07D4. This bit is logically ORed with CR11D7.

7   Reserved (0)

TRAP ENABLE REGISTER (XR16)
Read/Write at I/O Address 3B7h/3D7h
Index 16h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│   Trap on access to:
└──┴──┴──┴──┴──┴──┴──┴──┘   ── 3B4/3B5h
                           ──── 3B8/3BFh
                           ────── 3Cxh
                           ──────── 3D4/3D5h
                           ────────── 3D8/3D9h
                           ──────────── CR00-0B and CR10-18
                           ┐
                           ├ Reserved
                           ┘
```
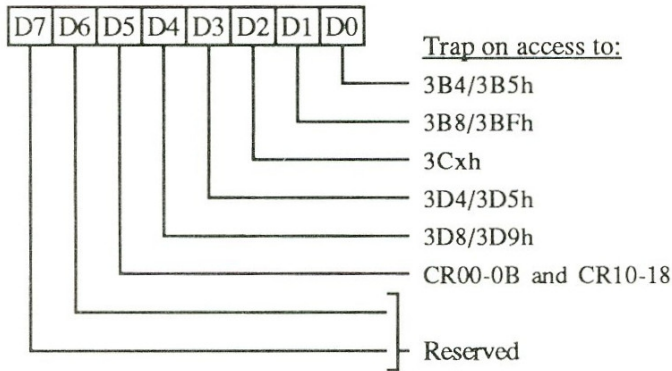
Trap Enable bits:

0	Generate Trap on Access to I/O Addresses 3B4h or 3B5h.
1	Generate Trap on Access to I/O Addresses 3B8h or 3BFh.
2	Generate Trap on Access to I/O Addresses 3Cxh.
3	Generate Trap on Access to I/O Addresses 3D4h or 3D5h.
4	Generate Trap on Access to I/O Addresses 3D8h or 3D9h.
5	Generate Trap on Access to registers CR00 through CR0B and CR10 through CR18.
6-7	Reserved (0)

For all bits:

   0:   Disable trap
   1:   Enable trap

This register is cleared (0) on reset.

TRAP STATUS REGISTER (XR17)
Read/Clear at I/O Address 3B7h/3D7h
Index 17h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│   Trap occurred at:
└──┴──┴──┴──┴──┴──┴──┴──┘   ── 3B4/3B5h
                           ──── 3B8/3BFh
                           ────── 3Cxh
                           ──────── 3D4/3D5h
                           ────────── 3D8/3D9h
                           ──────────── CR00-0B or CR10-18
                           ┐
                           ├ Reserved
                           ┘
```
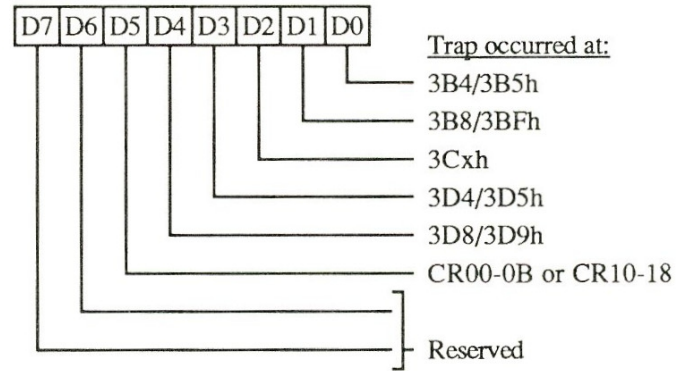
Trap Status bits:

0	Trap occurred on access to I/O Address 3B4h or 3B5h.
1	Trap occurred on access to I/O Address 3B8h or 3BFh.
2	Trap occurred on access to I/O Address 3Cxh.
3	Trap occurred on access to I/O Address 3D4h or 3D5h.
4	Trap occurred on access to I/O Address 3D8h or 3D9h.
5	Trap occurred on access to CRT Controller registers CR00 through CR0B and CR10 through CR18.
6-7	Reserved (0)

For all bits:

   0:   No access occurred
   1:   Access occurred

Any or all bits in this register may be cleared by writing a one (1) to the desired bit location.

**ALTERNATE HORIZONTAL
DISPLAY ENABLE END (XR18)**
Read/Write at I/O Address 3B7h/3D7h
Index 18h
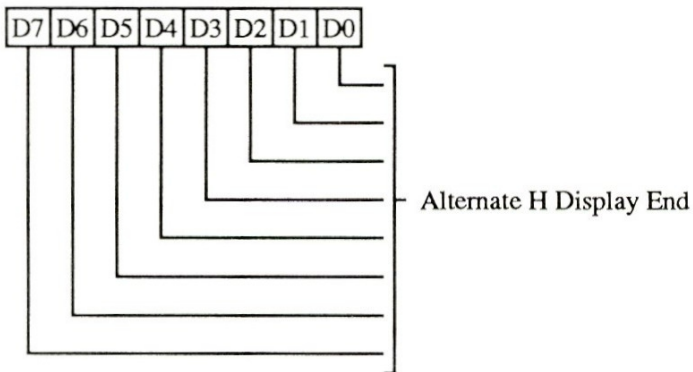
```
D7 D6 D5 D4 D3 D2 D1 D0
```
— Alternate H Display End

This register is used in CRT low resolution CGA modes, Hercules graphics and all flat panel modes.

7-0　Alternate Horizontal Display Enable End. See CR01 for description.

**ALTERNATE HORIZONTAL
SYNC START (XR19)**
Read/Write at I/O Address 3B7h/3D7h
Index 19h

```
D7 D6 D5 D4 D3 D2 D1 D0
```
— Alternate Hsync Start

This register is used in CRT low resolution CGA modes, Hercules graphics and all flat panel modes.

7-0　Alternate Horizontal Sync Start. See CR04 for description.

ALTERNATE HORIZONTAL SYNC END (XR1A)
Read/Write at I/O Address 3B7h/3D7h
Index 1Ah
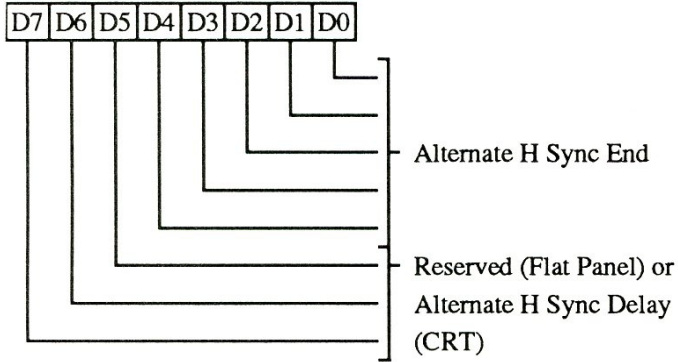
D7	D6	D5	D4	D3	D2	D1	D0

— Alternate H Sync End

— Reserved (Flat Panel) or
Alternate H Sync Delay
(CRT)

This register is used in CRT low resolution CGA modes, Hercules graphics and all flat panel modes.

4-0 Alternate Horizontal Sync End. See CR05 for description.

7-5 For CRT only: Alternate Horizontal Sync Delay. See CR05 for description.

For Flat Panel: Reserved (0).

ALTERNATE HORIZONTAL TOTAL (XR1B)
Read/Write at I/O Address 3B7h/3D7h
Index 1Bh
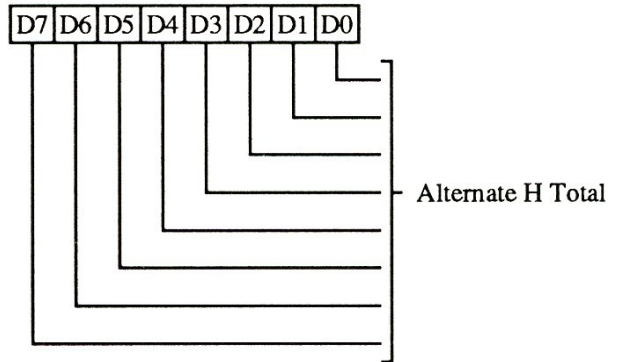
D7	D6	D5	D4	D3	D2	D1	D0

— Alternate H Total

This register is used in CRT low resolution CGA modes, Hercules graphics and all flat panel modes.

7-0 Alternate Horizontal Total. See CR00 for description.

ALTERNATE HORIZONTAL BLANK START (XR1C) [CRT]
Read/Write at I/O Address 3B7h/3D7h
Index 1Ch

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
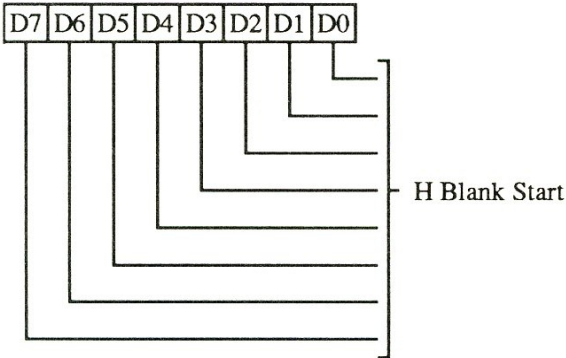
H Blank Start

This register is used in CRT low resolution CGA modes and Hercules graphics modes.

7-0   Alternate Horizontal Blank Start. See CR02 for description.

ALTERNATE HORIZONTAL BLANK END (XR1C) [Flat Panel]
Read/Write at I/O Address 3B7h/3D7h
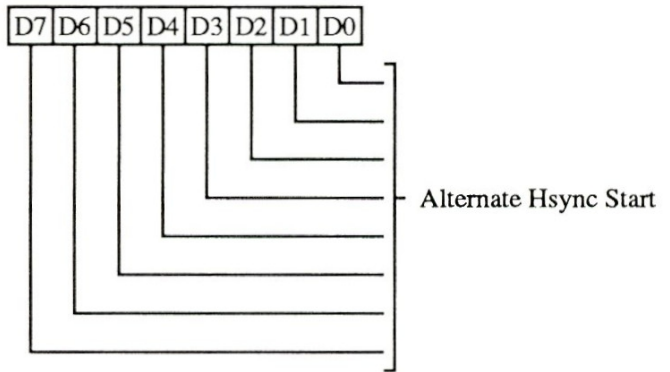*Index 1Ch*

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
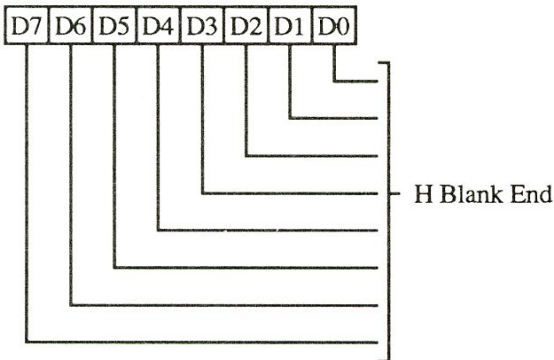
H Blank End

This register is used in all flat panel modes.

7-0   These bits specify the end of horizontal blank in terms of character clocks. The period between Vertical Blank End and the Horizontal Total is the left side border on screen.

ALTERNATE HORIZONTAL BLANK END (XR1D) [CRT]
Read/Write at I/O Address 3B7h/3D7h
Index 1Dh

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

H Blank End

DE Skew Control

Reserved

This register is used in CRT low resolution CGA modes and Hercules graphics modes.

4-0   Alternate Horizontal Blank End. See CR03 for description.

6-5   Display Enable Skew Control. See CR03 for description.

7   Reserved (0)

ALTERNATE HORIZONTAL BLANK START (XR1D) [Flat Panel]
Read/Write at I/O Address 3B7h/3D7h
Index 1Dh
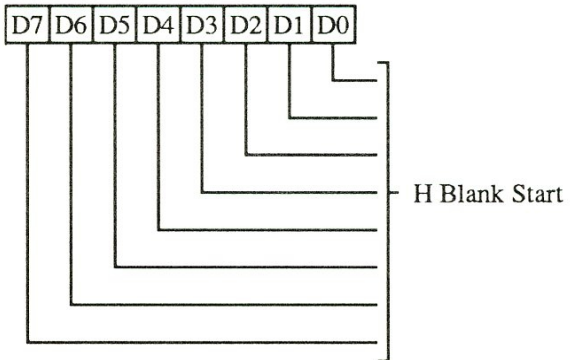
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

H Blank Start

This register is used in all flat panel modes.

7-0   Alternate Horizontal Blank Start. See CR02 for description.

Note: The function of XR1C and XR1D change from CRT to Flat Panel modes. A separate description is provided for each mode.

ALTERNATE OFFSET (XR1E)
Read/Write at I/O Address 3B7h/3D7h
Index 1Eh

```
D7  D6  D5  D4  D3  D2  D1  D0
                             └───┐
                                 │ Alternate
                             ─── │ Display Buffer
                                 │ Width
```
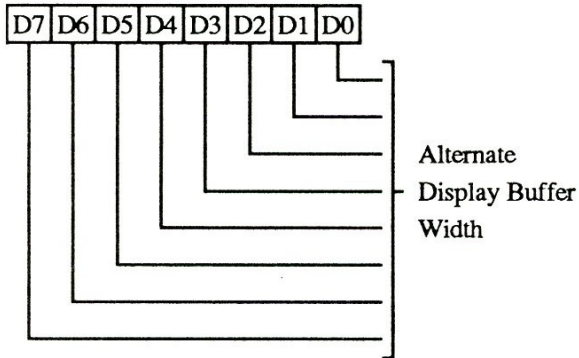
This register is used in low resolution CGA modes and Hercules graphics modes on both CRTs and Flat Panels.

7-0　Alternate Offset. See CR13 for description.

1　Blank / Display Enable Select

0: BLANK/ pin outputs BLANK/
1: BLANK/ pin outputs DE

The signal polarity selected by bit 0 is applicable for either selection.

Note: The BLANK/ pin should not be used to drive flat panels. The WGTCLK pin may be programmed (XR50D7 = 0) to provide the DE signal.

2　Shut off Video

0: Video not forced to default video (XR2B) during the blanking interval.
1: Video forced to default video (XR2B) during the blanking interval.

3　Shut Off Blank

0: The BLANK/ output is not forced to be active when the screen is blanked (using bit 5 of the Sequencer Clocking Mode register SR01)
1: The BLANK/ output is forced active when the screen is blanked (Bit 5 of SR01).

7-4　Reserved (0)

VIDEO INTERFACE REGISTER (XR28)
Read/Write at I/O Address 3B7h/3D7h
Index 28h

```
D7  D6  D5  D4  D3  D2  D1  D0
                             └── Blank/DE Polarity
                         ─────── Blank/DE Output Select
                     ─────────── Shut Off Video
                 ─────────────── Shut Off Blank

         ─────────────────────── Reserved
```
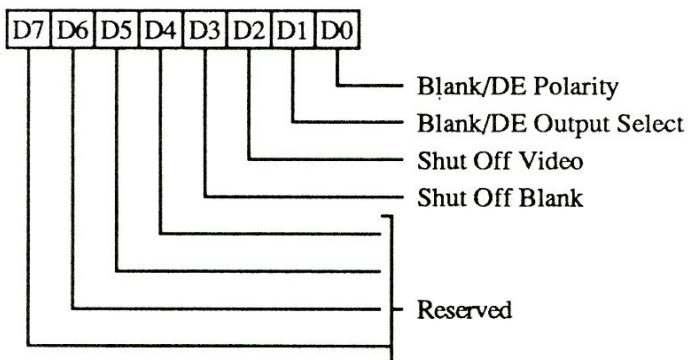
0　BLANK/Display Enable Polarity

0: Negative
1: Positive

DEFAULT VIDEO REGISTER (XR2B)
Read/Write at I/O Address 3B7h/3D7h
Index 2Bh

```
D7  D6  D5  D4  D3  D2  D1  D0
                             ─┐
                              │ Color displayed when
                              │ screen is blanked
```
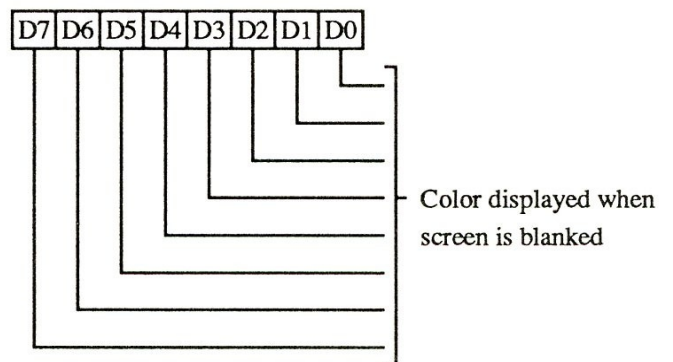
7-0　This register is effective only on CRT displays. These bits specify the palette value to be displayed during blank time.

PANEL FORMAT REGISTER (XR50)
Read/Write at I/O Address 3B7h/3D7h
Index 50h

```
D7 D6 D5 D4 D3 D2 D1 D0
```
Frame Rate Control

Pulse Width Modulation

Clock Divider

Reserved
Shift Clock Mask
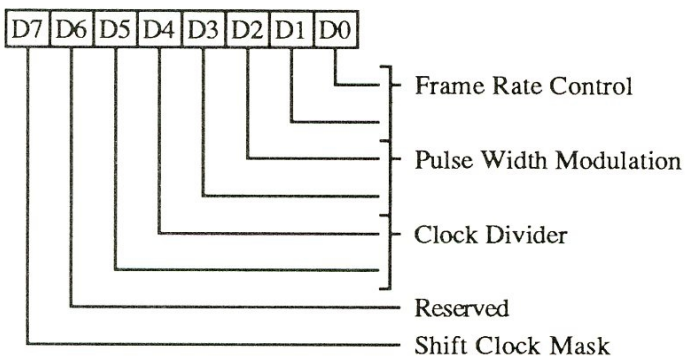
This register is effective only in flat panel mode as defined in bits 2-3 of XR51.

1-0 Frame Rate Control (FRC). These bits specify the gray levels simulated by the 82C455 on a frame by frame basis. This technique is used on flat panels that do not support gray levels internally, such as LCD panels.

00: No gray levels simulated for monochrome, 8 colors for color displays.

01: 4 levels simulated for color panels only. (64 colors are displayed.)

10: 16 gray levels simulated for monochrome panels only.

11: Reserved.

3-2 Pulse Width Modulation (PWM). This technique is used on flat panels that support internal gray levels such as most plasma panels.

00: No gray levels.

01: 4 levels of colors supported by the panel. Effective only with color panels. (64 colors are displayed.)

10: 16 levels of gray levels supported by the panel. Effective with monochrome panels only.

11: 256 levels of color supported by the panel. Effective only with color panels. Not supported for dual drive panels.

5-4 Clock Divide (CD). These bits specify the frequency ratio between the dot clock (CLK0, CLK1, CLK2) and the SHFCLK signal.

00: Shift clock frequency = dot clock frequency. This setting is used to output one pixel per clock with flat panel displays.

01: Shift clock frequency = dot clock frequency/2. This setting is used to output two pixels per clock with flat panel displays.

10: Shift clock frequency = dot clock frequency/4 This setting is used to output four pixels per clock with flat panel displays.

11: Shift clock frequency = dot clock frequency/8. This setting is used to output eight pixels per clock with flat panel displays.

6 Reserved (0)

7 Shift Clock Mask (SM). 0: Enable the SHIFT CLOCK to toggle outside the Display Enable interval. The Display Enable Signal (DE) is output on the WGTCLK output pin. 1: Cause the Shift Clock to stop (low) outside the Display Enable interval. The weighting clock is on the WGTCLK output pin.

DISPLAY TYPE REGISTER (XR51)
Read/Write at I/O Address 3B7h/3D7h
Index 51h

```
D7 D6 D5 D4 D3 D2 D1 D0
```
- Panel Drive
- Panel Organization
- Type of Display Media
- Mono/Color Panel
- Compatibility Enable
- Text Video Polarity
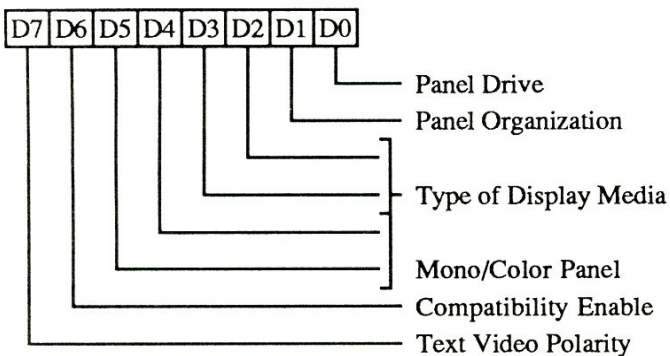
0   Type of Panel Drive. 0: Single Drive; 1: Double Drive. This mode is used only with Dual Panels. This bit must be set to 0 for single panels.

1   Type of Panel Organization

     0: Single Panel, 1: Dual Panel

3-2   Type of Display (CRT media is the default on reset.)

     00: LCD
     01: CRT
     10: Plasma, EL
     11: Reserved

5-4   Mono/Color Panel (MCP) Select.

     00: Color Panel, 3-bit data pack
     01: Color Panel, 4-bit data pack
     10: Monochrome panel
     11: Reserved

6   Compatibility Mode Enable (CMEN). When compatibility mode is enabled, the display is adjusted depending on the panel size, the current display mode and the contents of the compensation registers. When compatibility mode is disabled, the display is not adjusted. 0: Compatibility mode disabled. 1: Compatibility mode enabled.

7   Text Video Output Polarity. This bit sets the polarity of video data in text mode. This bit is effective only in flat panel text mode.

PANEL SIZE REGISTER (XR52)
Read/Write at I/O Address 3B7h/3D7h
Index 52h

```
D7 D6 D5 D4 D3 D2 D1 D0
```
- H Size
- Reserved
- V Size
- Reserved
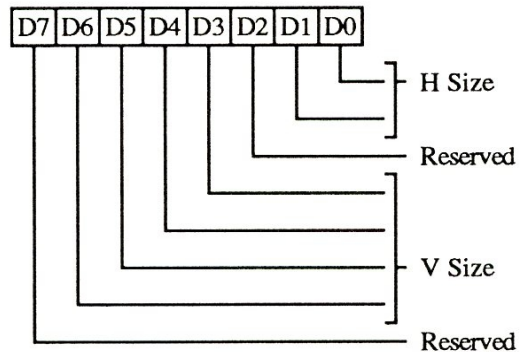
This register is effective in Flat Panel Mode only.

1-0   Horizontal Size Select

     00: Reserved
     01: 640 pixels
     10: 720 pixels
     11: Reserved

2   Reserved (0)

6-3   Vertical Size Select

     0000: Reserved
     0001: **200 lines**
     0010: **350 lines**
     0011: Reserved
     0100: **400 lines**
     0101: Reserved
     0110: Reserved
     0111: Reserved
     1000: **480 lines**
     1001: Reserved
     1010: Reserved
     1011: Reserved
     1100: Reserved
     1101: Reserved
     1110: Reserved
     1111: Reserved

7   Reserved (0)

OVERRIDE REGISTER (XR53)
Read/Write at I/O Address 3B7h/3D7h
Index 53h

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

— Disable AR10 D2
— Alt. Line Graphics Char.

— Reserved
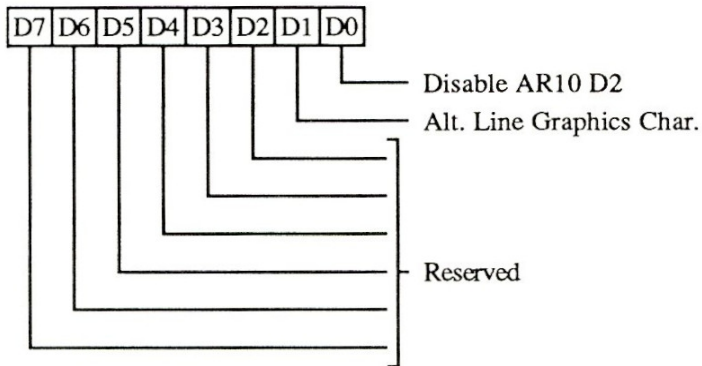
This register is used in both CRT and flat panel mode.

0   Disable AR10D2. This bit determines if the Line Graphics Character Code Enable is defined in the Attribute Controller by bit 1 of this register. This bit is also used to force 8 or 9 pixel fonts. 0: Use AR10D2 for Line Graphics control; 1: Use bit 1 of this register for Line Graphics control.

1   Alternate Line Graphics Character Code Control. If bit 0 of this register is 1, then this bit determines if the Line Graphics Character Codes are enabled. 0: Ninth pixel of Line Graphics Character Codes is set to the background color; 1: Ninth pixel of Line Graphics Character Codes is identical to the eighth pixel.

7-2   Reserved (0)

ALTERNATE MISCELLANEOUS OUTPUT REGISTER (XR54)
Read/Write at I/O Address 3B7h/3D7h
Index 54h

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

— Video Skew
— Reserved (0)
— Clock Select 1, 0

— Reserved

— HSYNC Polarity
— VSYNC Polarity
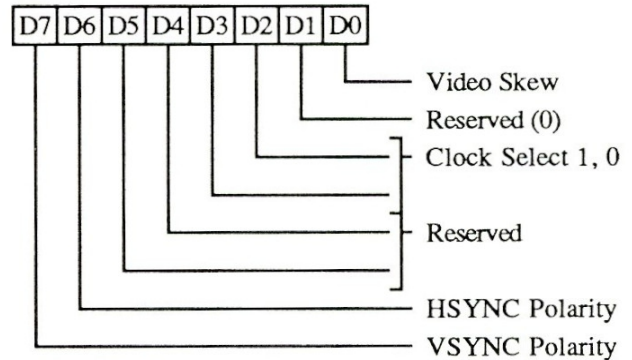
This register is used in Flat Panel modes.

0   Panel Video Skew

   0: No Panel Video data delay
   1: Video data delayed 1 clock cycle

1   Reserved (0)

3-2   Clock Select Bits. These bits select the flat panel dot clock source as follows:

   00: Select CLK0
   01: Select CLK1
   10: Select CLK2
   11: Reserved

5-4   Reserved (0)

6   Hsync Polarity (0 = pos, 1 = neg)
7   Vsync Polarity (0 = pos, 1 = neg)

(The polarity of the Blank pin is controlled through the Video Interface Register.)

TEXT MODE 350_A
COMPENSATION REGISTER (XR55)
Read/Write at I/O Address 3B7h/3D7h
Index 55h
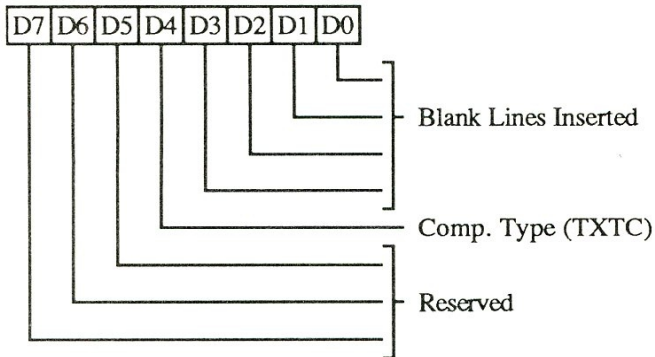
```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                    └─ Blank Lines Inserted

              └─ Comp. Type (TXTC)

        └─ Reserved
```

This register is used in Flat Panel Text Modes when the vertical registers are configured for a 350 line display and CR09D3 = 1.

3-0 Inserted Blank Lines (TCOMP). These bits specify the number of blank lines + 1 to insert after each row. The line inserted is set to the border color. This field is effective only when bit 4 of this register is 0.

4 Compensation Type (TXTC). 0: Insert blank lines after each row. Graphics compensation, if enabled, is turned off; 1: Do not insert blank lines. Graphics compensation, if enabled, is used.

7-5 Reserved (0)

TEXT MODE 350_B
COMPENSATION REGISTER (XR56)
Read/Write at I/O Address 3B7h/3D7h
Index 56h
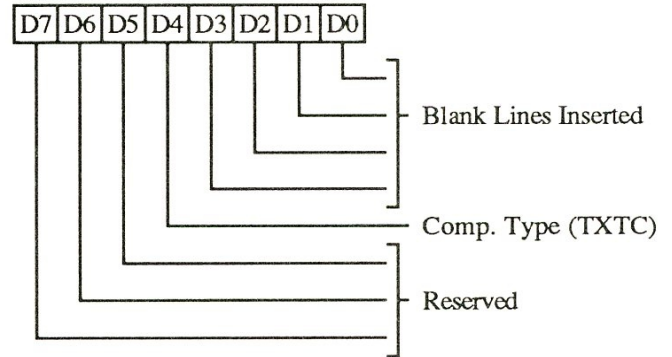
```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                    └─ Blank Lines Inserted

              └─ Comp. Type (TXTC)

        └─ Reserved
```

This register is used in Flat Panel Text Modes when the vertical registers are configured for a 350 line display and CR09D3 = 0 (8 line or smaller font).

3-0 Inserted Blank Lines (TCOMP). These bits specify the number of blank lines + 1 to insert after each row. The line inserted is set to the border color. This field is effective only when bit 4 of this register is 0.

4 Compensation Type (TXTC). 0: Insert blank lines after each row. Graphics compensation, if enabled, is turned off; 1: Do not insert blank lines. Graphics compensation, if enabled, is used

7-5 Reserved (0)

TEXT MODE 400
COMPENSATION REGISTER (XR57)
Read/Write at I/O Address 3B7h/3D7h
Index 57h

```
 D7  D6  D5  D4  D3  D2  D1  D0
```
— Blank Lines Inserted

— Comp. Type (TXTC)

— Reserved
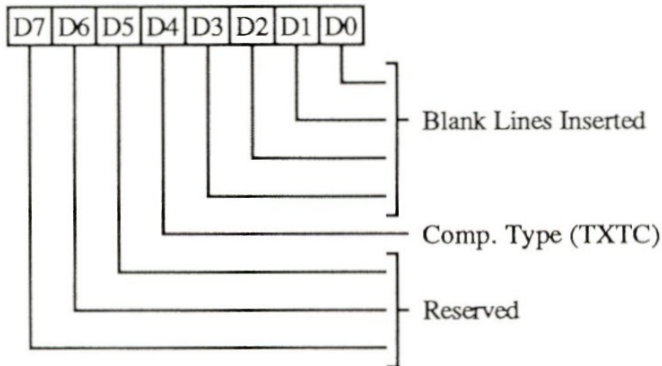
This register is used in Flat Panel Text Mode when the vertical registers are configured for 200 or 400 line displays.

3-0 Inserted Blank Lines (TCOMP). These bits specify the number of blank lines + 1 to insert after each row. The line inserted is set to the border color. This field is effective only when bit 4 of this register is 0.

4 Compensation Type (TXTC). 0: Insert blank lines after each row. Graphics compensation, if enabled, is turned off; 1: Do not insert blank lines. Graphics compensation, if enabled, is used.

7-5 Reserved (0)

GRAPHICS MODE 350
COMPENSATION REGISTER (XR58)
Read/Write at I/O Address 3B7h/3D7h
Index 58h

```
 D7  D6  D5  D4  D3  D2  D1  D0
```
— Comp. Line (COMPL)

— V Stretch Enable (STR)
— V Delete Enable (DEL)
— Comp. Incr. (COM+)
— Reserved
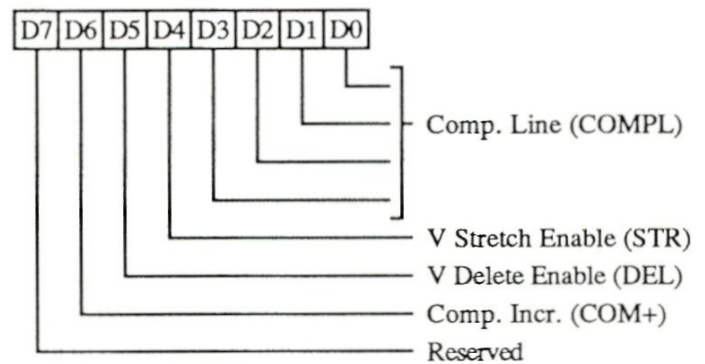
This register is used in Flat Panel 350 line modes. This feature is used for text modes when text compensation is disabled and in graphics modes.

3-0 Compensation Line (COMPL). These bits specify the number of displayed scan lines after which a scan line is replicated or skipped. When double scanning is enabled, one absolute scan line is actually two display scan lines.

4 Vertical Stretch Enable (STR). 0: No scan line is replicated. 1: A scan line is periodically replicated as specified by bits 0-3.

5 Vertical Delete Enable (DEL). 0: No scan line is deleted; 1: A scan line is periodically deleted (skipped) as specified by bits 0-3. These bits are effective only when double scanning is enabled. This ensures that there is no loss of information because only the second scan line is deleted.

6 Compensation Increment (COM+). 0: The COMPL field (bits 0-3) is used as programmed; 1: Increment the COMPL field every other period.

7 Reserved (0)

GRAPHICS MODE 400
COMPENSATION REGISTER (XR59)
Read/Write at I/O Address 3B7h/3D7h
Index 59h

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Comp. Line (COMPL)
- V Stretch Enable (STR)
- V Delete Enable (DEL)
- Comp. Incr. (COM+)
- Reserved
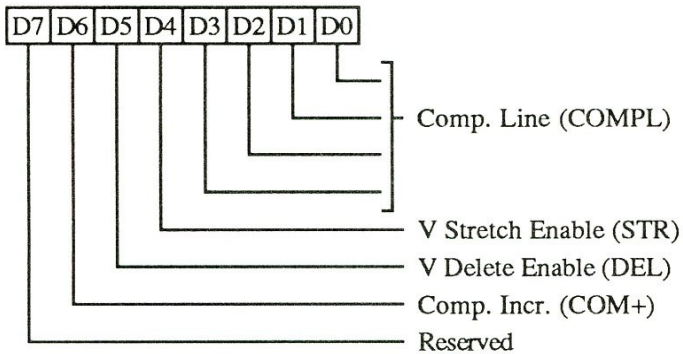
This register is used in Flat Panel 400 line modes. This register is also used for 200 line modes. This feature is used for text modes when text compensation is disabled and graphics modes.

3-0 Compensation Line (COMPL). These bits specify the number of displayed (not absolute) scan lines after which a scan line is replicated or skipped. When double scanning is enabled, one absolute scan line is actually two display scan lines.

4 Vertical Stretch Enable (STR).

    0: No scan line is replicated.
    1: A scan line is periodically replicated as specified by bits 0-3.

5 Vertical Delete Enable (DEL).

    0: No scan line is deleted.
    1: A scan line is periodically deleted (skipped) as specified by bits 0-3. These bits are effective only when double scanning is enabled. This ensures that there is no loss of information because only the second scan line is deleted.

6 Compensation Increment (COM+).

    0: The COMPL field (bits 0-3) is used as programmed.
    1: Increment the COMPL field every other period.

7 Reserved (0)

FLAT PANEL VERTICAL
DISPLAY START_400 (XR5A)
Read/Write at I/O Address 3B7h/3D7h
Index 5Ah
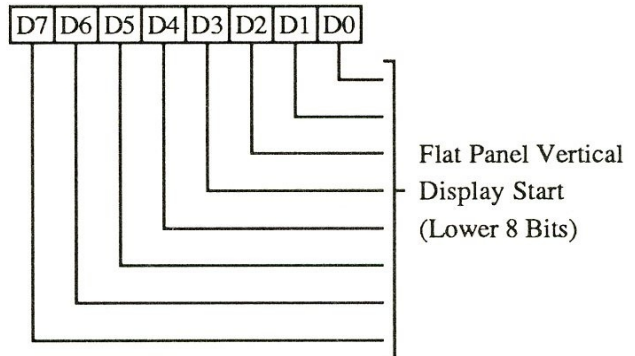
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

- Flat Panel Vertical Display Start (Lower 8 Bits)

7-0 These bits are used in 400-line flat panel modes. They specify the lower 8-bits of the vertical start address for Display Enable (in scan lines). The higher 2 bits are in the Flat Panel Vertical Overflow 2 register. To set the display start at the first scan line program this register with a value equal to the vertical total (XR64) + 1.

FLAT PANEL VERTICAL DISPLAY END_400 (XR5B)
Read/Write at I/O Address 3B7h/3D7h
Index 5Bh
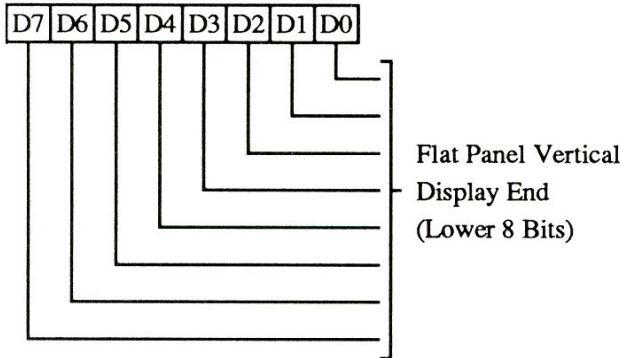
```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

Flat Panel Vertical
Display End
(Lower 8 Bits)

7-0 These bits are used in 400-line flat panel modes. They specify the lower 8-bits of the vertical end address for Display Enable (in scan lines). The high order 2 bits are in the Flat Panel Vertical Overflow 2 register. The correct value for this register is the start value + number of displayed lines (including inserted or replicated lines). Failure to correctly program this register will result in missing or extra line at the bottom of the display.

WEIGHT CLOCK CONTROL REGISTER A (XR5C)
Read/Write at I/O Address 3B7h/3D7h
Index 5Ch
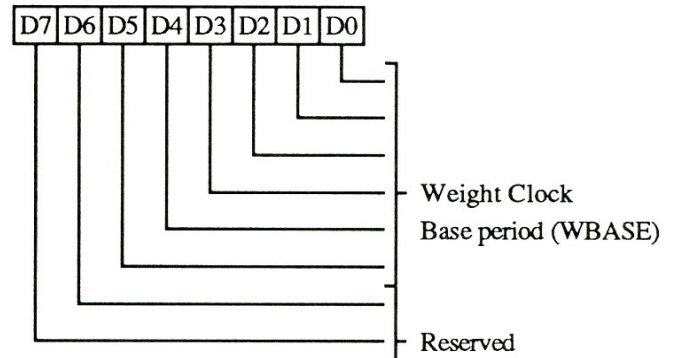
```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

Weight Clock
Base period (WBASE)

Reserved

This register is used in Flat Panel Mode when Bits 3 and 2 in the Panel Format register (XR50) are 01 or 10 and clock masking is Enabled (XR50D7 = 1). This register, along with XR5D and XR6C, controls the timing of the WGTCLK signal. This signal is used for grayscale panels requiring a weighting clock.

5-0 Base period for WGTCLK (WBASE). These bits define the number of units between the signal HSYNC and the first pulse on the WGTCLK output. A unit is 4 dot clocks per count programmed in this register. This defines a reference for the lowest grayscale level.

7-6 Reserved (0)

WEIGHT CLOCK
CONTROL REGISTER B (XR5D)
Read/Write at I/O Address 3B7h/3D7h
Index 5Dh
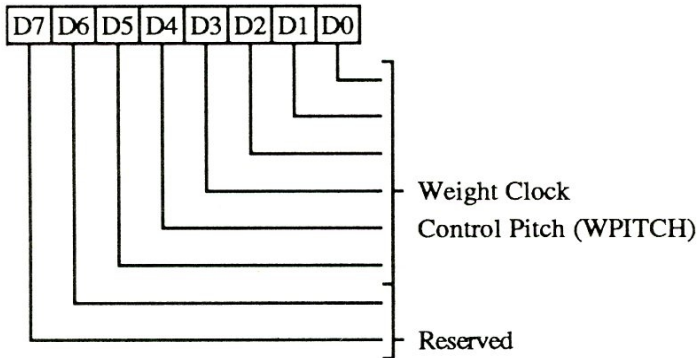
Weight Clock
Control Pitch (WPITCH)

Reserved

This register is used in Flat Panel Mode when Bits 3 and 2 in the Panel Format register (XR50) are 01 or 10 and clock masking is Enabled (XR50, D7 = 1). This register, along with XR5C and XR6C controls the timing of the WGTCLK signal. This signal is used for grayscale panels requiring a weighting clock.

5-0   Weight Clock Control Pitch (WPITCH). These bits define the number of units between subsequent pulses on the WGTCLK output. A unit is 4 dot clocks per count programmed fin this register. This defines the difference between two adjacent gray (or color) levels.

7-6   Reserved (0)

ACDCLK CONTROL REGISTER (XR5E)
Read/Write at I/O Address 3B7h/3D7h
Index 5Eh

ACDCLK Count

ACDCLK Control
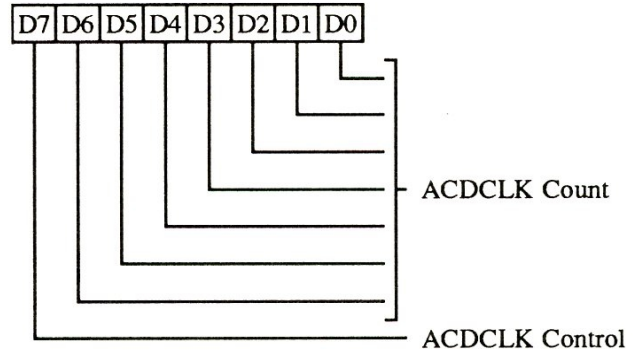
6-0   ACDCLK Count. These bits define the number of Hsyncs between adjacent phase changes on the ACDCLK output. This field is effective only when bit 7 of this register is 0. The number of Hsyncs between phase changes is equal to the value programmed in these bits plus two.

7   ACDCLK Control. 0: ACDCLK phase changes on value in bits 0-6. 1: ACDCLK phase inverts every frame.

POWER DOWN MODE
REFRESH REGISTER (XR5F)
Read/Write at I/O Address 3B7h/3D7h
Index 5Fh

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
Sleep Mode
Refresh Frequency
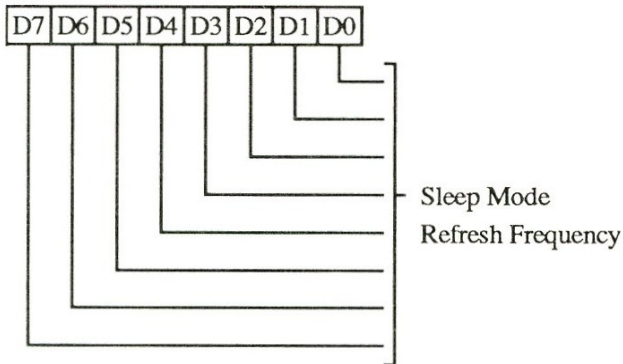
7-0 These bits define the frequency of RAS-only memory refresh cycles when PWRDN2 is high (82C455 disabled). The interval between two refresh cycles = Clock Period * [(4 * contents of this register) + 8]. A value of 0 causes no refresh to be done. The clock selected is specified by the Clock Select bits in the Miscellaneous Output register (3C2h).

BLINK RATE CONTROL (XR60)
Read/Write at I/O Address 3B7h/3D7h
Index 60h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
Blink Rate

Attribute Blink Duty Cycle
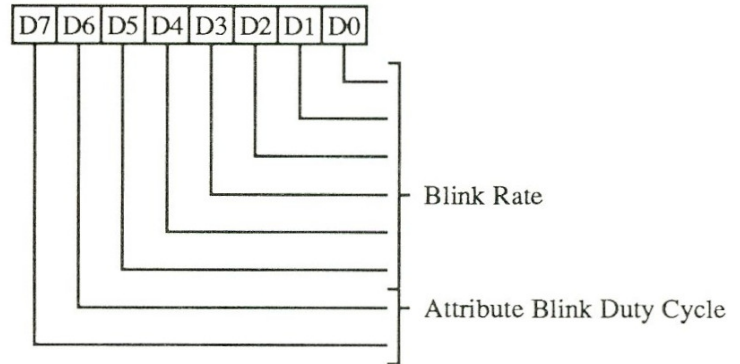
This register is used in all text modes. The graphics mode blink rate is fixed at 32 Vsyncs.

5-0 Blink Rate. These bits specify the number of VSYNC periods during which the cursor will be on and off (50% duty cycle). The character and pixel blink period will always be double the cursor blink period. The blink rate is selected as follows: Cursor Blink Frequency = VSYNC Frequency/[2 * contents of this register+1)].

7-6 Attribute Blink Duty Cycle. The cursor blink duty cycle is fixed at 50%. The character and pixel blink duty cycle is dependent on these bits as follows (default is 50% on reset):

Bit 7	Bit 6	Attribute Blink Duty Cycle
0	0	Reserved
0	1	25%
1	0	50%
1	1	75%

SMARTMAP™
CONTROL REGISTER (XR61)
Read/Write at I/O Address 3B7h/3D7h
Index 61h
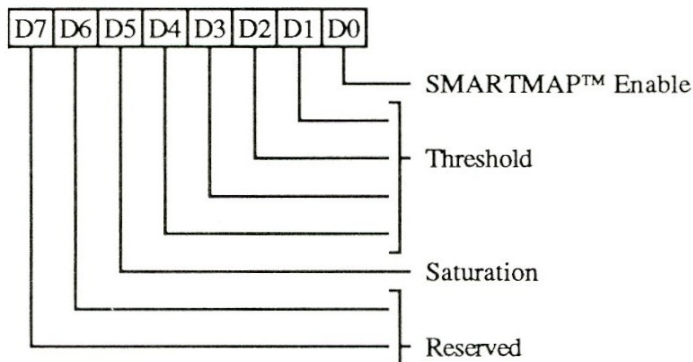
```
D7 D6 D5 D4 D3 D2 D1 D0
                     └──── SMARTMAP™ Enable

               └──────── Threshold

         └────────────── Saturation

   └──────────────────── Reserved
```

This register is used only in Flat Panel Text Mode when 16 gray levels are supported (Panel Format register fields FRC = 10 or PWM = 10).

0   SMARTMAP™ Enable.   0: Disable SMARTMAP and use color lookup table; 1: Enable SMARTMAP and bypass internal color lookup table.

4-1 SMARTMAP™ Threshold. These bits are used only when SMARTMAP is enabled in text mode. They define the minimum difference between the foreground and background colors. If the difference is less than this threshold, the colors are separated by adding and subtracting the shift values (XR62) to the foreground and background colors. However, if the foreground and background color values are the same, then the color values are not adjusted.

5   SMARTMAP™ Saturation. This bit is used only when SMARTMAP is enabled in text mode. It selects the clamping level after the color addition/subtraction. 0: The color result is clamped to the maximum and minimum values (0Fh and 00h respectively); 1: The result is computed modulo 16.

7-6 Reserved (0)

SMARTMAP™ SHIFT
PARAMETER REGISTER (XR62)
Read/Write at I/O Address 3B7h/3D7h
Index 62h
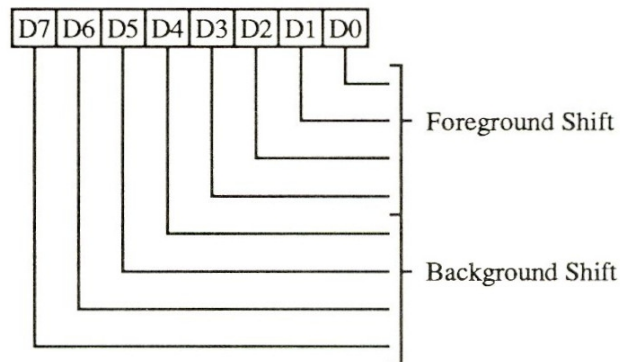
```
D7 D6 D5 D4 D3 D2 D1 D0
                     └──── Foreground Shift

         └────────────── Background Shift
```

This register is used only in Flat Panel Text Mode when 16 gray levels are supported (Panel Format register fields FRC = 10 or PWM = 10) and SMARTMAP™ is enabled.

3-0 Foreground Shift. These bits define the number of levels that the foreground color is shifted when the foreground and background colors are closer than the Shift Threshold. If the foreground color is "greater" than the background color, then this field is added to the foreground color. If the foreground color is "smaller" than the background color, then this field is subtracted from the foreground color.

7-4 Background Shift. These bits define the number of levels that the background color is shifted when the foreground and background colors are closer than the Shift Threshold. If the background color is "greater" than the foreground color, then this field is added to the background color. If the background color is "smaller" than the foreground color, then this field is subtracted from the background color.

GRAPHICS COLOR MAPPING CONTROL REGISTER (XR63)
Read/Write at I/O Address 3B7h/3D7h
Index 63h

D7	D6	D5	D4	D3	D2	D1	D0

- Color Threshold
- 256 Color Mapping
- Color Table Enable
- Color Table Protect
- Graphics Video Polarity
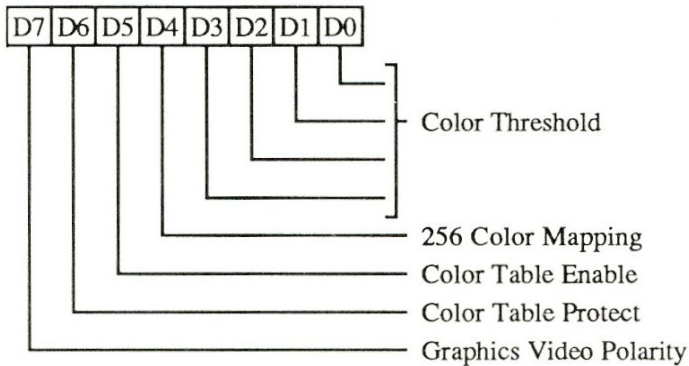
3-0 Color Threshold. These bits specify the threshold above which the color values are mapped to 1; color values less than the threshold are mapped to 0. This field is effective only in Flat Panel Graphics Mode when no gray levels are supported (Panel Format register fields FRC = 00 or PWM =00).

4 256 Color Mapping. 0: Specifies the use of the lower 4 bits of the 8 bits/pixel; 1: Specifies the use of the upper 4 bits of the 8 bits/pixel. This bit is effective only in the 256 color mode (bit 6 of AR10 = 1).

5 Color lookup table enable. This bit is effective in flat panel text modes with SMART-MAP™ disabled or graphics mode.

6 Color lookup table write protect. This bit is effective only if XR15D0 = 0. If XR15D0 = 1, then this bit is ignored. 0: Color lookup table (AR00-AR0F) not write protected; 1: Color lookup table write protected.

7 Graphics Video Output Polarity. This bit sets the polarity of video data in graphics mode. This bit is effective only in flat panel graphics mode.

ALTERNATE VERTICAL TOTAL (XR64)
Read/Write at I/O Address 3B7h/3D7h
Index 64h

D7	D6	D5	D4	D3	D2	D1	D0

- V Total
  (Scan Lines)
  (Lower 8 bits)
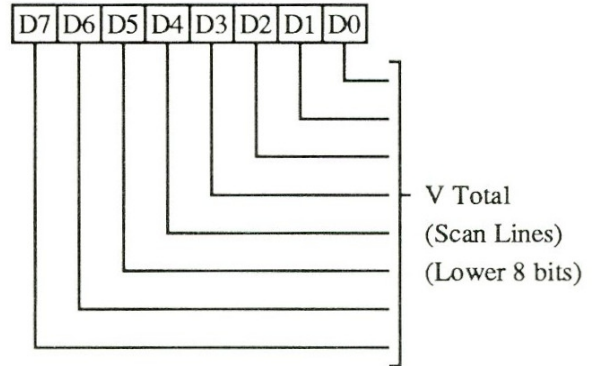
This register is used in flat panel modes.

7-0 Alternate Vertical Total. See CR06 for description.

ALTERNATE OVERFLOW (XR65)
Read/Write at I/O Address 3B7h/3D7h
Index 65h

D7	D6	D5	D4	D3	D2	D1	D0

- Alt V Total Bit 8
- Alt V Display End Bit 8
- Alt V Sync Start Bit 8
- Reserved (0)
- Alternate V Total Bit 9
- Alt V Display End Bit 9
- Alt V Sync Start Bit 9
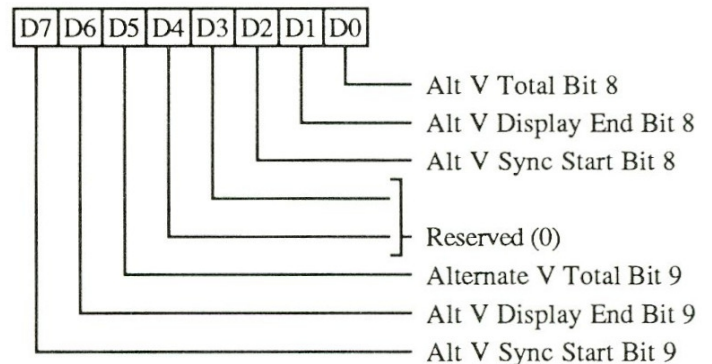
This register is used in flat panel modes.

0 Alternate Vertical Total Bit 8
1 Alternate Vertical Display End Bit 8
2 Alternate Vertical Sync Start Bit 8
3 Reserved (0)
4 Reserved (0)
5 Alternate Vertical Total Bit 9
6 Alternate Vertical Display End Bit 9
7 Alternate Vertical Sync Start Bit 9

**ALTERNATE
VERTICAL SYNC START (XR66)**
Read/Write at I/O Address 3B7h/3D7h
Index 66h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

— V Sync Start

(Lower 8 bits)
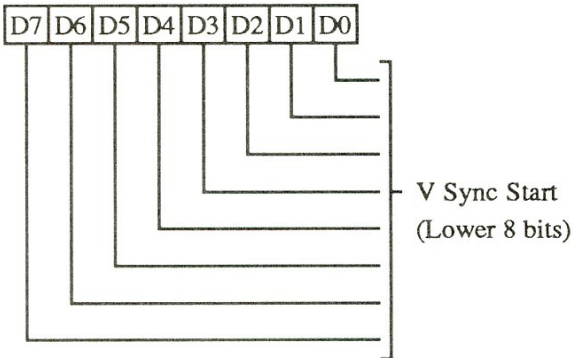
This register is used in flat panel modes.

7-0 Alternate Vsync Start. See CR10 for description.

**ALTERNATE
VERTICAL SYNC END (XR67)**
Read/Write at I/O Address 3B7h/3D7h
Index 67h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

— V End Sync
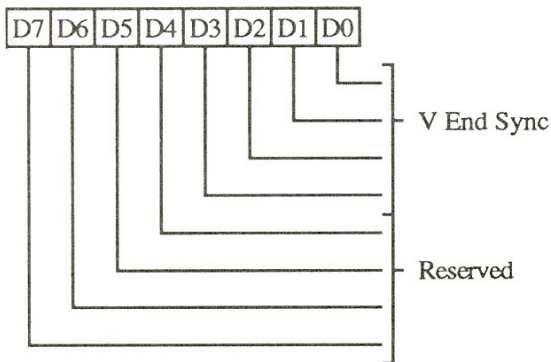
— Reserved

This register is used in flat panel modes.

3-0 Alternate Vsync End. See CR11 for description

7-4 Reserved (0)

**ALTERNATE
VERTICAL DISPLAY ENABLE (XR68)**
Read/Write at I/O Address 3B7h/3D7h
Index 68h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

— V display Enable End

(Lower 8 bits)

This register is used in flat panel modes. It is used to determine the size of the flat panel.

7-0 Alternate Vertical Display Enable End. See CR12 for description.

**FLAT PANEL
VERTICAL DISPLAY START_350 (XR69)**
Read/Write at I/O Address 3B7h/3D7h
Index 69h
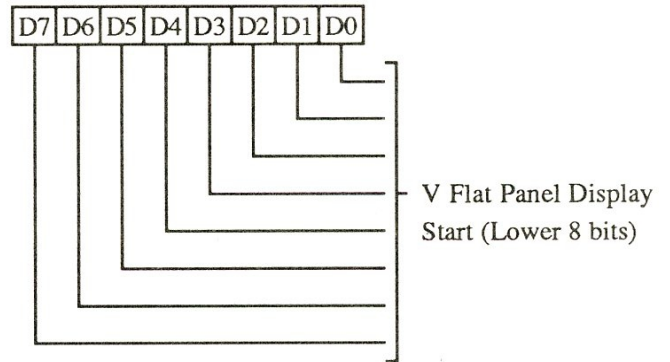
```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

— V Flat Panel Display

Start (Lower 8 bits)

7-0 These bits are used only in 350-line flat panel modes. They specify the lower 8-bits of the vertical start address for Display Enable (in scan lines). The high order 2 bits are in the Flat Panel Vertical Overflow 2 register. To set the display start at the first scan line program this register with a value equal to the vertical total (XR64) + 1.

FLAT PANEL
VERTICAL DISPLAY END_350 (XR6A)
Read/Write at I/O Address 3B7h/3D7h
Index 6Ah
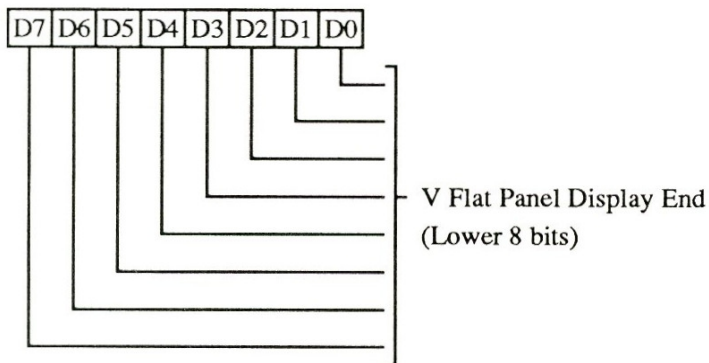
```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

V Flat Panel Display End
(Lower 8 bits)

7-0   These bits are used only in 350-line flat panel modes. They specify the lower 8-bits of the vertical end address for Display Enable (in scan lines). The high order 2 bits are in the Flat Panel Vertical Overflow 2 register. The correct value for this register is the start value + number of displayed lines (including inserted or replicated lines). Failure to correctly program this register will result in missing or extra lines at the bottom of the display.

FLAT PANEL
VERTICAL OVERFLOW 2 (XR6B)
Read/Write at I/O Address 3B7h/3D7h
Index 6Bh

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

V Display Start_350
Bits 9, 8
V Display Start_400
Bits 9, 8
V Display End _350
Bits 9, 8
V Display End_400
Bits 9. 8
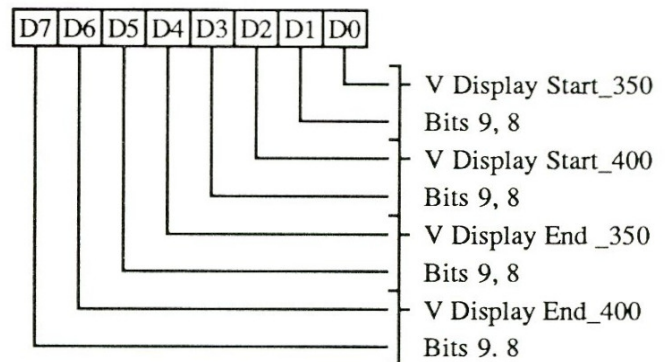
1-0   Bits 9-8 of Vertical Display Start_350
3-2   Bits 9-8 of Vertical Display Start_400
5-4   Bits 9-8 of Vertical Display End_350
7-6   Bits 9-8 of Vertical Display End_400

Bits 0-1 and 4-5 are used in 350-line Flat Panel modes only. Bits 2-3 and 6-7 are used in 400-line Flat Panel modes only.

WEIGHT CLOCK CONTROL REGISTER (XR6C)
Read/Write at I/O Address 3B7h/3D7h
Index 6Ch
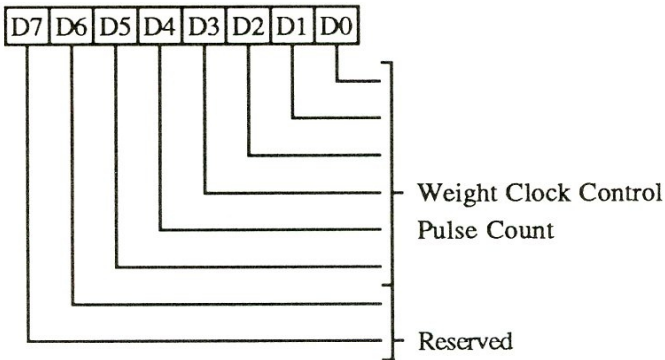
```
D7 D6 D5 D4 D3 D2 D1 D0
```
— Weight Clock Control
  Pulse Count

— Reserved

This register is used in Flat Panel Mode when Bits 3 and 2 in the Panel Format register (XR50) are 01 or 10 and clock masking is enabled (XR50D7 = 1). This register, along with XR5C and XR5D, controls the timing of the WGTCLK signal. This signal is used for grayscale panels requiring at weighting clock.

5-0 Weight Clock Control Pulse Count. These bits define the total number of pulses on the WGTCLK output.

7-6 Reserved (0)

CGA COLOR SELECT (XR7E)
Read/Write at I/O Address 3B7h/3D7h
Index 7Eh

```
D7 D6 D5 D4 D3 D2 D1 D0
```
— Color bit-0 (Blue)
— Color bit-1 (Green)
— Color bit-2 (Red)
— Color bit-3 (Intensity)
— Intensity Enable
— Color Set Select

— Reserved (0)
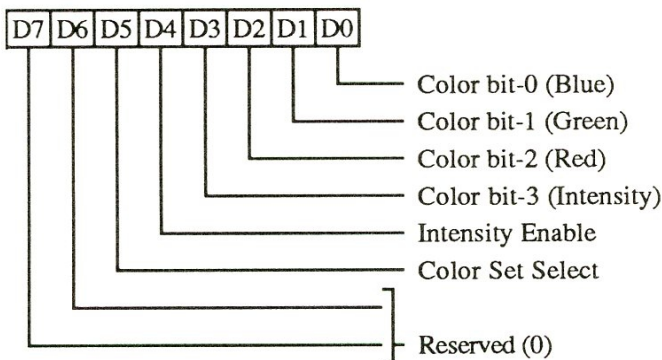
This register is a copy of the CGA color select register 3D9h. Writes to this register will change the copy at 3D9h. It is effective in CGA emulation mode. The copy at 3D9h is visible only in CGA emulation mode. The copy at XR7E is always visible.

DIAGNOSTIC (XR7F)
Read/Write at I/O Address 3B7h/3D7h
Index 7Fh

```
D7 D6 D5 D4 D3 D2 D1 D0
```
— 3-state Control
— Test Function

— Reserved (0)
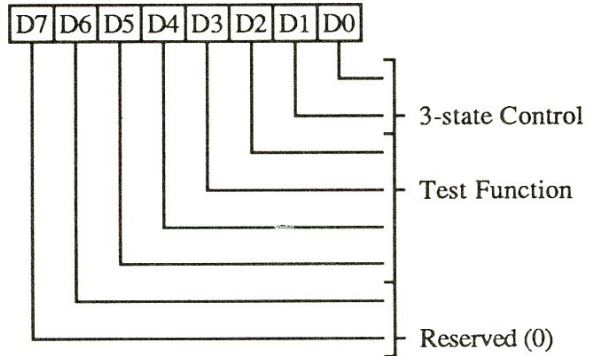
Diagnostic Register (I/O Address 3D7h; Address Pointer: 7Fh). Read - Write Register.

0 3-State Control bit 0.

   0: Normal Outputs.
   1: 3-state output pins PALRD, PALWR, WR46E8/, HSYNC, VSYNC, ACDCLK, WGTCLK, BLANK/, P[7:0], RDY, DATEN/ and IRQ/.

1 3-state Control bit 1.

   1: 3-state output pins WE, RAS, CAS0, CAS1, CAS2, CAS3, AA0-7 and BA0-7.

5-2 Test Function Pins. These bits are used for internal testing of the chip. They should be 0 for normal operation.

7-6 Reserved (0)

Programming and Parameters

82C455 REGISTER PROGRAMMING CONSIDERATIONS

The following pages provide extension register values for the 82C455. This information will allow the chip to be programmed for different flat panels and different compensation techniques.

Display Types:

VGA - Standard IBM VGA compatible Analog CRT.

LCD-DD - Dual Panel, Double Drive 640x480 Monochrome LCD Panel. These values will drive most LCD panels currently on the market.

LCD-DS - Dual Panel Single Drive 640x480 Monochrome LCD Panel. These panels are similar to LCD-DD, but only have one Data Bus (4 bits) for both upper and lower panels.

Plasma - 640x480 16 grayscale plasma or EL panels with a CRT type interface (1 Pixel/Clock).

General Programming Hints:

The values presented in this section make certain assumptions about the operating environment. The flat panel clock is assumed to be input on CLK2. If CLK0, or CLK1 is desired, bits D3 and D2 of XR54 should be changed accordingly. The values programmed into the SMARTMAP™ control registers (XR61 and XR62) give a threshold of 3 with foreground and background shift of 3 but SMARTMAP™ is turned off. To enable it, set XR61 D0 = 1. The value programmed in the ACDCLK Register (XR5E) will produce minimal ghosting on most LCD panels. However, this value should be optimized for each panel model. Certain LCD Panels (Epson in particular) require the ACDCLK to be synchronized to vertical sync. For this panel, XR5E should be programmed to 80h. The default value programmed in the refresh register (XR5F) will provide a refresh interval of 12 μ-second with a 25.175 MHz input clock when the 82C455 is disabled. This value is acceptable for standard DRAMs.

The vertical parameters assume a 480 Line Panel. If a 400 or 350 Line Panel is used, the vertical values should all be adjusted together. For single panels, the appropriate value (i.e. 80 or 130) should be subtracted from all vertical registers. For dual panel displays, the vertical timing values are for *each* panel. Therefore, the vertical values are one-half of the expected values. The adjustment value is one-half the change in resolution (i.e. 40 or 65). Vertical compensation should be disabled (pushed up configuration) or reduced. Both 400 line and 350 line values will need to be adjusted. To force the 82C455 to start the display on the first line, the flat panel display start (XR5A or XR69) should be equal to the vertical total (XR64) plus one.

The horizontal parameters assume a 640 pixel wide panel. The values presented here are the minimum required for each panel type. The horizontal values equal the number of characters clocks output per line. In dual drive panels this value includes both panels. Therefore, the horizontal values are double those expected.

For panels requiring longer sync times, these values may be increased. Due to pipelining of the horizontal counters, certain sync or blank values may result in no display. Generally, the horizontal blank start must equal the display end and the blank end must equal the horizontal total. The horizontal sync start and end values have a wide range of acceptable values.

For flat panel types and sizes not presented here, start with the parameters for a panel that most closely resembles the target panel. Adjust the flat panel configuration registers as needed and adjust the horizontal and vertical parameters as needed. Adaption to a non-standard panel is usually a trial and error process.

These parameters are recommended by Chips and Technologies for this part. They have been tested on several different flat panel displays. Customers should feel free to test other register values to improve the screen appearance or to customize the 82C455 for another flat panel display.

82C455 EXTENSION REGISTER VALUES

Register	CRT	LCD-DD	LCD-DS	PLASMA	Description
XR08	02	02	02	02	General Purpose Output Select B
XR09	02	00	00	00	General Purpose Output Select A
XR18	00	9F	4F	4F	Alt. Horizontal Display Enable End
XR19	00	A9	55	55	Alt. Horizontal Sync Start
XR1A	00	0D	19	19	Alt. Horizontal Sync End
XR1B	00	AD	59	59	Alt. Horizontal Total
XR1C	00	AD	59	59	Alt. Horizontal Blank End
XR1D	00	9F	4F	4F	Alt. Horizontal Blank Start
XR1E	00	28	28	28	Alt. Offset
XR50	00	B2	A2	08	Panel Format
XR51	04	63	62	E8	Display Type
XR52	00	41	41	41	Panel Size
XR53	00	00	00	00	Line Graphics Override
XR54	00	08	08	C8	Alt. Miscellaneous Output
XR55	10	10	10	10	Text Mode 350A Compensation
XR56	10	10	10	10	Text Mode 350B Compensation
XR57	10	10	10	10	Text Mode 400 Compensation
XR58	00	00	00	00	Graphics Mode 350 Compensation
XR59	00	00	00	00	Graphics Mode 400 Compensation
XR5A	00	27	27	27	Flat Panel Vertical Display Start 400
XR5B	00	B7	B7	B7	Flat Panel Vertical Display End 400
XR5C	00	03	03	03	Weight Clock Control A
XR5D	00	03	03	03	Weight Clock Control B
XR5E	00	05	05	00	ACDCLK Control
XR5F	00	4E	4E	4E	Power Down Mode Refresh
XR60	88	88	88	88	Blink Rate Control
XR61	00	06	06	06	SMARTMAP Control
XR62	00	33	33	33	SMARTMAP Shift Parameter
XR63	20	20	20	20	Graphics Color Mapping Control
XR64	00	F2	F2	F0	Alt. Vertical Total
XR65	00	00	00	07	Alt. Overflow
XR66	00	F1	F1	E0	Alt. Vertical Sync Start
XR67	00	02	02	01	Alt. Vertical Sync End
XR68	00	EF	EF	DF	Alt. Vertical Display Enable End
XR69	00	40	40	40	Flat Panel Vertical Display Start 350
XR6A	00	9E	9E	9E	Flat Panel Vertical Display End 350
XR6B	00	50	50	50	Flat Panel Overflow 2
XR6C	00	0F	0F	0F	Weight Clock Control C

Note:
CRT: Standard VGA Analog CRT display
LCD-DD: LCD Dual Panel Double Drive 640x480 Panel
LCD-DS: LCD Dual Panel Single Drive 640x480 Panel
PLASMA: Plasma 640x480 16-GRAY level panel

82C455 PARAMETERS - NO COMPENSATION

This configuration will position all text and graphics modes starting at the top of the panel.

The BIOS should program the extension registers as follows for all modes:

Register	Value	Description
XR55	10	Text Compensation 350A
XR56	10	Text Compensation 350B
XR57	10	Text Compensation 400
XR58	00	Graphics Compensation 350
XR59	00	Graphics Compensation 400
XR5A	00	Flat Panel Display Start 400
XR5B	90	Flat Panel Display End 400
XR69	00	Flat Panel Display Start 350
XR6A	5E	Flat Panel Display End 350
XR6B	50	Overflow 2

82C455 PARAMETERS - CENTERED CONFIGURATION

This configuration will center all text and graphics modes on a 480-line panel.

The BIOS should program the extension registers as follows for all modes:

Register	Value	Description
XR55	10	Text Compensation 350A
XR56	10	Text Compensation 350B
XR57	10	Text Compensation 400
XR58	00	Graphics Compensation 350
XR59	00	Graphics Compensation 400
XR5A	27	Flat Panel Display Start 400
XR5B	B7	Flat Panel Display End 400
XR69	40	Flat Panel Display Start 350
XR6A	9E	Flat Panel Display End 350
XR6B	50	Overflow 2

82C455 PARAMETERS - GRAPHICS COMPENSATION

This configuration will "stretch" all text and graphics modes on a 480-line panel using graphics compensation, and center the resulting display on the panel. This will stretch all text characters uniformly, so the same character at different positions on the screen will look the same.

The BIOS should program the extension registers as follows for all modes:

Register	Value	Description
XR55	10	Text Compensation 350A
XR56	10	Text Compensation 350B
XR57	10	Text Compensation 400
XR58	52	Graphics Compensation 350
XR59	17	Graphics Compensation 400
XR5A	0E	Flat Panel Display Start 400
XR5B	D0	Flat Panel Display End 400
XR69	0E	Flat Panel Display Start 350
XR6A	D0	Flat Panel Display End 350
XR6B	50	Overflow 2

82C455 PARAMETS - TEXT COMPENSATION

This configuration will extend text modes on a 480-line panel using text compensation to insert blank scan lines between text rows. It will "stretch" graphics modes using graphics compensation.

The BIOS should program the extension registers as follows for all modes:

Register	Value	Description
XR55	03	Text Compensation 350A
XR56	00	Text Compensation 350B
XR57	01	Text Compensation 400
XR58	52	Graphics Compensation 350
XR59	17	Graphics Compensation 400
XR5A	0E	Flat Panel Display Start 400
XR5B	D0	Flat Panel Display End 400
XR69	0E	Flat Panel Display Start 350
XR6A	D0	Flat Panel Display End 350
XR6B	50	Overflow 2

82C455 EXTENSION REGISTER VALUES FOR 400-LINE DUAL PANEL DOUBLE DRIVE LCD DISPLAY

Register	Value	Description
XR08	02	General Purpose Output Select B
XR09	00	General Purpose Output Select A
XR18	9F	Alt. Horizontal Display Enable End
XR19	A9	Alt. Horizontal Sync Start
XR1A	0D	Alt. Horizontal Sync End
XR1B	AD	Alt. Horizontal Total
XR1C	AD	Alt. Horizontal Blank End
XR1D	9F	Alt. Horizontal Blank Start
XR1E	28	Alt. Offset
XR50	B2	Panel Format
XR51	63	Display Type
XR52	**21**	Panel Size
XR53	00	Line Graphics Override
XR54	08	Alt. Miscellaneous Output
XR55	10	Text Mode 350A Compensation
XR56	10	Text Mode 350B Compensation
XR57	10	Text Mode 400 Compensation
XR58	00	Graphics Mode 350 Compensation
XR59	00	Graphics Mode 400 Compensation
XR5A	**CB**	Flat Panel Vertical Display Start 400
XR5B	**8F**	Flat Panel Vertical Display End 400
XR5C	03	Weight Clock Control A
XR5D	03	Weight Clock Control B
XR5E	0D	ACDCLK Control
XR5F	4E	Power Down Mode Refresh
XR60	88	Blink Rate Control
XR61	06	SMARTMAP Control
XR62	33	SMARTMAP Shift Parameter
XR63	20	Graphics Color Mapping Control
XR64	**CA**	Alt. Vertical Total
XR65	00	Alt. Overflow
XR66	**C9**	Alt. Vertical Sync Start
XR67	**0A**	Alt. Vertical Sync End
XR68	**C8**	Vertical Display Enable End
XR69	**11**	Flat Panel Vertical Display Start 350
XR6A	**6F**	Flat Panel Vertical Display End 350
XR6B	50	Flat Panel Overflow 2
XR6C	0F	Weight Clock Control C

Note: Registers which have a value that is different for 400 and 480 line panels are shown in **boldface**. All other registers are the same.

COMPATIBILITY

The 82C455 is compatible with the VGA, EGA, Hercules, CGA and MDA display standards. In general, application software written for one of these standards can be run on a 82C455 based system if a display with a resolution equal to or greater than that standard is used.

The 82C455 provides several features which aid in the implementation of a display system compatible with these standards. These features are as follows:

■   Write protection of internal registers using Write Protect (one of the Backward Compatibility registers). This ensures that writes to internal registers initiated by applications software do not corrupt register values, enabling a user to run software written for previous graphics standards.

■   Two sets of display parameter registers are supplied. The 82C455 automatically selects the set to be used based on the current display mode and the type of display in use. In flat panel modes, the alternate register set is always used.

Certain assumptions are made regarding the VGA and backward compatibility:

■   No NMI or any other interrupts have to be used. It is possible to generate NMI traps if required to support auto emulation.
■   On power up the chip is always in VGA mode.
■   There is no separate EGA mode. EGA mode is considered to be a special case of VGA mode. Special bits are provided to Write Protect some EGA specific registers. Software that uses the EGA in standard modes will work with the 82C455.
■   A software program can be executed to switch the chip into and out of CGA or Hercules modes. The software utility is consistent with the exact display being used. The BIOS for 82C455 available from Chips & Technologies includes software to program the 82C455 in the VGA, EGA, CGA, MDA and Hercules modes.

■   When in CGA or Hercules mode, all VGA/EGA registers are unavailable.
■   EGA, CGA, MDA and Hercules modes will function in the standard defined modes.

WRITE PROTECTING 82C455 REGISTERS

To use the write protect features:

A.   Initialize the CRT controller and alternate registers to generate sync signals for the display in use.

B.   Write protect the CRT controller registers using the Write Protect Register.

C.   Permit the application software to write CRT registers as if a particular display were in use. The 82C455 will operate as if a standard I/O write took place but will not permit protected registers to be altered.

TWO SETS OF DISPLAY PARAMETER REGISTERS

The 82C455 supplies two sets of Display Parameter Registers. The contents of the internal mode registers is interpreted automatically and either the CRTC or alternate registers is selected to generate the correct display. Since the display memory format in text and graphics is identical, switching between these modes does not require CPU or application software intervention. The registers and their use are summarized in the table below.

Write protect the CRTC registers using the Write Protect Register to prevent the application software from corrupting them.

DISPLAY PARAMETER REGISTERS USED FOR CRTS IN CGA AND HERCULES MODES

Note: The Alternate Registers are used for all Flat Panel Modes.

EMULATION	MODE	Horizontal Register Set	Vertical Register Set
CGA	Low-Res	Alternate	Regular
CGA	Hi-Res	Regular	Regular
Hercules	Text	Regular	Regular
Hercules	Graphics	Alternate	Regular

The BIOS supplied by Chips & Technologies can be used to initialize both sets of registers. To enable backward compatibility, the chip is programmed as follows:

A. Program the 82C455 exactly analogous to an IBM VGA. Disable the additional bits in the new registers.
B. Select VGA mode (default).

EGA MODE

A. Program the 82C455 exactly analogous to an IBM VGA. Disable the additional bits in the new registers.
B. Write protect Group 4 registers. Also, protect the external palette, clock select register, internal palette (if desired) and all CRT sync registers.
C. Force all 10th bits of vertical counters (including line compare) to 0.
D. Select the EGA type frame interrupt. This controlled with bit 7 of Emulation Mode Register.

CGA MODE

A. Program the regular CRT registers for the 640 pixels horizontal mode. The horizontal sync rate must be consistent with the monitor used. Program the Alternate Horizontal Register for 320 pixels horizontal mode.
B. The vertical resolution can be 200 or 400 lines. The vertical sync rate must be consistent with the monitor used.
C. Load the font in the memory.
D. Pre-program all registers in Sequencer, Attribute Controller and Graphics Controller as in Mode 2.
E. Set the sync polarity as required for 200 or 400 lines.
F. Enable Double Scanning (if required by the monitor).
G. Program CGA Mode Control Register (3D8h) and Color Palette Register (3D9h) as required. These registers are implemented in hardware.
H. Write Protect group 1, Group 3 and Group 4 registers.
I. Select CGA mode.

The 82C455 will automatically respond to 320/640 pixels/line and text/graphics mode as defined in the CGA Mode Control Register (3D8h). In 40 column CGA modes, the alternative CRTC registers are used.

MDA MODE

A.   Program the regular CRT registers in the 720 pixels horizontal mode with 9 pixels/character. The horizontal sync rate must be consistent with the monitor used.
B.   The vertical resolution must be 350 lines. The vertical sync rate must be consistent with the monitor used.
C.   Load the font in memory.
D.   Pre-program all registers in Sequencer, Attribute Controller and Graphics Controller as in Mode 7.
E.   Set the sync polarity as required for 350 lines.
F.   Write Protect Group 1, Group 3, and Group 4 registers.
G.   Select MDA mode.
H.   Hercules Control Registers do not work on this mode.

HERCULES MODE

A.   Program the regular CRT registers for 720 pixels horizontal mode with 9 dots/character. Program the alternate registers for 720 pixels with 8 dots/character. The clock divide parameter must be set to divide by 8 (not 9).
B.   The vertical resolution must be 350 lines. The vertical sync rate must be consistent with the monitor used. The vertical display end must be programmed to 350 Lines (Text Mode). In the Graphics Mode, 2 lines will automatically be subtracted. The Vertical Sync and Blank parameters must be programmed greater than 350 lines.
C.   Load the font in the memory.
D.   Pre-program all registers in Sequencer, Attribute Controller and Graphics Controller as in Mode 7. The 8/9 divide bit in the sequencer must be set to divide by 8.
E.   Set the sync polarity as required fir 350 lines.
F.   Program Display Mode Control Register (3B8h) and Hercules Configuration Register (3BFh) as required. These registers are implemented in hardware.
G.   Write Protect Group 1, Group 2 and Group 3 registers.
H.   Select Hercules mode.

The 82C455 will automatically respond to text, half graphics and full graphics modes as defined in the Mode Control Registers (3B8h and 3BFh). The regular CRT Offset Register is used in Hercules text mode. In Hercules graphics mode, the offset is defined in the Alternate Offset and Auxiliary Offset Registers. The Alternate Horizontal Registers are used in the Hercules Graphics mode.

When Emulation is enabled and the extension registers are disabled, bits 1 and 2 of the CRTC register addresses are ignored (Similar to CGA and Hercules). The CRTC Registers occupy addresses 3B0h - 3B7h (3D7h).

AUTO EMULATION TRAPS

The 82C455 also supports trap generation for auto emulation purposes. The traps can be enabled on various conditions as defined in the Trap Enable Register. Traps are generated for I/O Write cycles only.

LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter is saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space 10h and 11h. This allows simulating the Light Pen Hit technique to detect text/graphics modes on the CGA/Hercules cards.

A PRACTICAL IMPLEMENATION FOR BACKWARDS COMPATIBILITY:

The following procedure provides are practical way of implementing backwards compatibility on the 82C455. It assumes the display is an IBM VGA monitor or compatible or a flat panel. In order to use this implementation, the following VGA BIOS functions or equivalent code is required:

        Set Mode Function
                AH = 00h
                AL = Video Mode
        Set Scan Lines Function
                AH = 12h
                AL = Scan Line Code:
                        00 = 8 scan lines/character
                        01 = 14 scan lines/character
                        02 = 16 scan lines/character
                BL = 30h

VGA MODE

1. Set XR14 = 80h (00h for MCA bus).
2. Set XR15 = 00h.
3. Use Set Scan Lines Function to select 16 scan lines per character.
4. Use Set Mode Function to set a standard VGA text mode, such as 3+ or 7+.
5. Set XR02D4&3=00.

EGA MODE

1. Set XR14 = 80h (00h for MCA bus).
2. Set XR15 = 00h.
3. Use Set Scan Lines Function to select 14 scan lines per character.
4. Use Set Mode Function to set a standard EGA text mode, such as 3* or 7.
5. Set CR09D6=0.
6. Set XR15=18h.
7. Set XR02D4&3=10.

CGA MODE

1. Set the Equipment Installed byte at 40:10h D5=1 & D4=0 (color monitor).
2. Set XR14 = 80h (00h for MCA bus).
3. Set XR15 = 00h.
4. Use Set Scan Lines Function to select 8 scan lines per character.
5. Use Set Mode Function to set a standard CGA text mode, such as 3.
6. Set CR17=A2h, GR06=0Fh and AR10=01h.
7. Program extension registers XR0D, XR14, XR15, XR18, XR19, XR1A, XR1B, XR1C, XR1D and XR1E for the proper display type. (See following table.)
8. Set CGA Mode Control Register at 3D8h = 29h.
9. Set CGA Color Select Register at 3D9h=30h.

MDA MODE

1. Set the Equipment Installed byte at 40:10h D5=1 & D4=1 (monochrome monitor).
2. Set XR14 = 80h (00h for MCA bus).
3. Set XR15 = 00h.
4. Use Set Scan Lines Function to select 14 scan lines per character.
5. Use Set Mode Function to set MDA text mode 7.
6. Set AR08 = 00h.
7. Program extension registers XR0D, XR14, XR15, XR18, XR19, XR1A, XR1B, XR1C, XR1D and XR1E for the proper display type. (See following table.)
8. Set MDA Mode Control Register at 3B8h = 29h.

HERCULES MODE

1. Set the Equipment Installed byte at 40:10h D5=1 & D4=1 (monochrome monitor).
2. Set XR14 = 80h (00h for MCA bus).
3. Set XR15 = 00h.
4. Use Set Scan Lines Function to select 14 scan lines per character.
5. Use Set Mode Function to set MDA text mode 7.
6. Set SR01=01h, CR17 = A0h, GR06 = 0Bh, AR08 = 00h and AR10 = 07h.
7. Program extension registers XR0D, XR14, XR15, XR18, XR19, XR1A, XR1B, XR1C, XR1D and XR1E for the proper display type. (See following table.)
8. Set MDA Mode Control Register at 3B8h = 29h.

82C455 EXTENSION REGISTER VAULUES FOR BACKWARD COMPATIBILITY ON A VGA COMPATIBLE CRT

Register	CGA	MDA	HERC	EGA	VGA
XR0D	00	00	02	00	00
XR14	81	52	53	00	00
XR15	0D	0D	0D	18	00
XR16	00	00	00	00	00
XR17	00	00	00	00	00
XR18	27	00	59	00	00
XR19	2B	00	60	00	00
XR1A	A0	00	8F	00	00
XR1B	2D	00	6E	00	00
XR1C	28	00	5C	00	00
XR1D	10	00	31	00	00
XR1E	14	00	16	00	00
XR7E	30	0F	0F	----	----

For the MCA bus, D7=0.

82C455 EXTENSION REGISTER VALUES FOR BACKWARD COMPATIBILITY ON PANELS

Register	CGA	MDA	HERC	EGA	VGA
XR0D	00	00	02	00	00
XR14	81	52	53	00	80
XR15	0D	0D	0D	18	00
XR16	00	00	00	00	00
XR17	00	00	00	00	00
XR1E	14	28	16	----	----
XR7E	30	0F	0F	----	----

The Value in XR1D depends on the panel type used. The correct value for different panels types and compatibility modes is as follows:

Mode	LCD-DD	LCD-DS	PLASMA
VGA, EGA or MDA	9F	4F	4F
CGA	A0	50	50
Hercules	A1	50	50

Design Considerations

This section covers a variety of topics pertinent to designing a system which contains the 82C455.

CLOCK INPUTS

The 82C455 provides 3 dot clock inputs, CLK0, CLK1 and CLK2, one of which is selected via the Miscellaneous Output Register. The first two of these inputs are typically driven by 25.175 MHz and 28.322 MHz signals respectively ensuring VGA compatibility on a CRT monitor. The third input is usually used for a flat panel clock, however any of the three clocks may be used. The general purpose output pins on the 82C455 can be used in conjunction with external hardware to increase the number of clock input selections.

The MCLK input is used for internal sequencing of I/O cycles and is usually connected to CLK1 external to the 82C455.

ENABLING THE 82C455

After being reset the 82C455 is disabled. It must be explicitly enabled by writing to I/O address 102h in Setup Mode (per the MCA POS protocol).

In an MCA implementation, the 82C455 disappears from CPU memory and I/O space if the VGAENAB input is low. This pin should be controlled by bit-0 of port 3C3h; this port is *external* to the 82C455.

In the PC-Bus implementation, bit-3 of port 46E8h must be set to zero to disable the 82C455 and to one to enable it. When disabled, it is not visible in the CPU memory and I/O space. This port is *internal* to the 82C455.

Under normal circumstances, enable the 82C455 using one of the following sequences:

MCA Implementation:

1) Set bit-0 of port 3C3h (an off-chip register) to 1. This forces the VGAENAB input pin high.

2) Place the 82C455 in Setup mode by setting bit-5 at I/O address 94h to 1 (this causes the SETUP/ pin to go low).

3) Set bit-1 of port 102h to 1.

4) Place the 82C455 in its normal operating mode by setting bit-5 at I/O address 94h to 0.

PC-Bus Implementation:

1) Place the 82C455 in Setup mode by setting bit-3 at I/O address 46E8h to 1.

2) Set bit-1 of port 102h to 1.

3) Place the 82C455 in its normal operating mode by setting bit-4 at I/O address 46E8h to 0 and bit-3 to 1.

Disconnecting the Video Subsystem

The 82C455 and the Video Subsystem can be disconnected from the CPU as follows:

Disabling the 82C455:

This mode is entered after Reset or can be forced by the following technique.

- Write 0 to bit-3 of port 46E8h (PC Bus Interface) or force the VGAENAB pin low (MCA Interface).

- Enter Retire mode (PWRDN2 pin high).

Enabling the 82C455:

- Force the PWRDN2 pin low

- Set bits 4&3 of port 46E8h to 01 (PC Bus Interface) or force the VGAENAB pin high (MCA Interface)

External Color Palette

Although the external color palette is not used in the flat panel mode, the data contained in it is required by some applications. The mode 13 utility, SHADE455 (also contained in the Chips and Technologies BIOS), will not function properly without being able to read the palette data.

82C455 Application Schematic Examples

This section includes schematic examples showing
how to connect the 82C455 chip. The schematics
are broken down into four main groups for
discussion:

    1) System Bus Interface
    2) Display Memory Interface
    3) Video Interface
    4) Clock Interface

82C455 Circuit Example
8-Bit ISA Bus Interface

Pin	Signal		Pin	Signal	Alt

B02 — RESET
+5V — 82 — MCA/
114 — RESET
B19 — RFSH/ — 80 — RFSH/ [DISA/]
+5V — 72 — BHE/
A11 — AEN — 71 — AEN [MIO/]
B13 — IOWR/ — 79 — IOWR/ [SETUP/]
B14 — IORD/ — 68 — IORD/ [CMD/]
B11 — MEMW/ — 69 — MEMW/ [S0/]
B12 — MEMR/ — 70 — MEMR/ [S1/]
A10 — RDY — 74 — RDY
B04 — IRQ9 — 113 — IRQ

NC — 78 — IOCS16/ [VGAREQ/]
NC — 77 — MEN16/ [DS16/]
NC — 75 — WR46E8/ [CSFB/]

A12 — A19 — 41 — ADDHI
A13 — A18 — 42 — A18
A14 — A17 — 43 — A17
A15 — A16 — 44 — A16

GND = B1, B10, B31, D18
+5V = B3, B29, D16

38 — TEST
To Power Control — 40 — PWRDN2
Circuitry — 111 — PWRDN1

NC — 76 — ROMCS/ [POSIDEN/]

82C455
VGA

ENA — 19
DIR — 1 — +5V
A24 — A7 — 9 — 11 — BD7
A25 — A6 — 8 — 12 — BD6
A26 — A5 — 7 — 13 — BD5
A27 — A4 — 6 — 14 — BD4
A28 — A3 — 5 — 15 — BD3
A29 — A2 — 4 — 16 — BD2
A30 — A1 — 3 — 17 — BD1
A31 — A0 — 2 — 245 — 18 — BD0

A1..0 to RAMDAC

39 — DATEN/
67 — ADREN/
NC — 64 — RDHI/
A16 — A15 — 46 — AD15
A17 — A14 — 47 — AD14
A18 — A13 — 48 — AD13
A19 — A12 — 49 — AD12
A20 — A11 — 50 — AD11
A21 — A10 — 51 — AD10
A22 — A9 — 52 — AD9
A23 — A8 — 53 — AD8

ENA — 19
DIR — 1
A02 — D7 — 9 — 11 — BD7 — 65 — RDLO/
A03 — D6 — 8 — 12 — BD6 — 56 — AD7
A04 — D5 — 7 — 13 — BD5 — 57 — AD6
A05 — D4 — 6 — 14 — BD4 — 58 — AD5
A06 — D3 — 5 — 15 — BD3 — 59 — AD4
A07 — D2 — 4 — 16 — BD2 — 60 — AD3
A08 — D1 — 3 — 17 — BD1 — 61 — AD2
A09 — D0 — 2 — 245 — 18 — BD0 — 62 — AD1
63 — AD0

BD7..0 to RAMDAC

82C455 Circuit Example
16-Bit ISA Bus Interface

82C455
VGA

82 MCA/
114 RESET
80 RFSH/ [DISA/]
72 BHE/
71 AEN [MIO/]
79 IOWR/ [SETUP/]
68 IORD/ [CMD/]
69 MEMW/ [S0/]
70 MEMR/ [S1/]
74 RDY
113 IRQ

B42 RESET
A54 BHE/
A34 MIO/
A01 SETUP/
B34 CMD/
A32 S0/
A33 S1/
A36 RDY
B22 IRQ9/

+5V or motherboard logic register 102h bit-0

82C455 VGA

To CHIPS/250 or CHIPS/280 motherboard logic VGAREQ/
78 IOCS16/ [VGAREQ/]
77 MEN16/ [DS16/]

A55 DS16/

B36 CSFB/
75 WR46E8/ [CSFB/]

B11 A19 — 41 ADDHI
B12 A18 — 42 A18
B14 A17 — 43 A17
B15 A16 — 44 A16

ENA DIR 19 1 +5V
38 TEST
40 PWRDN2
111 PWRDN1

NC — 76 ROMCS/ [POSIDEN/]

B16 A15 9 — 11 BD15
B18 A14 8 — 12 BD14
B19 A13 7 — 13 BD13
B20 A12 6 — 14 BD12
A04 A11 5 — 15 BD11
A05 A10 4 — 16 BD10
A06 A9 3 — 17 BD9
A08 A8 2 — 18 BD8
H→ ⟷ A B 245

ENA DIR 19 1 +5V
A09 A7 9 — 11 BD7
A10 A6 8 — 12 BD6
A12 A5 7 — 13 BD5
A13 A4 6 — 14 BD4
A14 A3 5 — 15 BD3
A16 A2 4 — 16 BD2
A17 A1 3 — 17 BD1
A18 A0 2 — 18 BD0
H→ ⟷ A B 245

A1:0 to Color Palette

To Power Control Circuitry

82C455 Circuit Example MCA Bus Interface

ENA DIR 19 1
39 DATEN/
67 ADREN/
64 RDHI/
B53 D15 9 — 11 BD15 — 46 AD15
B52 D14 8 — 12 BD14 — 47 AD14
A51 D13 7 — 13 BD13 — 48 AD13
B51 D12 6 — 14 BD12 — 49 AD12
A50 D11 5 — 15 BD11 — 50 AD11
A49 D10 4 — 16 BD10 — 51 AD10
B49 D09 3 — 17 BD9 — 52 AD9
B48 D08 2 — 18 BD8 — 53 AD8
H→ ⟷ A B 245

ENA DIR 19 1
65 RDLO/
A42 D07 9 — 11 BD7 — 56 AD7
A41 D06 8 — 12 BD6 — 57 AD6
A40 D05 7 — 13 BD5 — 58 AD5
B40 D04 6 — 14 BD4 — 59 AD4
B39 D03 5 — 15 BD3 — 60 AD3
A38 D02 4 — 16 BD2 — 61 AD2
B38 D01 3 — 17 BD1 — 62 AD1
A37 D00 2 — 18 BD0 — 63 AD0
H→ ⟷ A B 245

BD7:0 to Color Palette

82C455
Display Memory
Circuit
64Kx4 DRAMs

82C455
VGA

82C455
Display Memory
Circuit
64Kx8 DRAMs

82C455 VGA

M3D7 133 — 9 D15
M3D6 131 — 8 D14
M3D5 129 — 7 D13
M3D4 125 — 6 D12
M3D3 123 — 5 D11
M3D2 121 — 4 D10
M3D1 119 — 3 D9
M3D0 116 — 2 D8
M2D7 132 — 19 D7
M2D6 130 — 18 D6
M2D5 128 — 17 D5
M2D4 124 — 16 D4
M2D3 122 — 15 D3
M2D2 120 — 14 D2
M2D1 118 — 12 D1
M2D0 115 — 11 D0

ZIP
1664
64Kx16
DRAM

BA7 32 — 36 A7
BA6 27 — 35 A6
BA5 23 — 34 A5
BA4 15 — 29 A4
BA3 11 — 28 A3
BA2 6 — 27 A2
BA1 2 — 26 A1
BA0 141 — 25 A0

R̄ C̄ Ū L̄ Ō
24 39 22 23 38

Note 1

74AC08   74AC08
74AC32
74AC32

CAS2/ 136
CAS3/ 137

M1D7 35 — 9 D15
M1D6 31 — 8 D14
M1D5 26 — 7 D13
M1D4 22 — 6 D12
M1D3 14 — 5 D11
M1D2 10 — 4 D10
M1D1 5 — 3 D9
M1D0 144 — 2 D8
M0D7 33 — 19 D7
M0D6 28 — 18 D6
M0D5 24 — 17 D5
M0D4 16 — 16 D4
M0D3 12 — 15 D3
M0D2 7 — 14 D2
M0D1 3 — 12 D1
M0D0 142 — 11 D0

ZIP
1664
64Kx16
DRAM

AA7 34 — 36 A7
AA6 29 — 35 A6
AA5 25 — 34 A5
AA4 21 — 29 A4
AA3 13 — 28 A3
AA2 8 — 27 A2
AA1 4 — 26 A1
AA0 143 — 25 A0

R̄ C̄ Ū L̄ Ō
24 39 22 23 38

RAS/ 20

Note 1

74AC08   74AC08
74AC32
74AC32

CAS0/ 134
CAS1/ 135
WE/ 139

Note 1. The 74AC08 delay path needs to be slightly longer than the 74AC32 gates on the upper and lower write enables to ensure that WE/ to CAS/ setup time is met. This will guarantee the DRAM will always be in EARLY-WRITE mode during write cycles.

82C455 Display Memory Circuit 64Kx16 DRAMs

Note: This circuit assumes the BT475 color palette chip is programmed to 'sleep' mode (via command register bit-0) to save power and blank the CRT display while the flat panel display is enabled.

J11 = DK455 Flat Panel
26-Pin Connector

82C455 VGA

82C455 VGA pin	signal
(TRAP/) LCD/	112
WGTCLK	83
SHFCLK	92
(M) ACDCLK	17
(LP) HSYNC	97
(FLM) VSYNC	98
(DE) BLANK/	96

241

FPEN/ — J11-4
SHFCLK — J11-9
ACDCLK — J11-1
HS — J11-5
VS — J11-3
HSYNC — J1-14
VSYNC — J1-13
NC WGTCLK — J11-7
NC BLANK/ — J11-2

244

P7 — J11-25
P6 — J11-23
P5 — J11-21
P4 — J11-19
P3 — J11-17
P2 — J11-15
P1 — J11-13
P0 — J11-11

+5V
4.7 uH
22 uF 0.1 0.047

PCLK 84 — 7 / 40 BLANK AVCC 4
P7 95 — 39 C7   AVCC 20
P6 94 — 38 C6   AVCC 21
P5 93 — 37 C5   AVCC 22
P4 89 — 36 C4   OPA 30
P3 88 — 35 C3   COMP 29
P2 87 — 34 C2
P1 86 — 33 C1   VREF 31 R_{set} 1%   1.2V
P0 85 — 32 C0   IREF 28   LM385
                SETUP 23   1K
PALRD/ 100 — 6 RD
PALWR/ 99 — 16 WR   AGND 3
                   AGND 24

(MS2) NC — J1-4
(MS1) NC — J1-12
(MS0) NC — J1-11

SENSE 108
              OL3 44
              OL2 43
              OL1 42
              OL0 41
(ERMEN/) 140 SYNC 5
GPOUT0   EXT 2
+5V

BT475 RAM DAC

R 25 — J1-1
G 26 — J1-2
B 27 — J1-3

R_L 150, 2%
NC — J1-9
NC — J1-15

D7 15 BD7
D6 14 BD6
D5 13 BD5
D4 12 BD4
D3 11 BD3
D2 10 BD2
D1 9 BD1
D0 8 BD0

SENSE 1
RS2 19
RS1 18
RS0 17

From A1
From A0

To Buffered Data Bus BD0-7   PLCC-44

J1 = CRT Analog Video
15-Pin Connector

470

Digital Ground
Analog Ground

J1-6
J1-7
J1-8

J1-10
J1-5

$$R_{set} \text{ (ohms)} = \frac{K * 1000 * V_{ref} \text{ (V)}}{I_{out} \text{ (mA)}}$$

R_L=75Ω, V_{out}=0.70V (I_{out}=18.67mA):
6-bit: K=3.000, R_{set}=193Ω
8-bit: K=3.175, R_{set}=204Ω

R_L=150Ω, V_{out}=0.64V (I_{out}=12.8mA):
6-bit: K=3.000, R_{set}=281Ω
8-bit: K=3.175, R_{set}=298Ω

**82C455 Video Circuit Example
For LCD Panels
(Brooktree BT475 Color Palette)**

Note: Flat panel signals P0-7, BLANK/, HS, VS, WGTCLK, and ACDCLK are never all needed at one time. The usual combinations are P0-7, HS, VS, SHFCLK, and ACDCLK or P0-3, HS, VS, SHFCLK, and WGTCLK.

Note: This circuit assumes the BT475 color palette chip is programmed to 'sleep' mode (via command register bit-0) to save power and blank the CRT display while the flat panel display is enabled.

J11 = DK455 Flat Panel
26-Pin Connector

(TRAP/) LCD/ 112
WGTCLK 83
SHFCLK 92
(M) ACDCLK 17
(LP) HSYNC 97
(FLM) VSYNC 98
(DE) BLANK/ 96

FPEN/ — J11-4
SHFCLK — J11-9
WGTCLK — J11-7
HS — J11-5
VS — J11-3
HSYNC — J1-14
VSYNC — J1-13
NC ACDCLK — J11-1
NC BLANK/ — J11-2

82C455
VGA

241

P7 — J11-25
P6 — J11-23
P5 — J11-21
P4 — J11-19
P3 — J11-17
P2 — J11-15
P1 — J11-13
P0 — J11-11

244

+5V
4.7 uH
22 uF   0.1   0.047

PCLK 84   BLANK AVCC 4
40   AVCC 20
AVCC 21
0.1   0.1
AVCC 22
P7 95   39 C7   AVCC 30
P6 94   38 C6   OPA 29   470
P5 93   37 C5   COMP
P4 89   36 C4
P3 88   35 C3   VREF 31   R_set 1%
P2 87   34 C2   IREF 28   1.2V
P1 86   33 C1   SETUP 23   LM385
P0 85   32 C0   1K
AGND 3
PALRD/ 100   6 RD   AGND 24   (MS2) NC — J1-4
PALWR/ 99   16 WR   (MS1) NC — J1-12
(MS0) NC — J1-11
BT475
SENSE 108   RAM   R 25 — J1-1
DAC   G 26 — J1-2
B 27 — J1-3
(ERMEN/)   44 OL3
GPOUT0 140   43 OL2   R_L
42 OL1   150, 2%
41 OL0   15 BD7   NC — J1-9
5 SYNC   D7   14 BD6   NC — J1-15
2 EXT   D6   13 BD5
+5V   D5   12 BD4
D4   11 BD3   J1-6
1 SENSE   D3   10 BD2   J1-7
From A1   19 RS2   D2   9 BD1   Digital Ground   J1-8
From A0   18 RS1   D1   8 BD0   Analog Ground
17 RS0   D0   J1-10
To Buffered Data Bus BD0-7   PLCC-44   J1-5

J1 = CRT Analog Video
15-Pin Connector

$$R_{set} \text{ (ohms)} = \frac{K * 1000 * V_{ref} \text{ (V)}}{I_{out} \text{ (mA)}}$$

R_L=75Ω, V_{out}=0.70V (I_{out}=18.67mA):
6-bit: K=3.000, R_{set}=193Ω
8-bit: K=3.175, R_{set}=204Ω

R_L=150Ω, V_{out}=0.64V (I_{out}=12.8mA):
6-bit: K=3.000, R_{set}=281Ω
8-bit: K=3.175, R_{set}=298Ω

**82C455 Video Circuit Example
For Plasma and EL Panels
(Brooktree BT475 Color Palette)**

Note: Flat panel signals P0-7, BLANK/, HS, VS, WGTCLK, and ACDCLK are never all needed at one time. The usual combinations are P0-7, HS, VS, SHFCLK, and ACDCLK or P0-3, HS, VS, SHFCLK, and WGTCLK.

82C455 Clock Circuit Example - Minimum Configuration

		82C455
28.322 MHz	101 MCLK	VGA
25.175 MHz	105 CLK0	
Panel Freq	104 CLK1	
	103 CLK2	
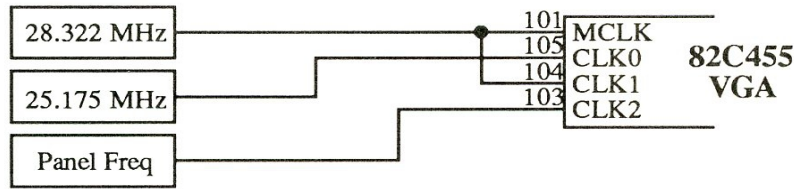
82C455 Clock Circuit Example - Minimum Configuration

82C455 Clock Circuit Example - Configuration For High Res CRT Mode Support

		82C455
28.322 MHz	101 MCLK	VGA
25.175 MHz	105 CLK0	
40.000 MHz	104 CLK1	
Panel Freq	103 CLK2	

LCD/ — SEL B A Y G — (ground)

82C455 Clock Circuit Example - Configuration For High Res CRT Mode Support

Clock Chip Configuration

RESET
IOWR/
D3
D2
AEN

Pin		PAL 16L8	
A9	1	I	
A8	2	I	
A7	3	I O 19	Q2
A6	4	I O 18	
A5	5	I I/O 17	
A4	6	I I/O 16	
A3	7	I I/O 15	
A2	8	I I/O 14	
A1	9	I I/O 13	WR3C2/
A0	11	I O 12	Q3

28 – 40 MHz

Clock Gen: SEL0, SEL1, SEL2, SEL3, REF, OUT

PWRDN — SEL2
LCD/ — SEL3
14.31818 MHz — REF

		82C455
101	MCLK	VGA
103	CLK0	
104	CLK1	
105	CLK2	

SEL				Clock Gen
3	**2**	**1**	**0**	**Frequency**
0	0	0	0	Panel Freq
0	0	0	1	Panel Freq
0	0	1	0	Panel Freq
0	0	1	1	Panel Freq
0	1	0	0	Low Freq
0	1	0	1	Low Freq
0	1	1	0	Low Freq
0	1	1	1	Low Freq
1	0	0	0	25.175 MHz
1	0	0	1	28.322 MHz
1	0	1	0	40.000 MHz
1	0	1	1	0 MHz
1	1	0	0	Low Freq
1	1	0	1	Low Freq
1	1	1	0	Low Freq
1	1	1	1	Low Freq

!Q2 = !RESET & !WR3C2 & !D2
    + !RESET & WR3C2 & !Q2
    + !RESET & !D2 & !Q2

!Q3 = !RESET & !WR3C2 & !D3
    + !RESET & WR3C2 & !Q3
    + !RESET & !D3 & !Q3

WR3C2 = IOWR & !AEN & A9 & A8 & A7 & A6 & !A5 & !A4 & !A3 & !A2 & !A1 & !A0

82C455 Clock Circuit Example - Clock Chip Configuration

82C455 Flat Panel Interface Examples

This section includes schematic examples showing how to connect the 82C455 chip to various flat panels.

1) Epson   EG-9005F-LS   (DD LCD Panel)
2) Hitachi   LMG6221XUFE   (DD LCD Panel)
3) Sharp   LM6418Z   (DD LCD Panel)
4) Sanyo   LCM-5464-24NAK (DD LCD Panel)
5) Citizen   G481L-FF   (DD LCD Panel)
6) Hitachi   TM26D01VC   (TFT Color Panel)
7) Panasonic MD480F640PG1   (Plasma Panel)
8) Finlux   MD640.350   (EL Panel)

DK82C455
Development Kit PCB
Connector J11

Epson EG-9005F-LS
Panel Connector

Epson Pin	Signal		J11 Pin (odd)	Signal	J11 Pin (even)	Signal
1	VDD		1	ACDCLK	2	BLANK/
2	VSS		3	VS	4	FPEN/
3	VLCD		5	HS	6	+5V
4	LP		7	WGTCLK	8	+5V
5	FR		9	SHFCLK	10	+5V
6	NC		11	P0	12	+5V
7	YSCL		13	P1	14	GND
8	DIN		15	P2	16	GND
9	XSCL		17	P3	18	GND
10	NC		19	P4	20	GND
11	UD0		21	P5	22	GND
12	UD1		23	P6	24	GND
13	UD2		25	P7	26	GND
14	UD3					
15	LD0					
16	LD1					
17	LD2					
18	LD3					
19	EI					
20	EO					

GND   +5V   -23V

82C455 Panel Hookup - Epson EG-9005F-LS (DD LCD Panel)
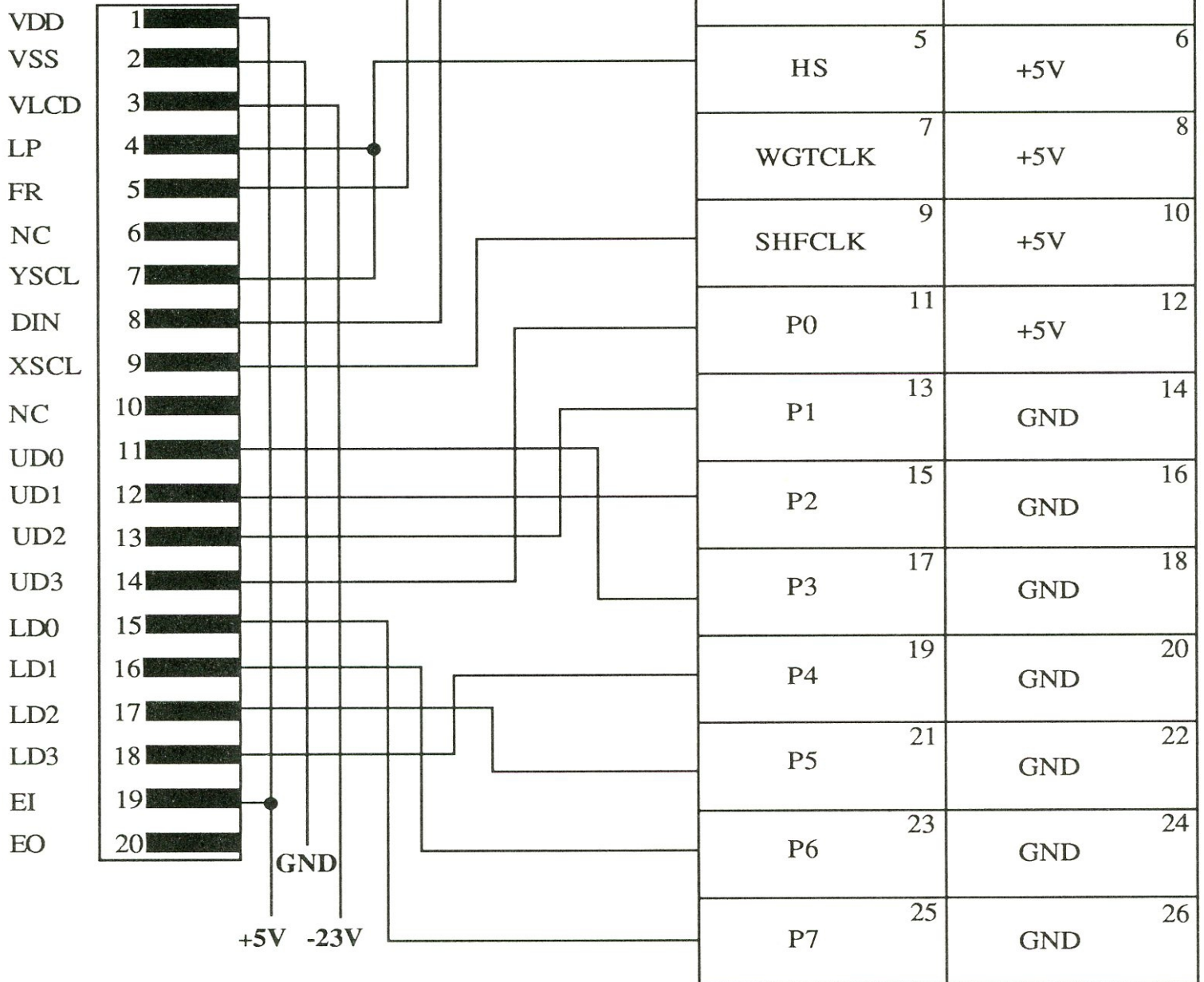
Hitachi LMG6221XUFE
Panel Connector

DK82C455
Development Kit PCB
Connector J11

Panel Pin	Signal		J11		
1	UD0		1 ACDCLK	2 BLANK/
2	UD1		3 VS	4 FPEN/
3	UD2		5 HS	6 +5V
4	UD3		7 WGTCLK	8 +5V
5	DISPOFF		9 SHFCLK	10 +5V
6	FLM		11 P0	12 +5V
7	DF		13 P1	14 GND
8	LOAD		15 P2	16 GND
9	CP		17 P3	18 GND
10	LD0		19 P4	20 GND
11	LD1		21 P5	22 GND
12	LD2		23 P6	24 GND
13	LD3		25 P7	26 GND
14	VSS			
15	VDD			

+5V

GND

82C455 Panel Hookup - Hitachi LMG6221XUFE (DD LCD Panel)

Sharp LM6418Z
Panel Connector

S	1	
CP1	2	
CP2	3	
NC	4	
NC	5	
VDD	6	
VSS	7	
VEE	8	
DU0	9	
DU1	10	
DU2	11	
DU3	12	
DL0	13	
DL1	14	
DL2	15	
DL3	16	

+5V

GND

+16V

DK82C455
Development Kit PCB
Connector J11

1 ACDCLK	2 BLANK/
3 VS	4 FPEN/
5 HS	6 +5V
7 WGTCLK	8 +5V
9 SHFCLK	10 +5V
11 P0	12 +5V
13 P1	14 GND
15 P2	16 GND
17 P3	18 GND
19 P4	20 GND
21 P5	22 GND
23 P6	24 GND
25 P7	26 GND

82C455 Panel Hookup - Sharp LM6418Z (DD LCD Panel)

82C455 Panel Hookup - Sanyo LCM-5464-24NAK (DD LCD Panel)

DK82C455
Development Kit PCB
Connector J11

Citizen G6481L-FF
Panel Connector

Citizen G6481L-FF Panel Connector		
+28V	1	
+28V	2	
GND	3	
VCC	4	
DISPOFF	5	
NC	6	
CP	7	
LOAD	8	
DF	9	
FRAME	10	
UD3	11	
UD2	12	
UD1	13	
UD0	14	
LD3	15	
LD2	16	
LD1	17	
LD0	18	
N/C	19	
N/C	20	

+28v

+5v

GND

1 ACDCLK	2 BLANK/
3 VS	4 FPEN/
5 HS	6 +5V
7 WGTCLK	8 +5V
9 SHFCLK	10 +5V
11 P0	12 +5V
13 P1	14 GND
15 P2	16 GND
17 P3	18 GND
19 P4	20 GND
21 P5	22 GND
23 P6	24 GND
25 P7	26 GND
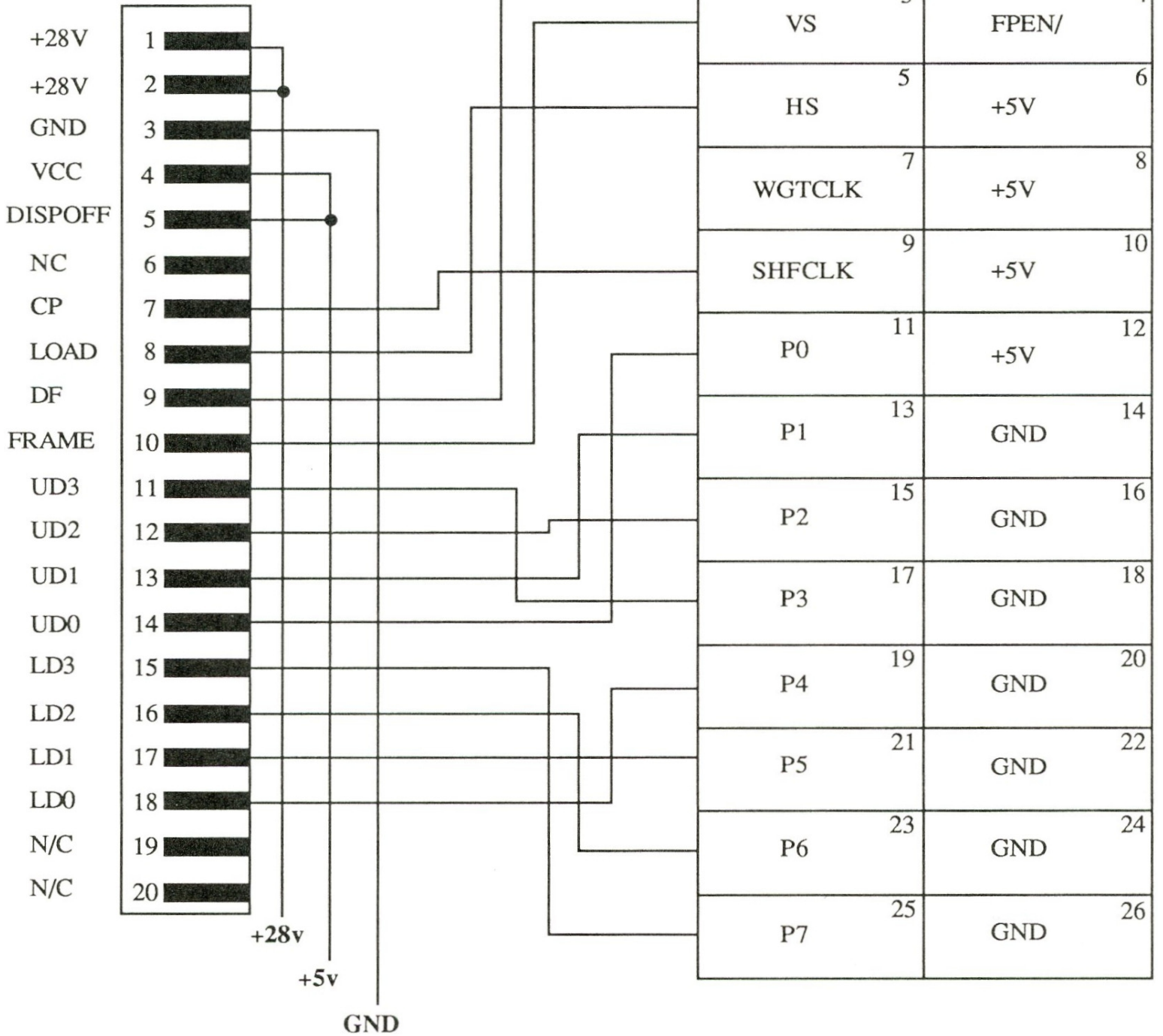
82C455 Panel Hookup - Citizen G481L-FF (DD LCD Panel)

DK82C455
Development Kit PCB
Connector J11

ACDCLK	1	BLANK/	2
VS	3	FPEN/	4
HS	5	+5V	6
WGTCLK	7	+5V	8
SHFCLK	9	+5V	10
P0	11	+5V	12
P1	13	GND	14
P2	15	GND	16
P3	17	GND	18
P4	19	GND	20
P5	21	GND	22
P6	23	GND	24
P7	25	GND	26

Hitachi TM26D01VC
Panel Connector

VSS	1
VSS	2
VSS	3
VSS	4
NC	5
VLCD	6
VLCD	7
	8
DOTE	9
VSS	10
VDD	11
VSYNC	12
VDD	13
HSYNC	14
VSS	15
DTMG	16
VSS	17
GD	18
VSS	19
RD	20
VSS	21
BD	22
	23
VSS	24
VSS	25
DCLK	26
VSS	27
VSS	28
VSS	29
VSS	30

GND | +5V

+25V

82C455 Panel Hookup - Hitachi TM26D01VC (TFT Color Panel)

DK82C455
Development Kit PCB
Connector J11

Panasonic
MD480F640PG1
Panel Connector J1

Panel Connector J1		DK82C455 Connector J11	
VDD	1	1 ACDCLK	2 BLANK/
VDD	2	3 VS	4 FPEN/
ENA	3	5 HS	6 +5V
VSS	4	7 WGTCLK	8 +5V
VSYNC	5	9 SHFCLK	10 +5V
VSS	6	11 P0	12 +5V
HSYNC	7	13 P1	14 GND
VSS	8	15 P2	16 GND
BLANK	9	17 P3	18 GND
VSS	10	19 P4	20 GND
CLOCK	11	21 P5	22 GND
VSS	12	23 P6	24 GND
DATA0	13	25 P7	26 GND
VSS	14		
DATA1	15		
VSS	16		
DATA2	17		
VSS	18		
DATA3	19		
VSS	20		

+5V

GND

82C455 Panel Hookup - Panasonic MD480F640PG1 (Plasma Panel)

Finlux MD640.350
Panel Connector J3

DK82C455
Development Kit PCB
Connector J11

	1		2
	ACDCLK		BLANK/
	3		4
	VS		FPEN/
	5		6
	HS		+5V
	7		8
	WGTCLK		+5V
	9		10
	SHFCLK		+5V
	11		12
	P0		+5V
	13		14
	P1		GND
	15		16
	P2		GND
	17		18
	P3		GND
	19		20
	P4		GND
	21		22
	P5		GND
	23		24
	P6		GND
	25		26
	P7		GND

VCC2 1
VCC2 2
VCC1 3
VCC1 4
NC 5
NC 6
GND 7
GND 8
VS 9
GND 10
HS 11
GND 12
VCLK 13
GND 14
VID 15
GND 16

+12v

+5v

GND

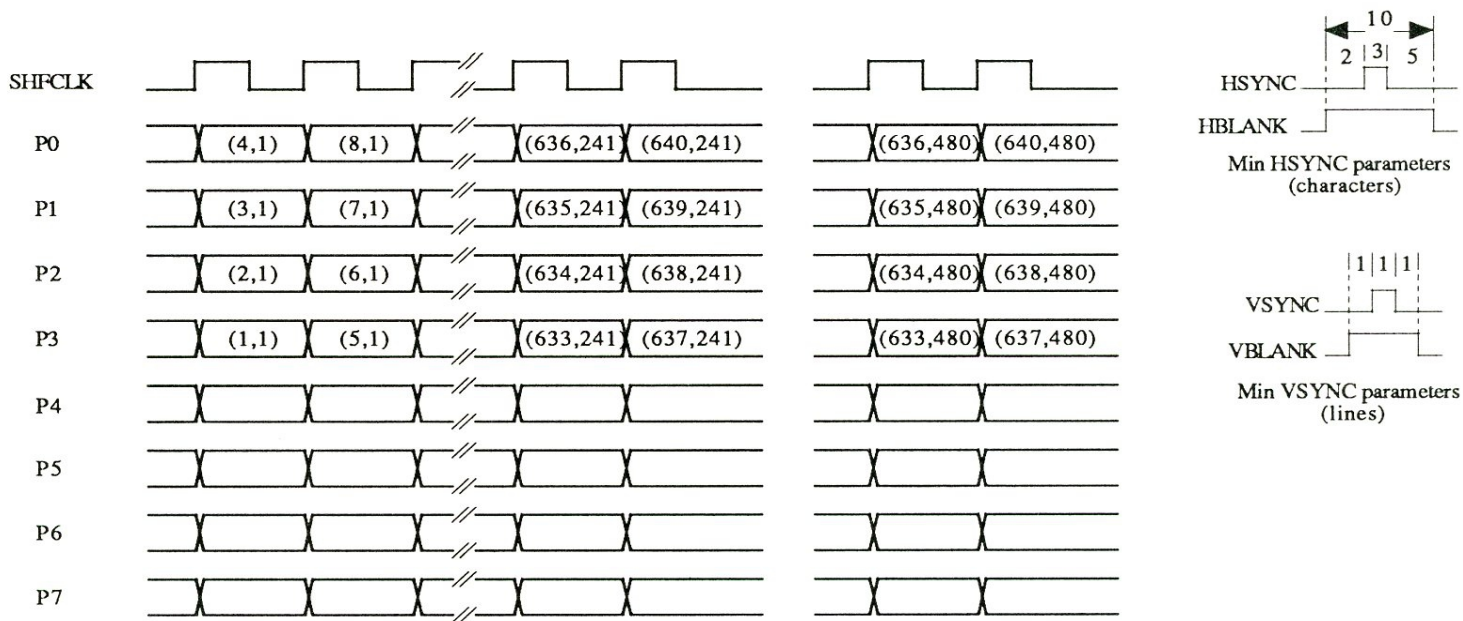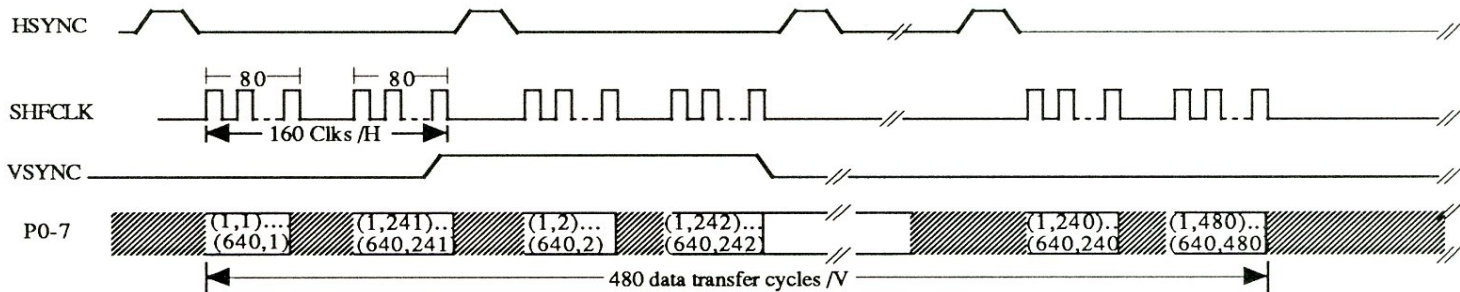82C455 Panel Hookup - Finlux MD640.350 (EL Panel)

82C455 Flat Panel Timing

This section shows detailed timing diagrams for the 82C455 outputting data and control sequences to a variety of panel types. The panel types included are:
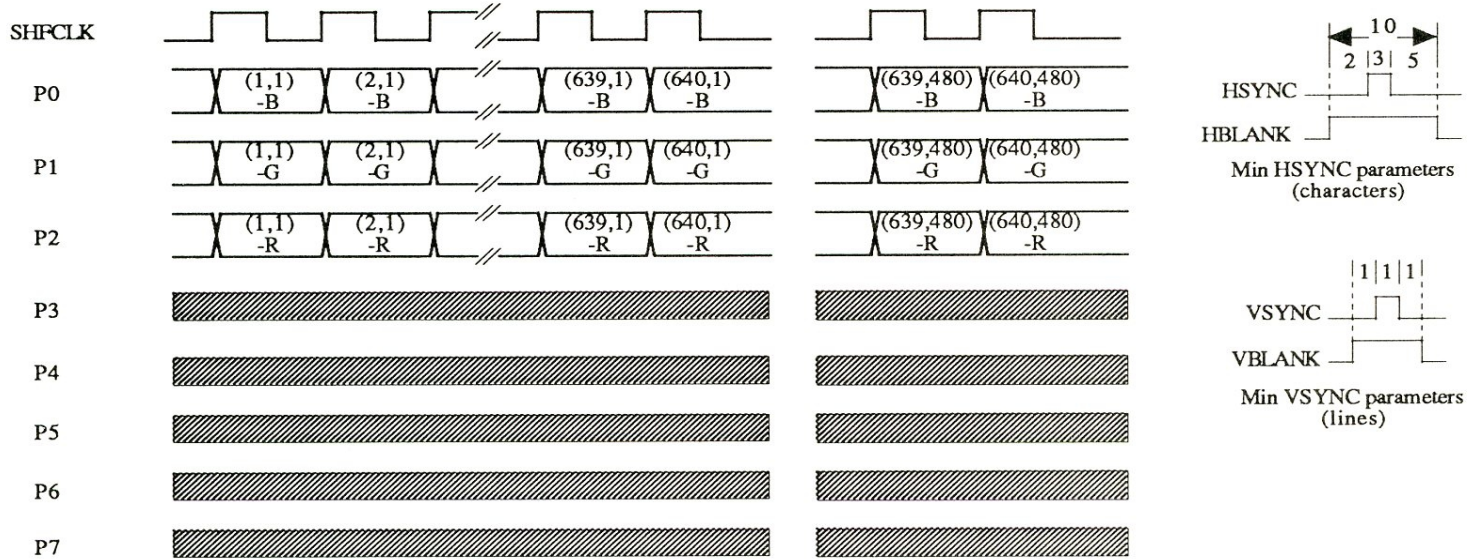
1) Dual Panel Double Drive 640x480
   Monochrome LCD Panel

2) Dual Panel Single Drive 640x480
   Monochrome LCD Panel

3) Single Panel Single Drive 640x480
   TFT Color LCD Panel

4) Dual Panel Single Drive 640x480 (4-Bit Pack)
   STN Color LCD Panel

5) Dual Panel Single Drive 640x480 (3-Bit)
   STN Color LCD Panel

6) 16-Level PWM Plasma Panel
   2 Pixels/Shift-Clock, 4 Bits/Pixel Interface

7) 16-Level PWM EL Panel
   2 Pixels/Shift-Clock, 4 Bits/Pixel Interface
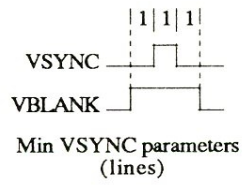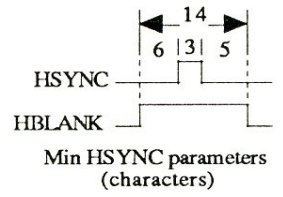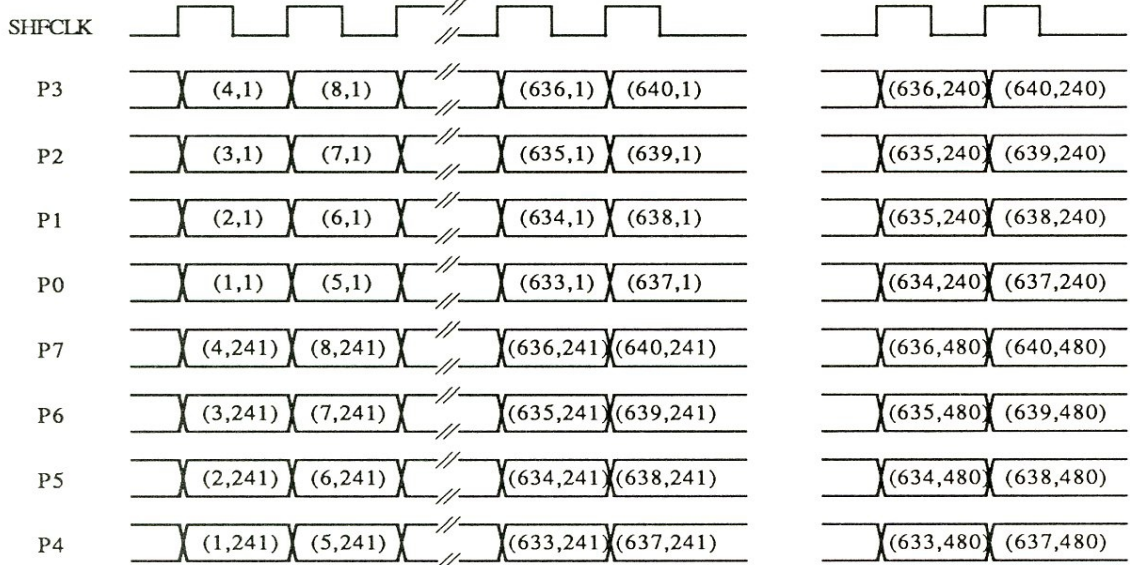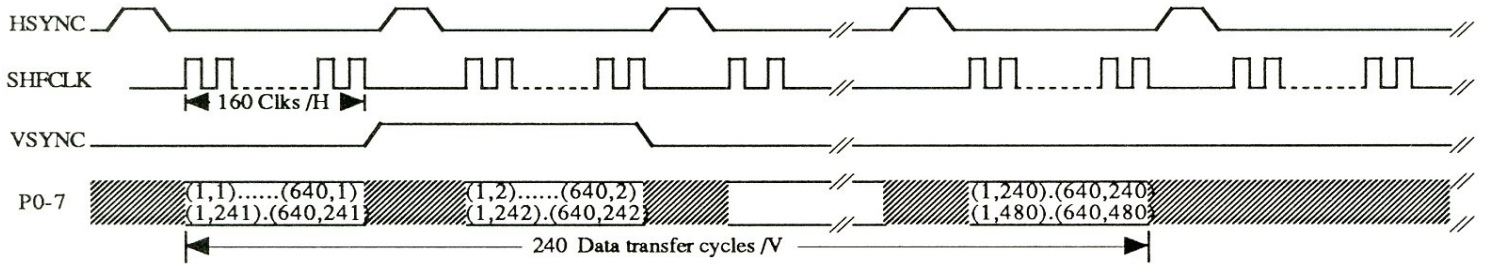
82C455 Panel Timing - LCD DD

82C455 Panel Timing - LCD DS

HSYNC

WGTCLK

SHFCLK |← 640 Clks /H →|

VSYNC

P0-7   (1,1).........(640,1)   (1,2)..........(640,2)   (1,480)....(640,480)

|← 480 data transfer cycles /V →|

SHFCLK

P0   (1,1) -B   (2,1) -B   (639,1) -B   (640,1) -B   (639,480) -B   (640,480) -B

P1   (1,1) -G   (2,1) -G   (639,1) -G   (640,1) -G   (639,480) -G   (640,480) -G

P2   (1,1) -R   (2,1) -R   (639,1) -R   (640,1) -R   (639,480) -R   (640,480) -R

P3

P4

P5

P6

P7

|← 10 →|
2 |3| 5

HSYNC

HBLANK

Min HSYNC parameters
(characters)

|1|1|1|

VSYNC

VBLANK

Min VSYNC parameters
(lines)
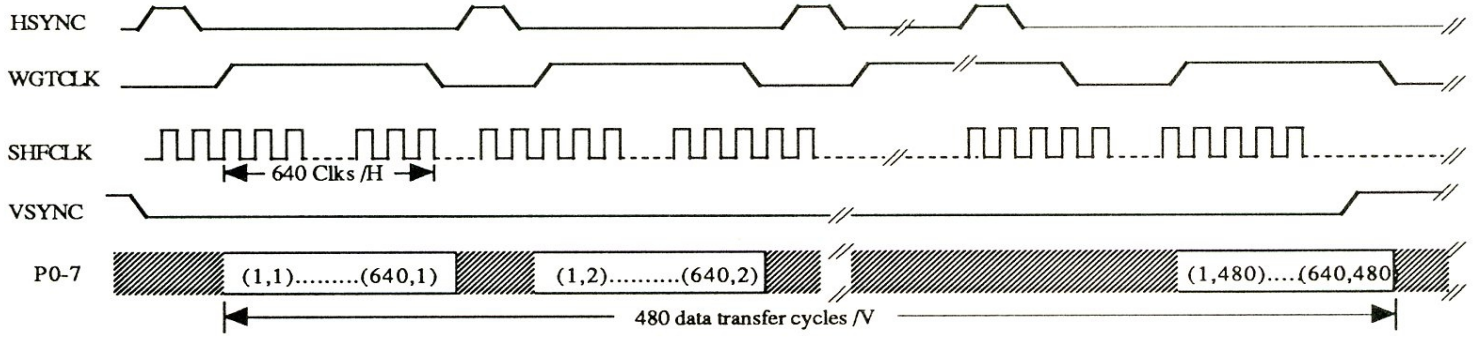
82C455 Panel Timing - TFT Color LCD SS
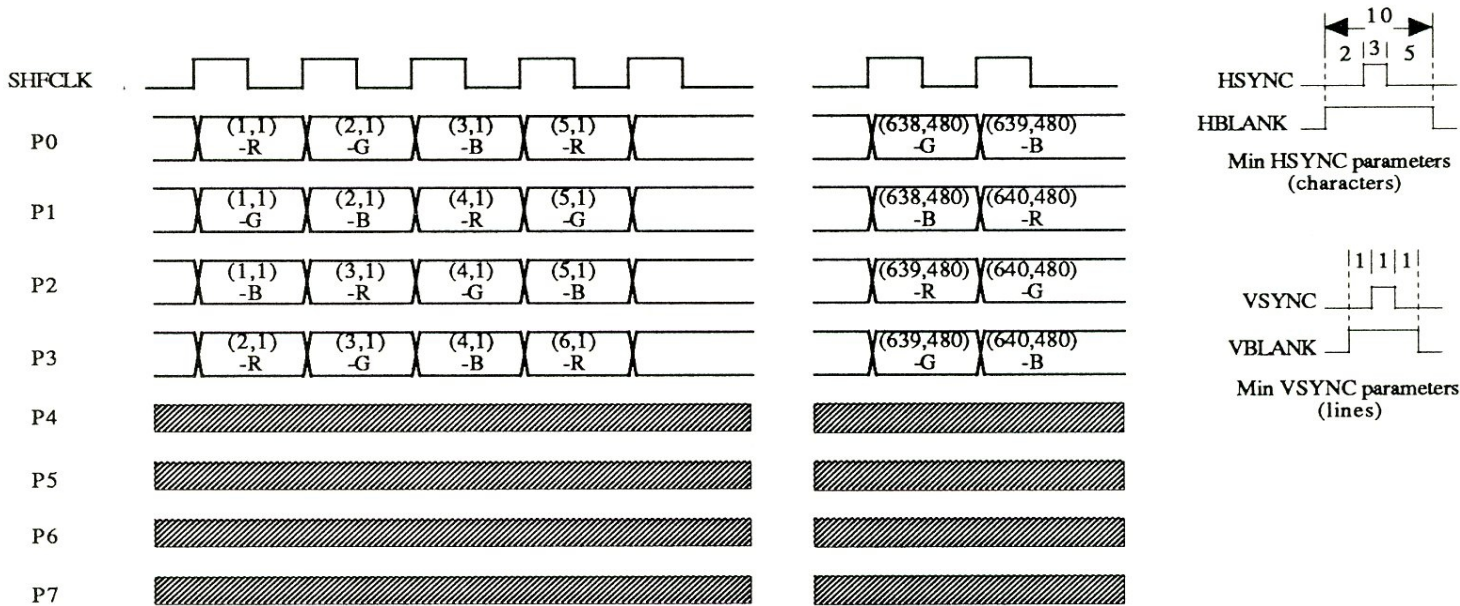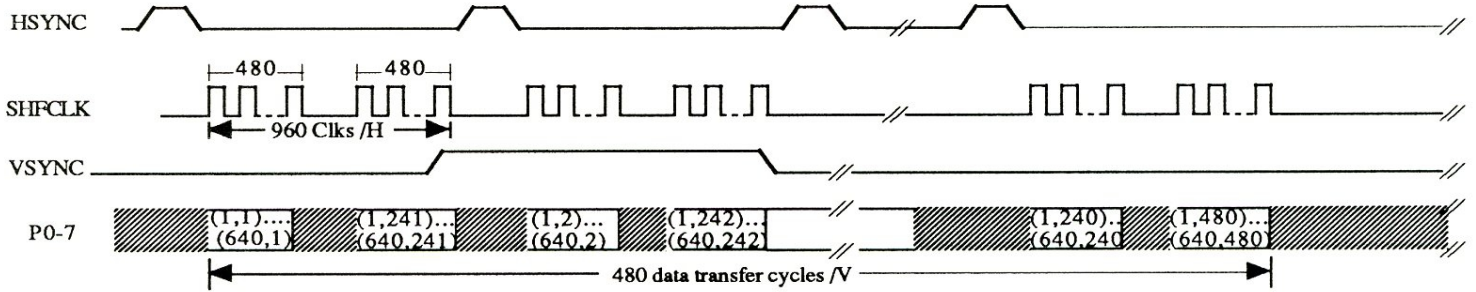
82C455 Panel Timing - STN Color LCD DS (4-Bit Pack)

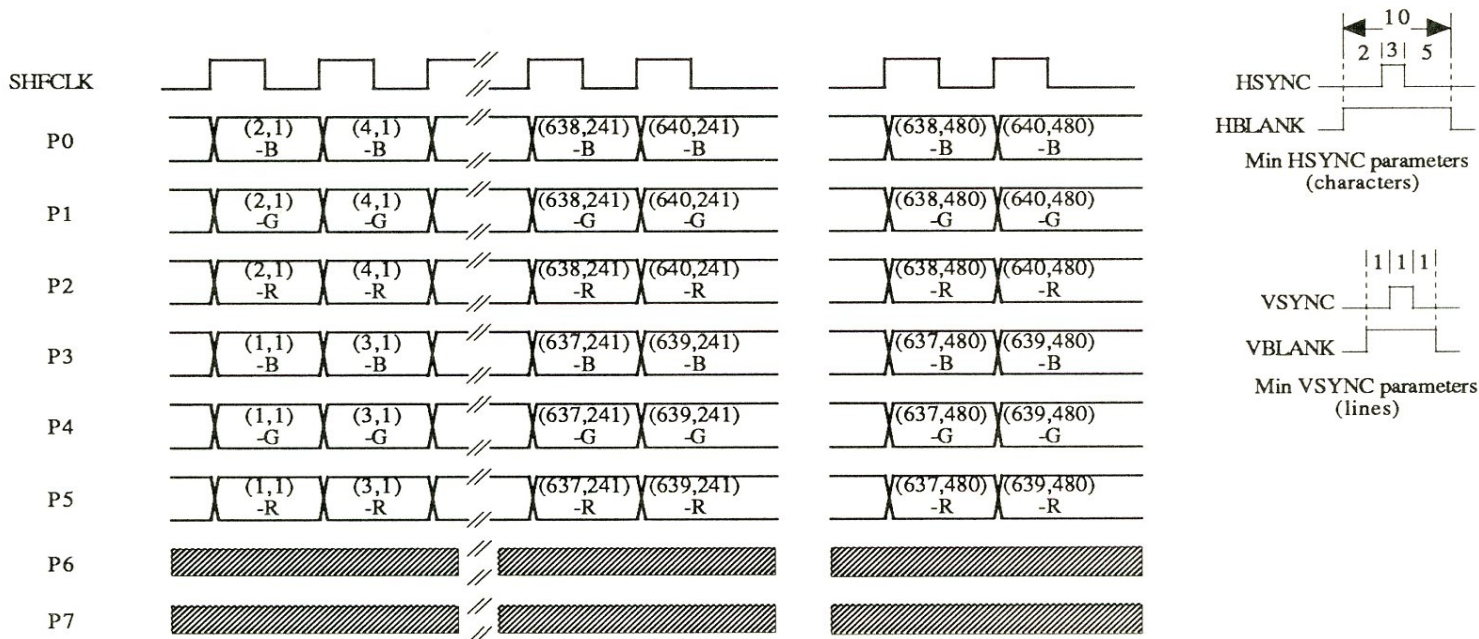**82C455 Panel Timing - STN Color LCD DS (3-Bit)**
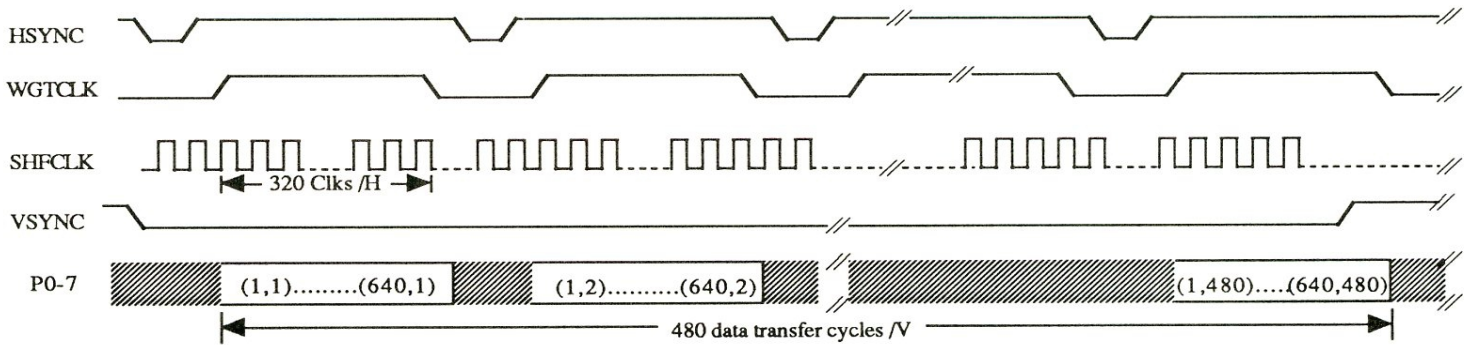
82C455 Panel Timing - Plasma (16-Level PWM) 2 Pixels/Shift Clock

HSYNC

WGTCLK

SHFCLK
|← 320 Clks /H →|

VSYNC

P0-7 (1,1).........(640,1) (1,2).........(640,2) (1,480).....(640,480)

|←———————— 480 data transfer cycles /V ————————→|

$\overline{\text{SHFCLK}}$

P0	(2,1) -1	(4,1) -1	(638,1) -1	(640,1) -1	(638,480) -1	(640,480) -1
P1	(2,1) -2	(4,1) -2	(638,1) -2	(640,1) -2	(638,480) -2	(640,480) -2
P2	(2,1) -4	(4,1) -4	(638,1) -4	(640,1) -4	(638,480) -4	(640,480) -4
P3	(2,1) -8	(4,1) -8	(638,1) -8	(640,1) -8	(638,480) -8	(640,480) -8
P4	(1,1) -1	(3,1) -1	(637,1) -1	(639,1) -1	(637,480) -1	(639,480) -1
P5	(1,1) -2	(3,1) -2	(637,1) -2	(639,1) -2	(637,480) -2	(639,480) -2
P6	(1,1) -4	(3,1) -4	(637,1) -4	(639,1) -4	(637,480) -4	(639,480) -4
P7	(1,1) -8	(3,1) -8	(637,1) -8	(639,1) -8	(637,480) -8	(639,480) -8

10
2 |3| 5

HSYNC

HBLANK

Min HSYNC parameters
(characters)

|1|1|1|

VSYNC

VBLANK

Min VSYNC parameters
(lines)

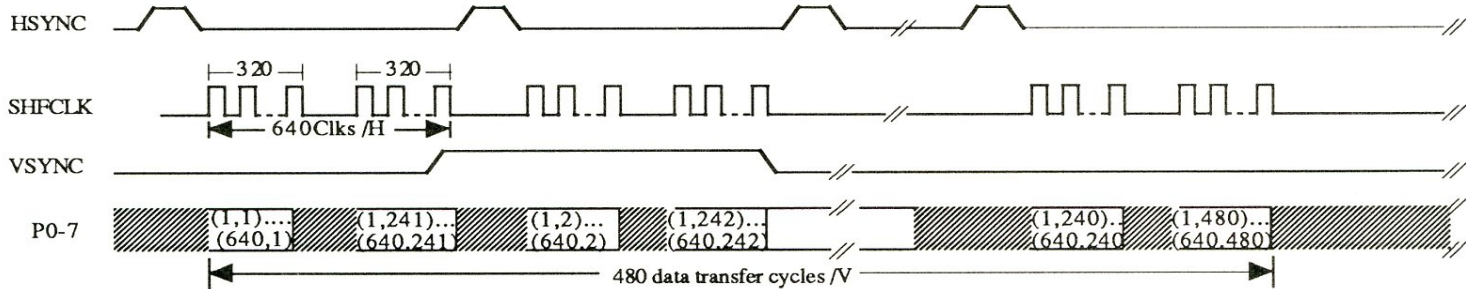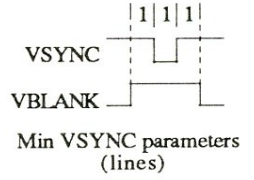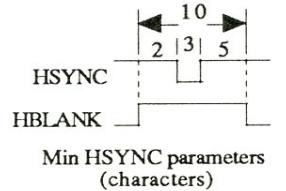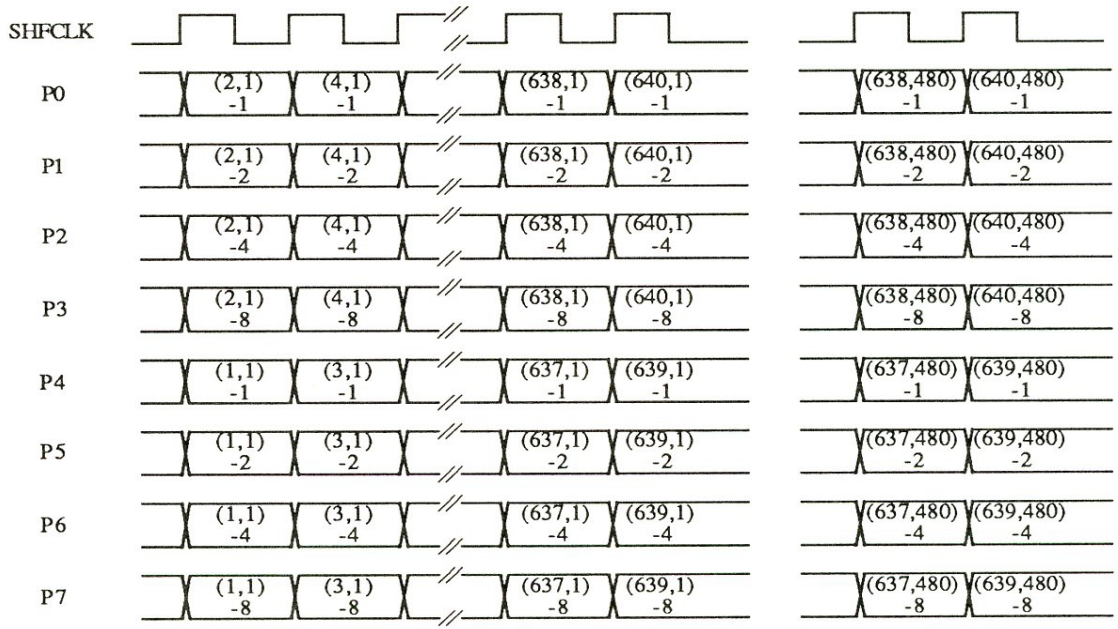**82C455 Panel Timing - EL (16-Level PWM) 2 Pixels/Shift Clock**

82C455 Flat Panel Pixel Timing

The 82C455 is the most flexible flat panel graphics controller available, enabling the widest possible range of panel interfaces. This section includes timing diagrams for various scenarios, such as various clock divides, color and monochrome panels, and different levels of Pulse Width Modulation (PWM). The following timing diagrams are included:

1) Single Drive (CD=00, 01)
2) Single Drive (CD=10, 11)
3) Single Drive (CD=00, 01) 16-Level PWM
4) Single Drive Color 3-Bit Pack (CD=00, 01)
5) Single Drive Color 4-Level PWM
6) Single Drive Color 4-Bit Pack (PWM=00, 01)
7) Double Drive Monochrome (CD=11)

Extension register 50 (XR50) bits 5-4 define the clock divide (CD):

00 - Shift clock frequency = dot clock frequency
01 - Shift clock frequency = dot clock frequency/2
10 - Shift clock frequency = dot clock frequency/4
11 - Shift clock frequency = dot clock frequency/8

Extension register 51 (XR51) bits 5-4 define Mono/Color Panel Mode (MCP):

00 - Color Panel (3-bit data)
01 - Color Panel (4-bit data pack)
10 - Monochrome Panel
11 - Reserved

Extension register 50 (XR50) bits 3-2 define Pulse Width Modulation (PWM):

00 - No gray levels
01 - 4 levels of color supported by the panel
10 - 16 levels of gray supported by the panel
11 - 256 levels of color supported by the panel
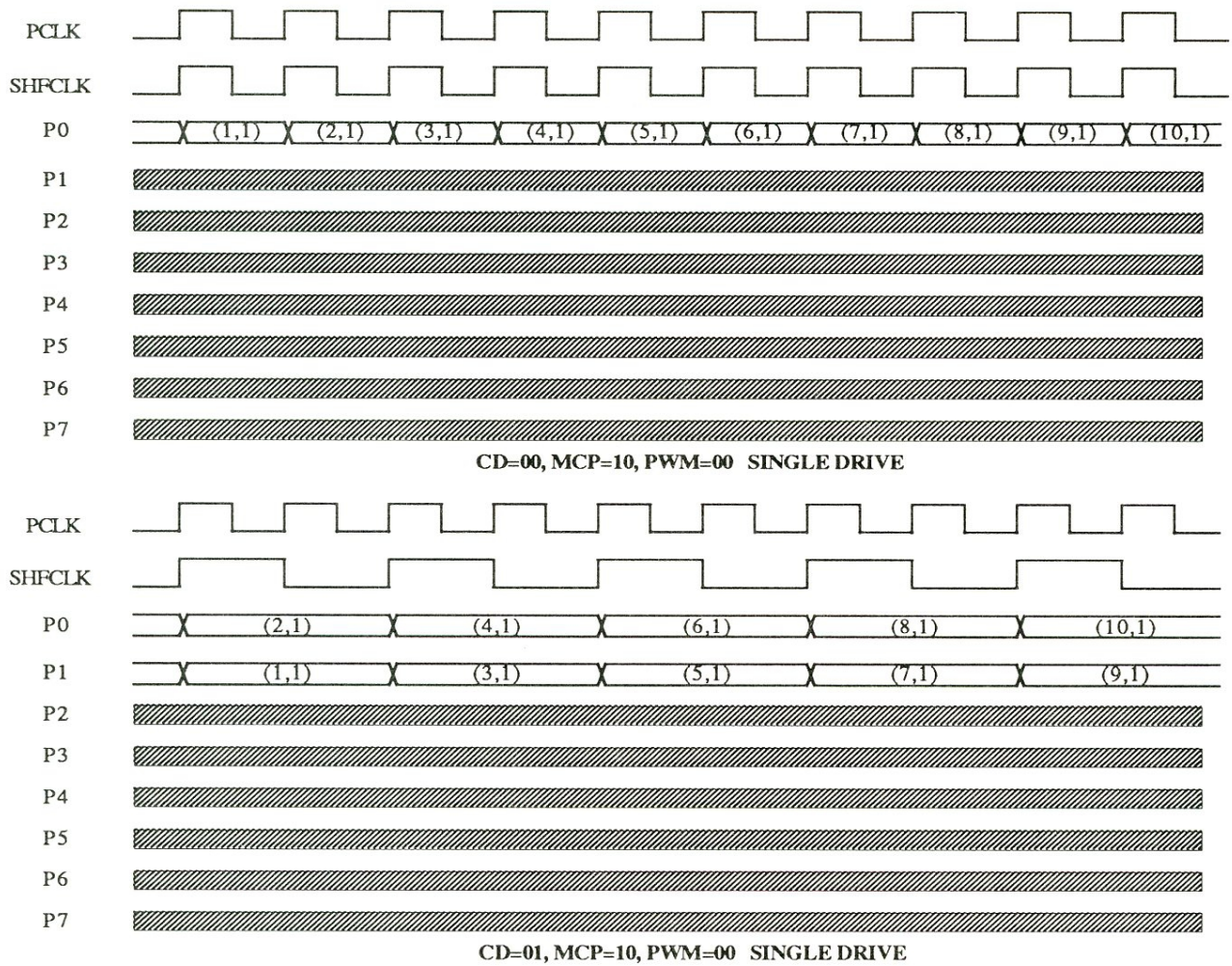
CD=00, MCP=10, PWM=00 SINGLE DRIVE

CD=01, MCP=10, PWM=00 SINGLE DRIVE

82C455 Panel Pixel Timing - Single Drive (Clock Divide 00 & 01)

These timing diagrams show the 82C455 outputs to the flat panel for two scenarios:

1) One pixel per shift clock (where shift clock frequency = dot clock frequency) for monochrome panels with no internal gray-scale generation

2) Two pixels per shift clock (where shift clock frequency = dot clock frequency / 2) for monochrome panels with no internal gray-scale generation

PCLK

SHFCLK

P0   (4,1)   (8,1)   (12,1)

P1   (3,1)   (7,1)   (11,1)

P2   (2,1)   (6,1)   (10,1)

P3   (1,1)   (5,1)   (9,1)

P4

P5

P6

P7

CD=10, MCP=10, PWM=00   SINGLE DRIVE

PCLK

SHFCLK

P0   (8,1)

P1   (7,1)

P2   (6,1)

P3   (5,1)

P4   (4,1)

P5   (3,1)

P6   (2,1)

P7   (1,1)

CD=11, MCP=10, PWM=00   SINGLE DRIVE
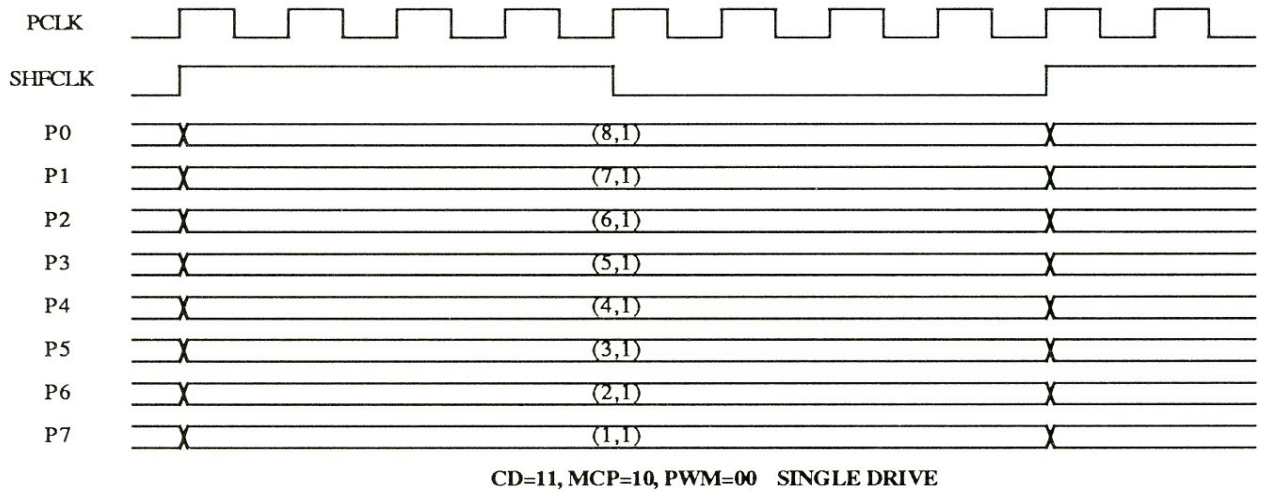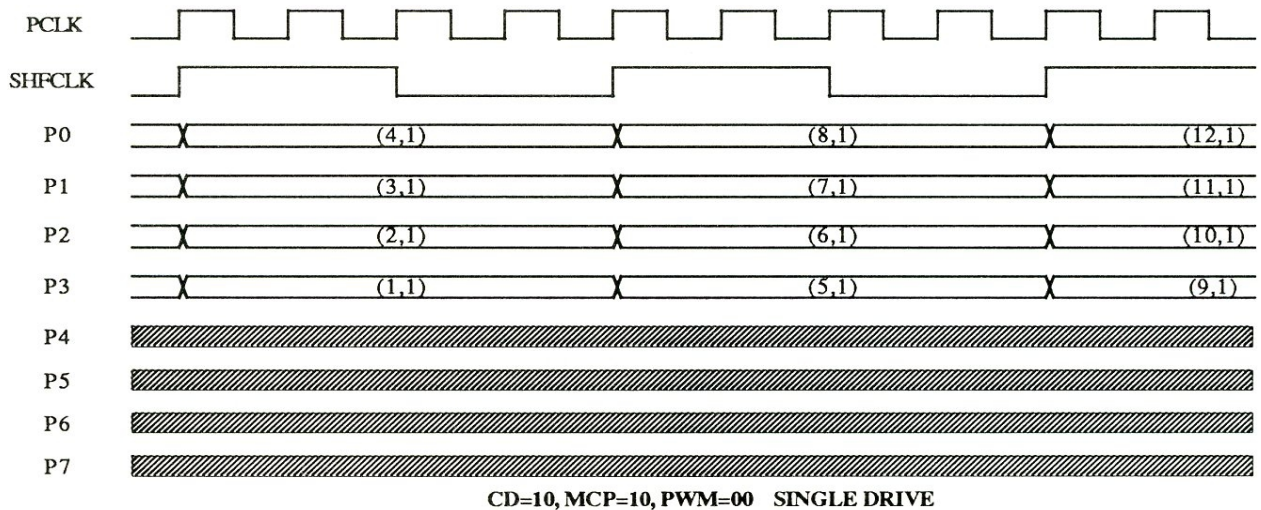
82C455 Panel Pixel Timing - Single Drive (Clock Divide 10 & 11)

These timing diagrams show the 82C455 outputs to the flat panel for two scenarios:

1) Four pixels per shift clock (where shift clock frequency = dot clock frequency / 4) for monochrome panels with no internal gray-scale generation

2) Eight pixels per shift clock (where shift clock frequency = dot clock frequency / 8) for monochrome panels with no internal gray-scale generation

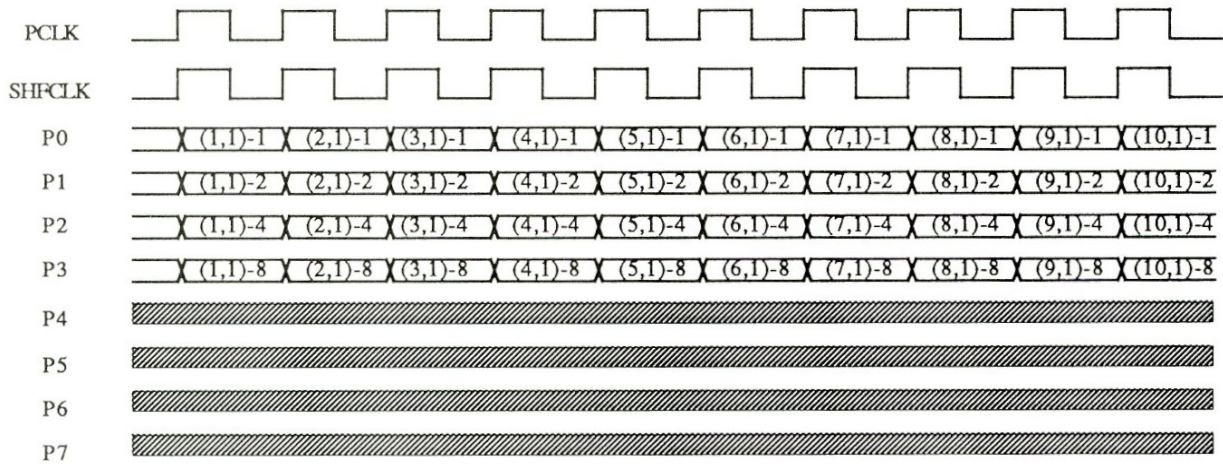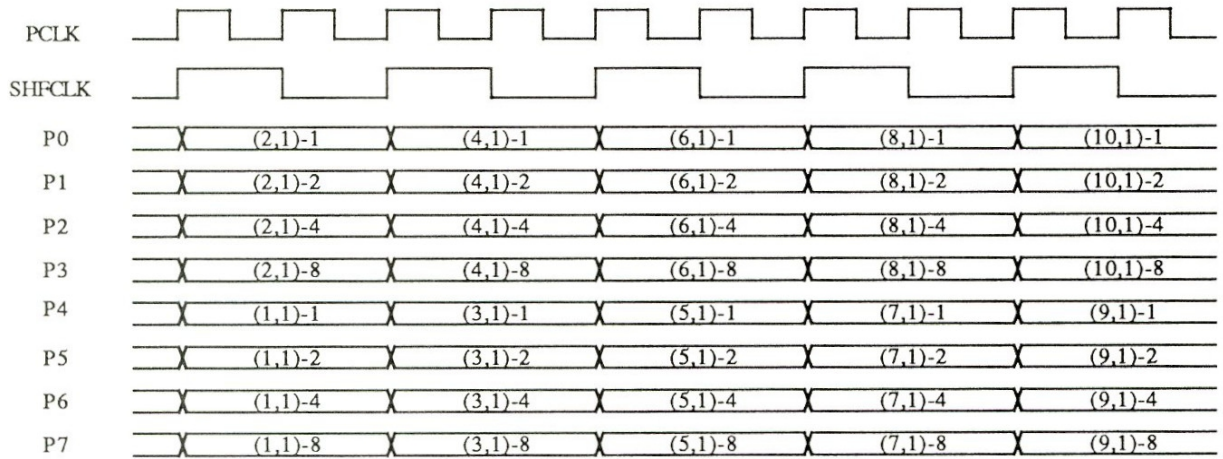| PCLK										
SHFCLK										
P0	(1,1)-1	(2,1)-1	(3,1)-1	(4,1)-1	(5,1)-1	(6,1)-1	(7,1)-1	(8,1)-1	(9,1)-1	(10,1)-1
P1	(1,1)-2	(2,1)-2	(3,1)-2	(4,1)-2	(5,1)-2	(6,1)-2	(7,1)-2	(8,1)-2	(9,1)-2	(10,1)-2
P2	(1,1)-4	(2,1)-4	(3,1)-4	(4,1)-4	(5,1)-4	(6,1)-4	(7,1)-4	(8,1)-4	(9,1)-4	(10,1)-4
P3	(1,1)-8	(2,1)-8	(3,1)-8	(4,1)-8	(5,1)-8	(6,1)-8	(7,1)-8	(8,1)-8	(9,1)-8	(10,1)-8
P4										
P5										
P6										
P7										

CD=00, MCP=10, PWM=10 SINGLE DRIVE

PCLK					
SHFCLK					
P0	(2,1)-1	(4,1)-1	(6,1)-1	(8,1)-1	(10,1)-1
P1	(2,1)-2	(4,1)-2	(6,1)-2	(8,1)-2	(10,1)-2
P2	(2,1)-4	(4,1)-4	(6,1)-4	(8,1)-4	(10,1)-4
P3	(2,1)-8	(4,1)-8	(6,1)-8	(8,1)-8	(10,1)-8
P4	(1,1)-1	(3,1)-1	(5,1)-1	(7,1)-1	(9,1)-1
P5	(1,1)-2	(3,1)-2	(5,1)-2	(7,1)-2	(9,1)-2
P6	(1,1)-4	(3,1)-4	(5,1)-4	(7,1)-4	(9,1)-4
P7	(1,1)-8	(3,1)-8	(5,1)-8	(7,1)-8	(9,1)-8

CD=10, MCP=10, PWM=10 SINGLE DRIVE

01

82C455 Panel Pixel Timing - Single Drive (Clock Divide 00 & 01) 16-Level PWM

These timing diagrams show the 82C455 outputs for a monochrome flat panel display with 16 levels of internal gray scale generation. Two scenarios are presented:

1) One pixel per shift clock (where shift clock frequency = dot clock frequency)

2) Two pixels per shift clock (where shift clock frequency = dot clock frequency / 2)
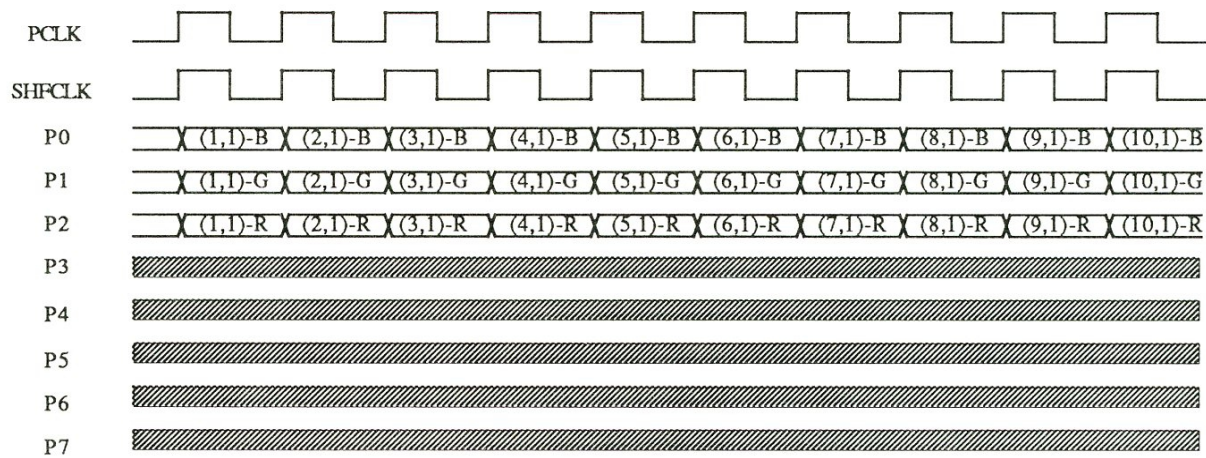
CD=00, MCP=00, PWM=00 3-BIT COLOR SINGLE DRIVE
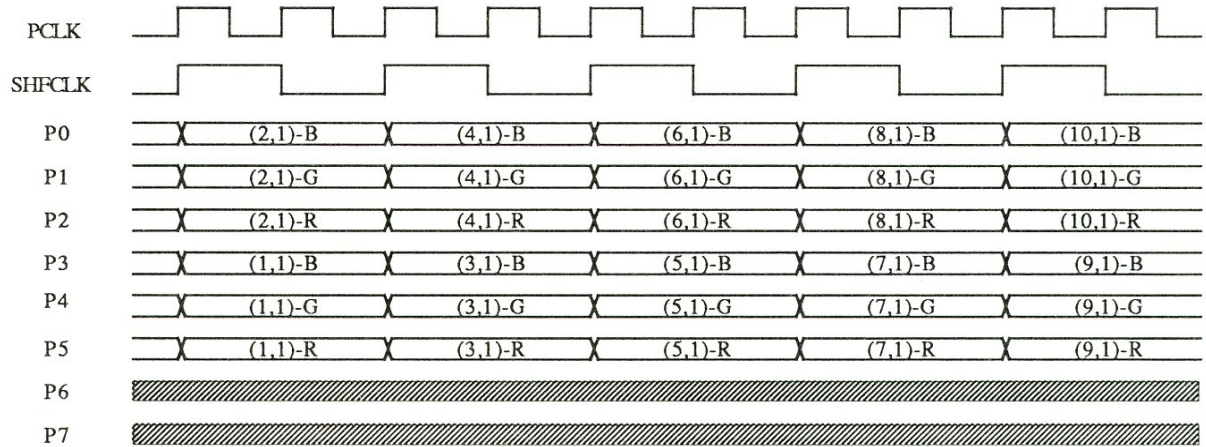
CD=01, MCP=00, PWM=00 3-BIT COLOR SINGLE DRIVE

82C455 Panel Pixel Timing - Color Single Drive 3-Bit (Clock Divide 00 & 01)

These timing diagrams show the 82C455 outputs for a single drive 3-bit color panel with no internal PWM generation. Two scenarios are presented:

1) One pixel per shift clock (where shift clock frequency = dot clock frequency)

2) Two pixels per shift clock (where shift clock frequency = dot clock frequency / 2)

PCLK	
SHFCLK	
P0	(1,1)-B (2,1)-B (3,1)-B (4,1)-B (5,1)-B (6,1)-B (7,1)-B (8,1)-B (9,1)-B (10,1)-B
P1	(1,1)-G (2,1)-G (3,1)-G (4,1)-G (5,1)-G (6,1)-G (7,1)-G (8,1)-G (9,1)-G (10,1)-G
P2	(1,1)-R (2,1)-R (3,1)-R (4,1)-R (5,1)-R (6,1)-R (7,1)-R (8,1)-R (9,1)-R (10,1)-R
P3	(1,1)-Bs (2,1)-B (3,1)-Bs (4,1)-Bs (5,1)-Bs (6,1)-Bs (7,1)-Bs (8,1)-Bs (9,1)-Bs (10,1)-Bs
P4	(1,1)-Gs (2,1)-Gs (3,1)-Gs (4,1)-Gs (5,1)-Gs (6,1)-Gs (7,1)-Gs (8,1)-Gs (9,1)-Gs (10,1)-Gs
P5	(1,1)-Rs (2,1)-Rs (3,1)-Rs (4,1)-Rs (5,1)-Rs (6,1)-Rs (7,1)-Rs (8,1)-Rs (9,1)-Rs (10,1)-Rs
P6	
P7	

CD=00, MCP=00, PWM=01   3-BIT COLOR SINGLE DRIVE

82C455 Panel Pixel Timing - Color Single Drive 4-Level PWM

This timing diagram shows the 82C455 outputs for a single drive 3-bit color panel with 4-level internal PWM and a one pixel per shift clock interface.

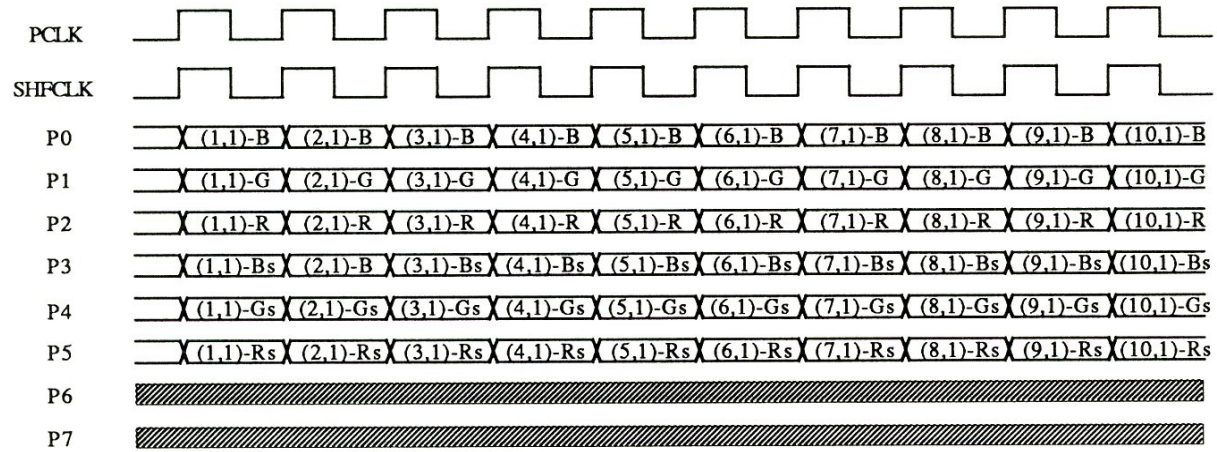CD=00, MCP=01, PWM=00   4-BIT PACK COLOR SINGLE DRIVE

CD=00, MCP=01, PWM=01   4-BIT PACK COLOR SINGLE DRIVE
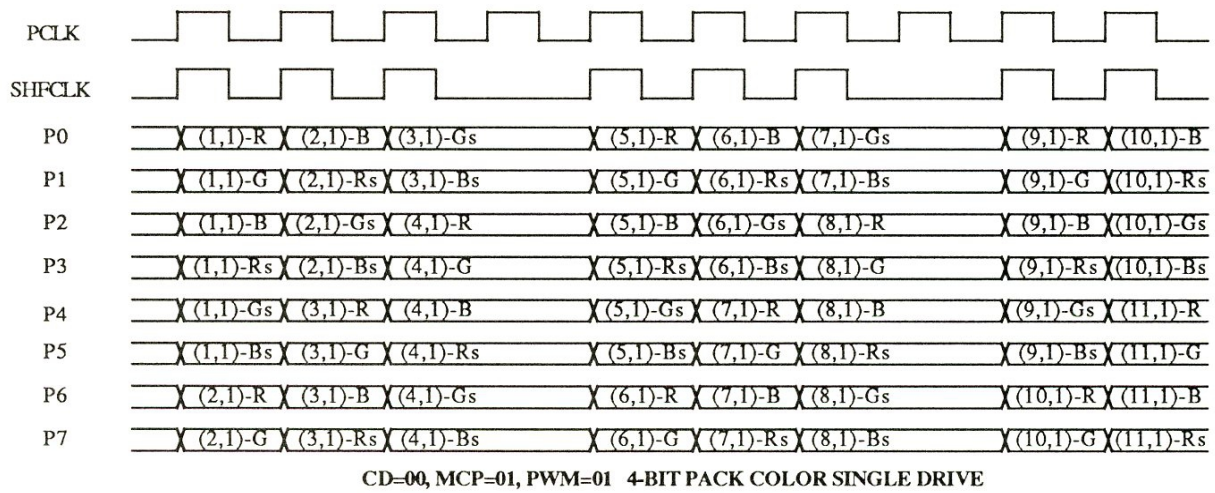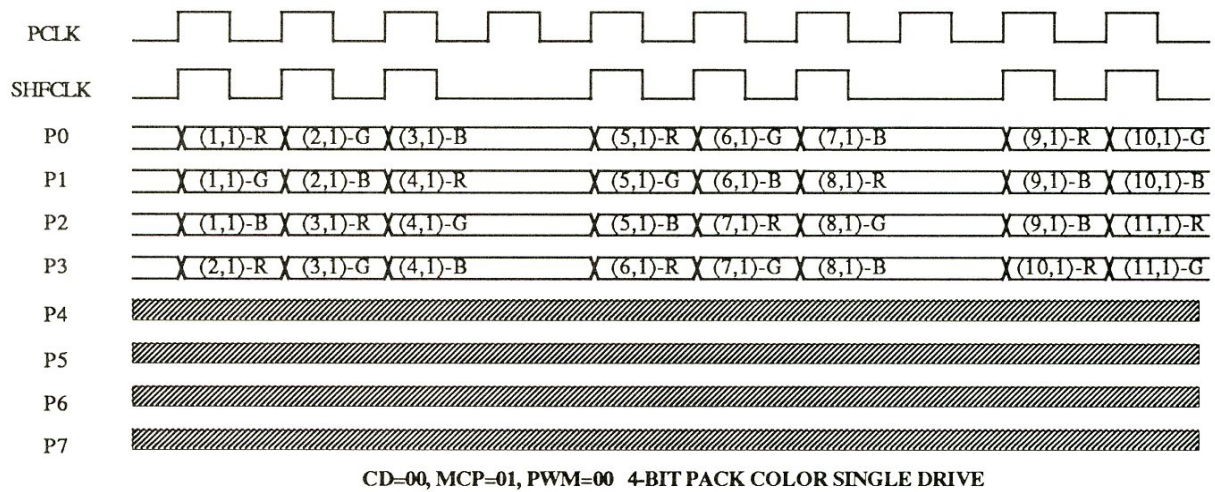
82C455 Panel Pixel Timing - Color Single Drive 4-Bit Pack (PWM 0 & 1)

These timing diagrams show the 82C455 outputs for a single drive 4-bit pack color panel with a one pixel per shift clock interface for two cases:

1) No internal PWM supported by the panel

2) 4 levels of PWM supported by the panel

PCLK

SHFCLK

P3	(4,1)
P2	(3,1)
P1	(2,1)
P0	(1,1)
P7	(4,241)
P6	(3,241)
P5	(2,241)
P4	(1,241)
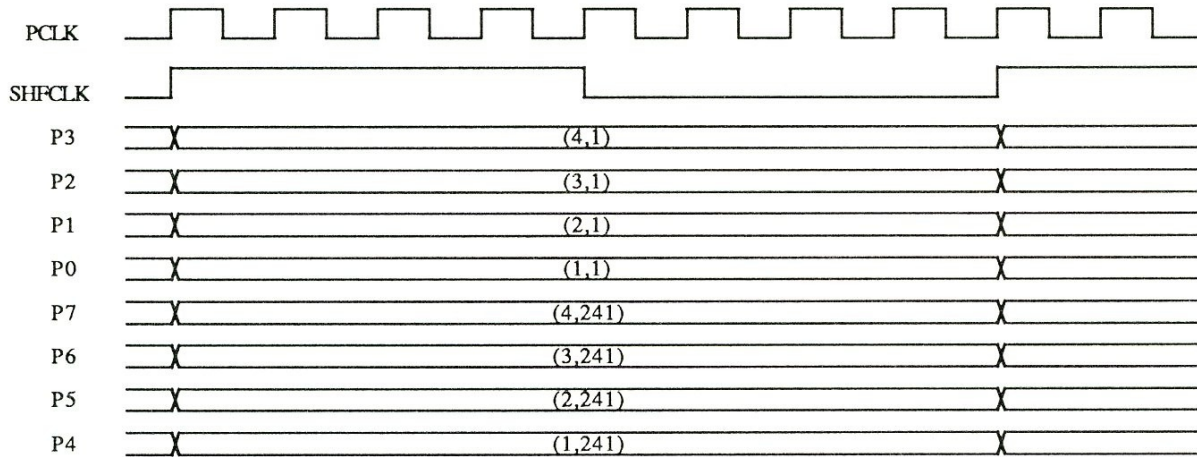
CD=11, MCP=10, PWM=00   DOUBLE DRIVE

82C455 Panel Pixel Timing - Monochrome Double Drive (Clock Divide By 8)

This timing diagram shows the 82C455 outputs for a double drive monochrome panel with an eight pixels per shift clock interface where the shift clock frequency equals the dot clock frequency divided by 8.

82C455 Electrical Specifications

82C455 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Units
P_D	Power Dissipation	–	1	W
V_{CC}	Supply Voltage	–0.5	7	V
V_I	Input Voltage	–0.5	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	85	°C
T_{STG}	Storage Temperature	–40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C455 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
T_A	Ambient Temperature	0	70	°C
T_C	Case Temperature	0	85	°C

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

82C455 DC CHARACTERISTICS

(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC1}	Power Supply Current	Normal @ 25 MHz CLK, 0°C	–	100	mA
I_{CC2}	Power Supply Current	(Retire Mode @ 25 MHz CLK, 0°C)	–	10	mA
I_{IL}	Input Leakage Current		–10	+10	uA
I_{OZ}	Output Leakage Current	High Impedance	–10	+10	uA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage	(All pins except clocks)	2.0	V_{CC}+0.5	V
		(CLK0, CLK1, CLK2, MCLK)	2.8	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = -8 mA (RDY,IRQ,TRAP/, ERMEN/, IOCS16/)	–	0.5	V
		I_{OL} = -4 mA (all others)	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –8 mA (RDY,IRQ,TRAP/, ERMEN/, IOCS16/)	2.4	–	V
		I_{OH} = –4 mA (all others)	2.4	–	V

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

82C455 AC TIMING CHARACTERISTICS - CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	CLKIN Period (Flat Panel)	32 MHz	31	–	–	nS
T_C	CLKIN Period (CRT)	40 MHz	25	–	–	nS
T_{CH}	CLKIN High Time		$0.45T_C$	–	$0.55T_C$	nS
T_{CL}	CLKIN Low Time		$0.45T_C$	–	$0.55T_C$	nS
T_M	MCLKPeriod	25 - 33 MHz (Note 1)	30	–	40	nS
T_{MH}	MCLK High Time		$0.45T_M$	–	$0.55T_M$	nS
T_{ML}	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	nS
T_{rf}	CLK Rise/Fall		–	–	5	nS
	CLKIN Freq. for 120 nS DRAM	Note 2	–	–	30	MHz
	CLKIN Freq. for 100 nS DRAM	Note 3	–	–	33	MHz
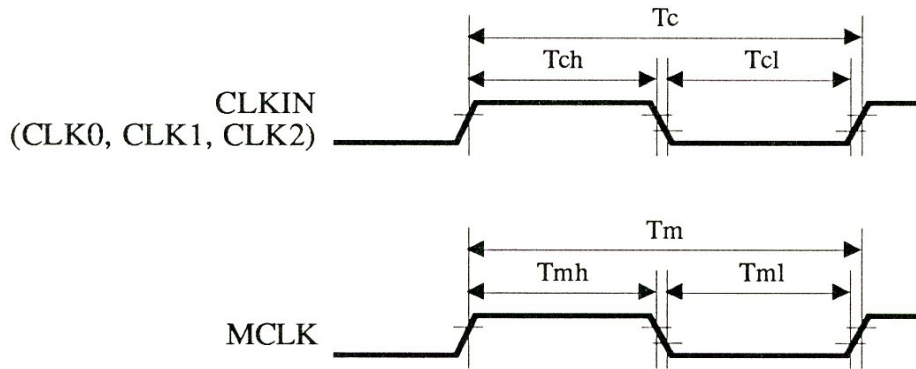
Note 1: The minimum MCLK frequency is required for an MCA bus CPU speedof 16MHz or a PC/AT bus speed of 8MHz. A faster system will require a faster MCLK.

Note 2: A maximum clock input of 30 Mhz is allowed for most 120 ns DRAMs. If the DRAMs have less than typical RAS precharge and RAS cycle requirement, 150 ns DRAMs may be used with clock inputs up to 28.322 Mhz.

Note 3: A maximum clock input of 33 Mhz is allowed for most 100 ns DRAMs. If the DRAMs have a less than typical RAS precharge requirement, clock speeds to 40 Mhz may be used with 100 ns DRAMs.

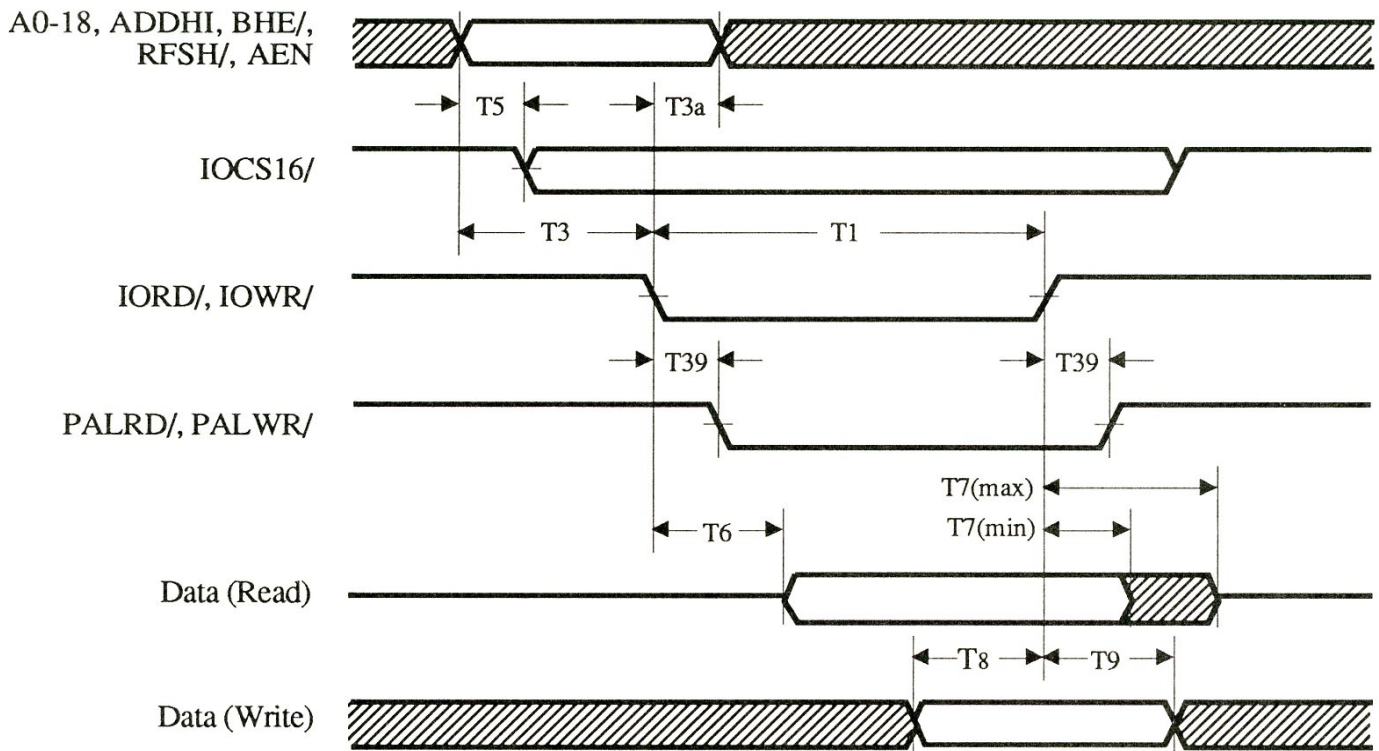## 82C455 AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
–	RESET Pulse Width		64 T_C	–	–	nS

82C455 AC TIMING CHARACTERISTICS - ISA (PC/AT) Bus Timing

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_1	IORD/, IOWR/ Pulse Width	4 & 5	175	–	–	nS
T_2	MEMR/, MEMW/ Pulse Width	5	175	–	–	nS
T_3	Address setup to Read/Write		80	–	–	nS
T_{3a}	Address hold from Read/Write Signal		20	–	–	nS
T_5	IOCS16/ Delay from valid address		–	–	35	nS
T_4	MEMR/, MEMW/ hold from RDY (Memory)		0	–	–	nS
T_6	I/O Read Data delay from IORD/		–	–	50	nS
T_7	I/O Read Data hold from IORD/		5	–	40	nS
T_8	I/O Write Data setup to IOWR/		40	–	–	nS
T_9	I/O Write Data hold from IOWR/		10	–	–	nS
T_{10}	Memory Read Data hold from MEMR/		5	–	40	nS
T_{11}	Memory Write Data hold from MEMW/		0	–	–	nS
T_{12}	MEMR/, MEMW/ to RDY Low delay		–	–	25	nS
T_{13}	Memory Read Data setup to RDY		25	–	–	nS
T_{14}	Memory Write Data setup to RDY		40	–	–	nS
T_{15}	RDY width		$7T_C$	–	$128T_C$	nS
T_{39}	PALRD/, PALWR/ delay from Read/Write		–	–	25	nS

Note 4: A minimum IOWR pulse width of 3 MCLKs is required for access to an indexed register (ie. SR, CR, AR, GR, XR.)

Note 5: A minimum of 6 MCLKs is required from the falling edge of IOWR to the falling edge of MEMR/ or MEMW/.
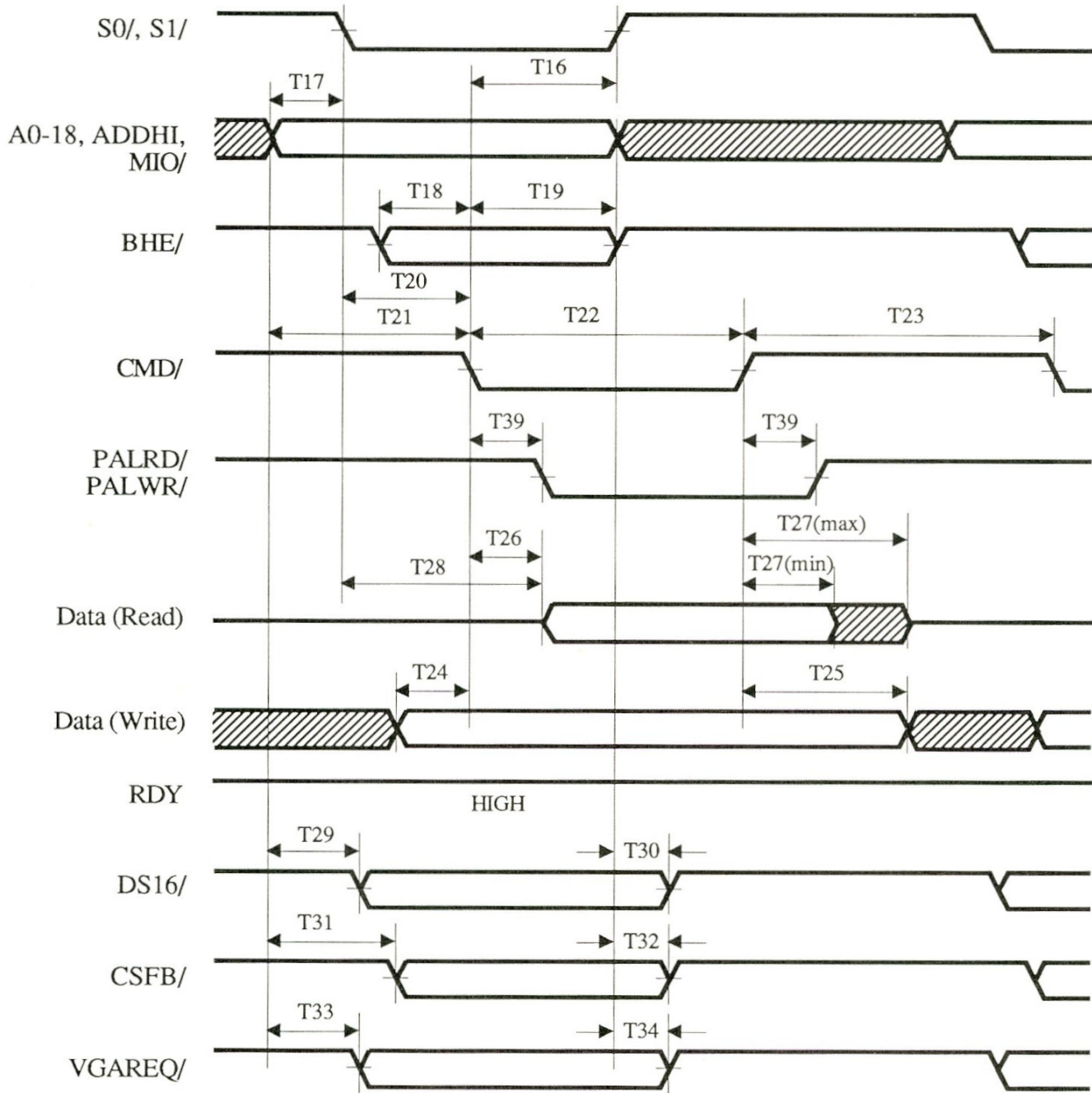
ISA (PC/AT) Bus I/O Cycle Timing
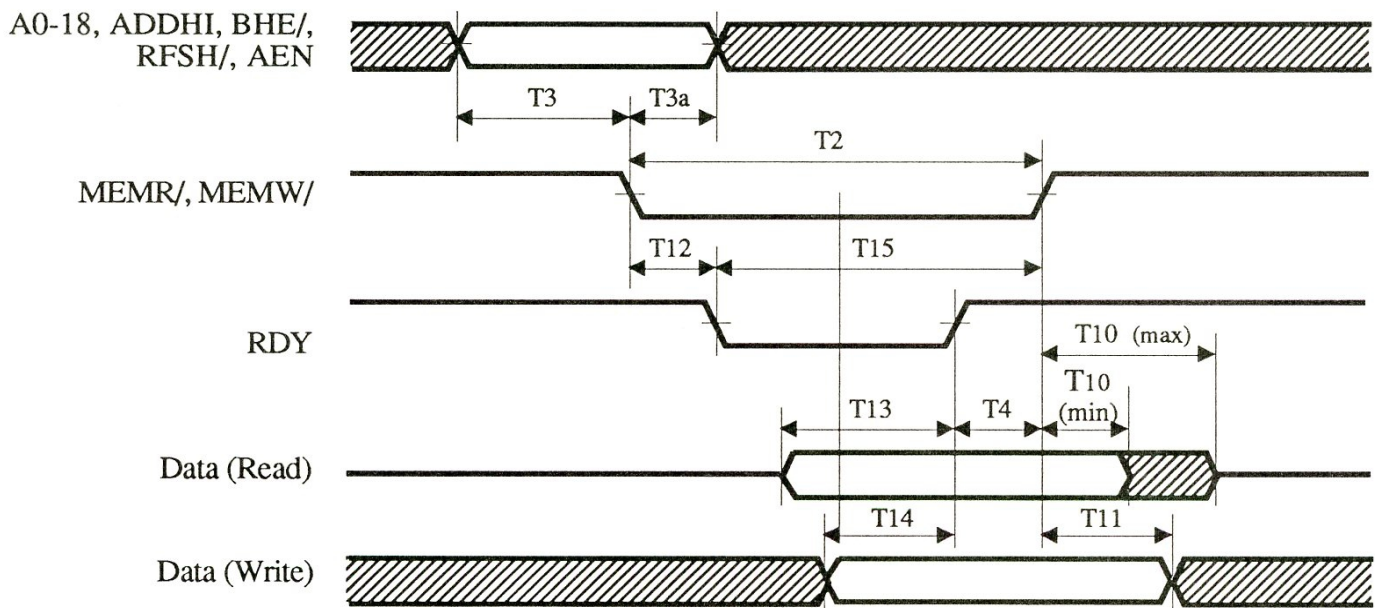
ISA (PC/AT) Bus Memory Cycle Timing

82C455 AC TIMING CHARACTERISTICS - MCA BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{16}	Status hold from CMD/		20	–	–	nS
T_{17}	Status active from address valid		0	–	–	nS
T_{18}	BHE/ Setup to CMD/		30	–	–	nS
T_{19}	Address , BHE/ hold from CMD/		20	–	–	nS
T_{20}	CMD/ active from Status		45	–	–	nS
T_{21}	CMD/ from address valid		80	–	–	nS
T_{22}	CMD/ Pulse Width		80	–	–	nS
T_{23}	CMD/ inactive to next CMD/		80	–	–	nS
T_{24}	Write data setup to CMD/		0	–	–	nS
T_{25}	Write data hold from CMD/		10	–	–	nS
T_{26}	Read data valid from CMD/		–	–	50	nS
T_{27}	Read data hold from CMD/		5	–	40	nS
T_{28}	Status to Read data valid		–	–	125	nS
T_{29}	DS16/ active from address valid		–	–	25	nS
T_{30}	DS16/ inactive from Status		5	–	25	nS
T_{31}	CSFB/ active from address valid		–	–	25	nS
T_{32}	CSFB/ inactive from Status		5	–	25	nS
T_{33}	VGA REQ/active frrom address valid		–	–	25	nS
T_{34}	VGA REQ/ inactive from Status		5	–	25	nS
T_{35}	RDY active from CMD/ high		65	–	–	nS
T_{36}	Read data from RDY active (high)		–	–	50	nS
T_{37}	RDY inactive (low) from Status		–	–	25	nS
T_{38}	Write data setup to RDY active (high)		–	–	40	nS
T_{39}	PAL RD/, PALWR/ delay from CMD/		–	–	25	nS

MCA Bus I/O Cycle Timing
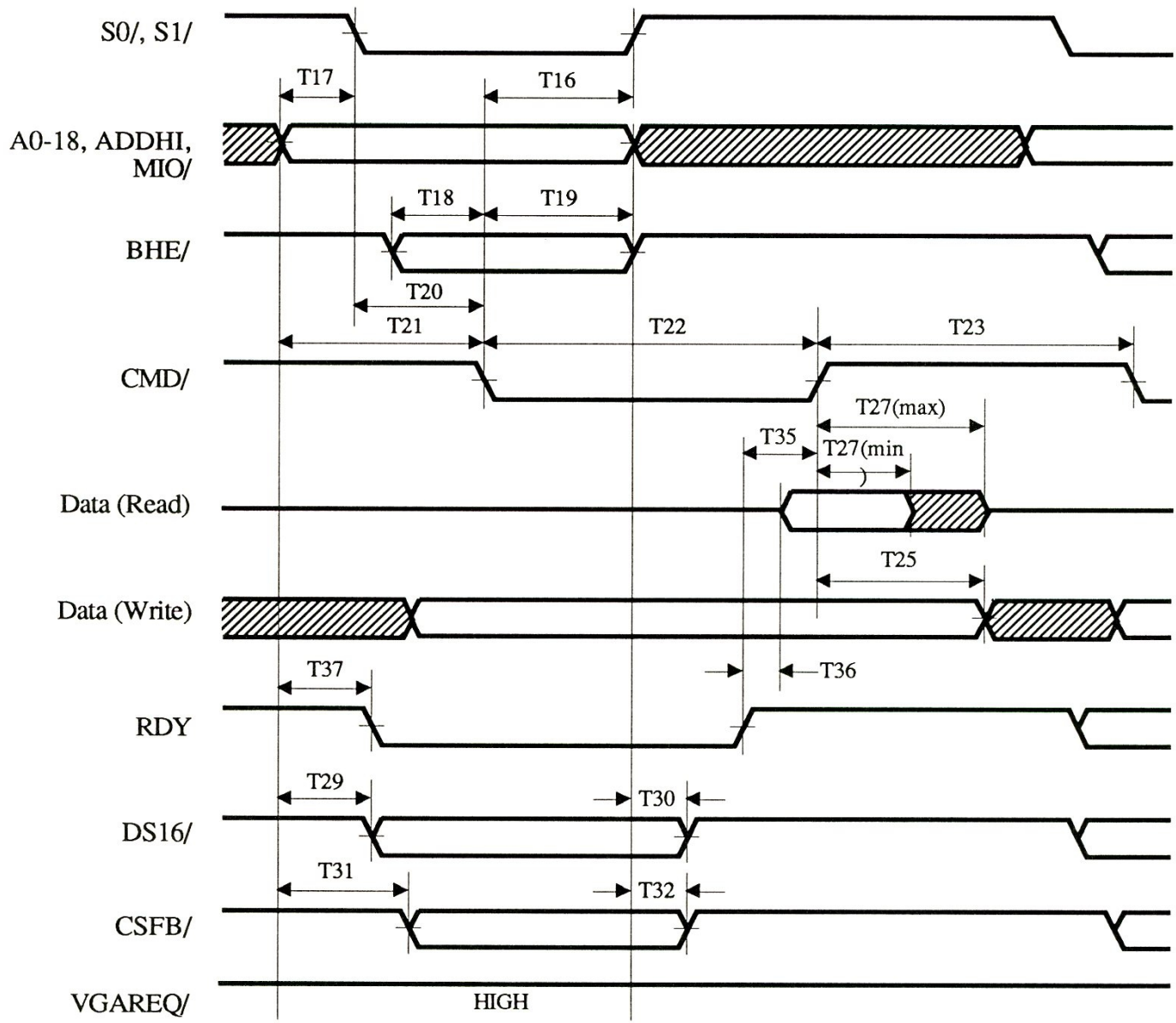
MCA Bus Memory Cycle Timing

82C455 AC TIMING CHARACTERISTICS - DRAM TIMING

Symbol	Parameter	8-dot Mode		9-dot Mode		Units
		Min	Max	Min	Max	
T_{rc}	Read/Write Cycle Time	$7T_C - 1$	–	$8T_C - 1$	–	nS
T_{ras}	RAS/ Pulse Width	$4T_C - 5$	–	$4T_C - 5$	–	nS
T_{ar}	Column Address Hold from RAS/	$5T_C - 5$	–	$5T_C - 5$	–	nS
T_{rp}	RAS/ Precharge	$3T_C$	–	$4T_C$	–	nS
T_{crp}	CAS/ to RAS/ precharge	$1T_C - 1$	–	$2T_C - 1$	–	nS
T_{csh}	CAS/ Hold from RAS/	$6T_C - 7$	–	$6T_C - 7$	–	nS
T_{rcd}	RAS/ to CAS/ delay	$2T_C - 3$	–	$2T_C - 3$	–	nS
T_{rsh}	RAS/ Hold from CAS/	$2T_C - 4$	–	$2T_C - 4$	–	nS
T_{cpn}	CAS/ Precharge	$3T_C$	–	$4T_C$	–	nS
T_{cas}	CAS/ Pulse Width	$4T_C - 5$	–	$4T_C - 5$	–	nS
T_{asr}	Row Address Setup to RAS/	$2T_C - 5$	–	$3T_C - 5$	–	nS
T_{asc}	Column Address Setup to CAS/	$1T_C - 5$	–	$1T_C - 5$	–	nS
T_{rah}	Row Address Hold from RAS/	$1T_C$	–	$1T_C$	–	nS
T_{cah}	Column Address Hold from CAS/	$3T_C - 3$	–	$3T_C - 3$	–	nS
T_{cac}	Data Access Time from CAS/	–	$3T_C$	–	$3T_C$	nS
T_{rac}	Data Access Time from RAS/	–	$5T_C$	–	$5T_C$	nS
T_{wp}	WE/ Pulse Width	$7T_C - 6$	–	$8T_C - 6$	–	nS
T_{ds}	Write Data Setup to CAS/	$2T_C - 4$	–	$2T_C - 4$	–	nS
T_{dh}	Write Data Hold from CAS/	$5T_C - 2$	–	$6T_C - 2$	–	nS
T_{dhr}	Write Data Hold from RAS/	$7T_C - 5$	–	$8T_C - 5$	–	nS
T_{wch}	WE/ Hold from CAS/	$5T_C - 4$	–	$6T_C - 4$	–	nS
T_{wcs}	WE/ Setup to CAS/	$2T_C - 5$	–	$2T_C - 5$	–	nS
T_{rwl}	WE/ Lead to RAS/	$4T_C - 7$	–	$4T_C - 7$	–	nS
T_{cwl}	WE/ Lead to CAS/	$6T_C - 8$	–	$6T_C - 8$	–	nS
T_{wcr}	WE/ Hold from RAS/	$7T_C - 6$	–	$8T_C - 6$	–	nS

82C455 AC TIMING CHARACTERISTICS - DRAM REFRESH TIMING

Symbol	Parameter	Max	Units
–	DRAM Refresh interval	85000/(VR*VL)	nS

Note: VR = Vertical refresh rate (in Hz.)
VL = Total number of lines per frame (including retrace)

ERMEN/ (Note 6)
Tc
Tc
Trc
Tras
Trp

RAS/
Tcsh

Tcrp
Trcd
Trsh
Tcpn
Tcas

CAS/
Tar

Tasr
Trah
Tasc
Tcah

Address
Row Address
Column Address
Row Address
Column Address

Trwl
Tcwl
Twcs
Twch
Twp

WE/ (Write)
Twcr
Tdhr
Tds
Tdh

Data (Write)
Data Out

WE/ (Read)
High
Tcac
Trac

Data (Read)
Data In
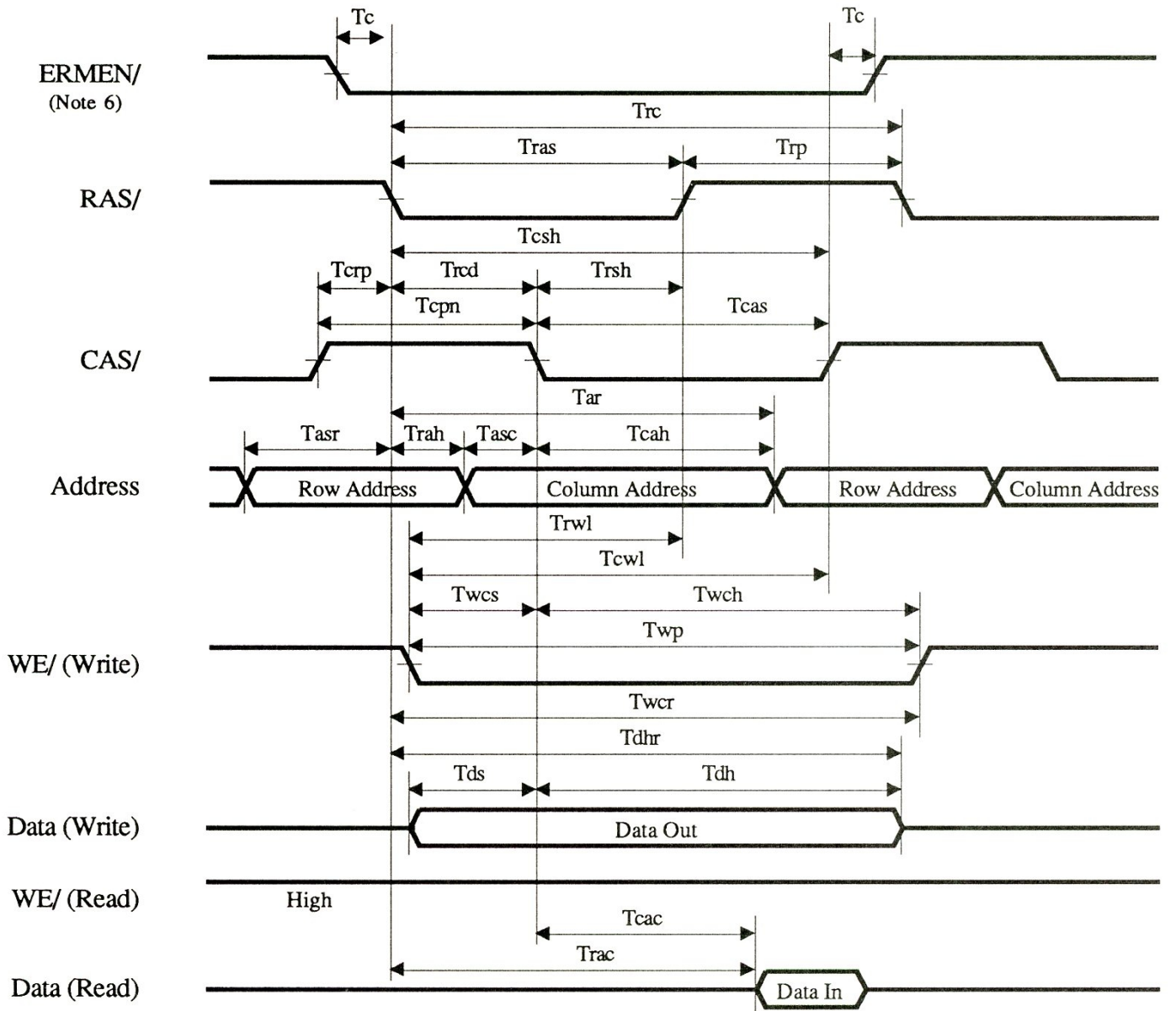
Note 6: ERMEN/ is active (low) only during CPU memory cycles

DRAM Read / Write Cycle Timing

RAS/

CAS/

Address

WE/

Data

Trc

Tras

Trp

High

Tasr

Trah

Refresh Address

Row Address

High

High Impedance
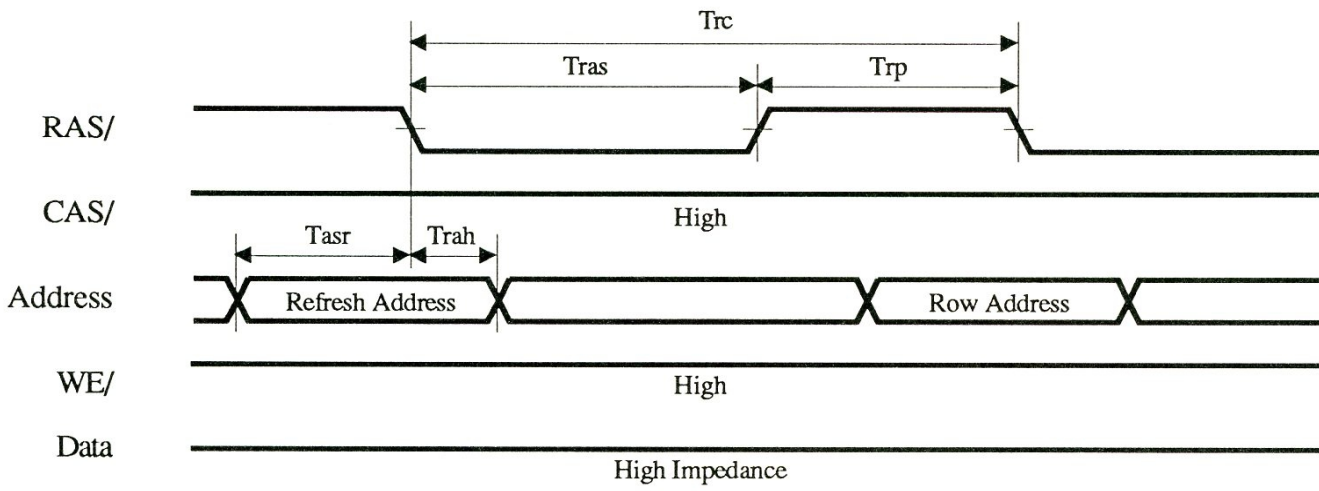
DRAM Refresh Cycle Timing

82C455 AC TIMING CHARACTERISTICS - VIDEO TIMING

Symbol	Parameter	Min	Max	Units
T_{cd}	CLKIN to PCLK Delay	–	25	nS
T_{syn}	SYNC and VIDEO CONTROL delay from PCLK	–	25	nS
T_{vid}	Video delay from PCLK	–	25	nS
T_{shd}	CLKIN TO SHFCLK delay	–	30	nS
T_{hin}	HSYNC delay from SHFCLK	–	25	nS
T_{vin}	VSYNC delay from SHFCLK	–	25	nS
T_{ded}	DISPLAY ENABLE delay from SHFCLK	–	15	nS
T_{vid}	Video delay from SHFCLK	–	15	nS
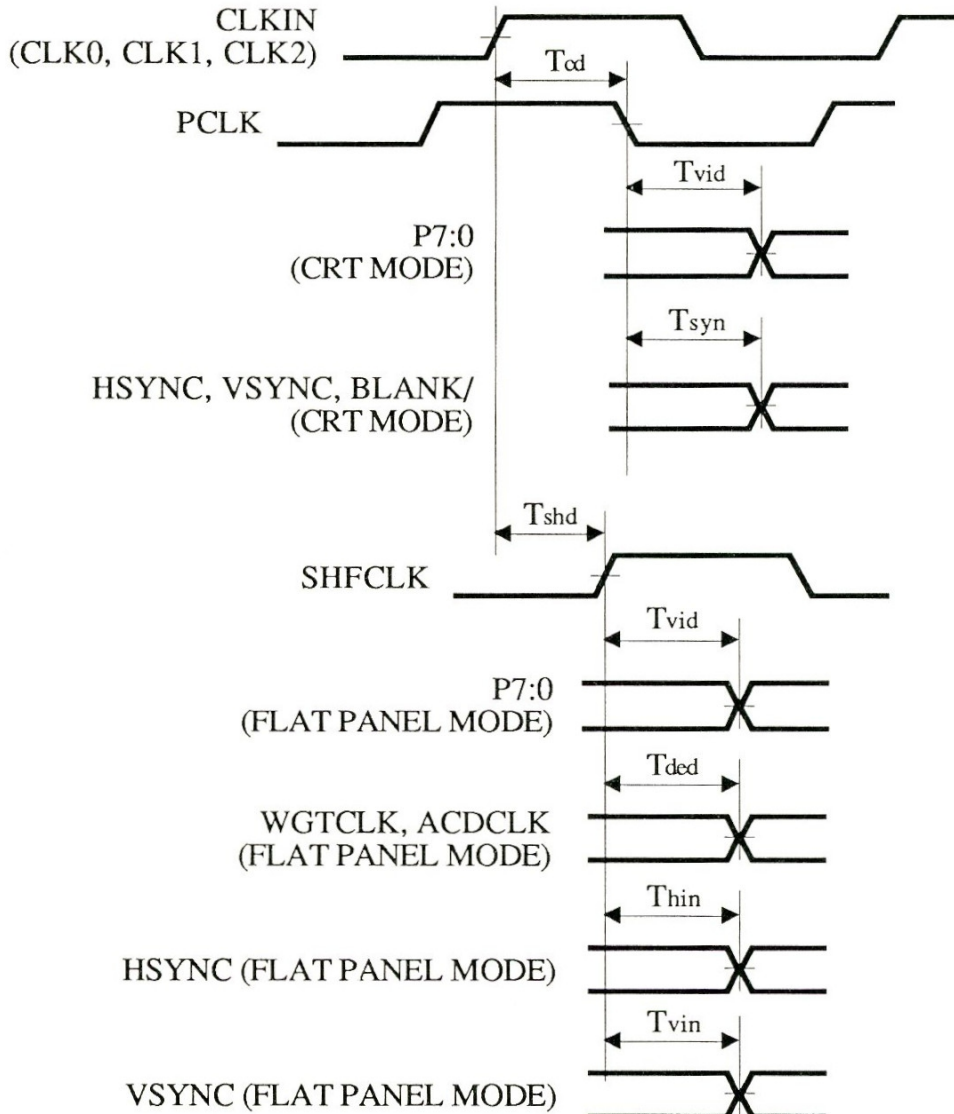
82C455 Mechanical Specifications:

Lead Pitch 0.65 (0.0256) Non-Accumulative

Lead Width 0.30 ±0.10 (0.012 ±0.004)

Lead Length See Note 2

Pin 1

CHIPS
144-Pin
Plastic Flat Pack

82C455

Footprint $\frac{30.5\ (1.201)}{32.4\ (1.276)}$ See Note 1

See Note 1

Footprint $\frac{30.5\ (1.201)}{32.4\ (1.276)}$

Lead Length See Note 2

DIMENSIONS: mm (in)

Clearance $\frac{0.000\ (0.000)}{0.406\ (0.016)}$

Max Height 4.26 (0.168)

Seating Plane
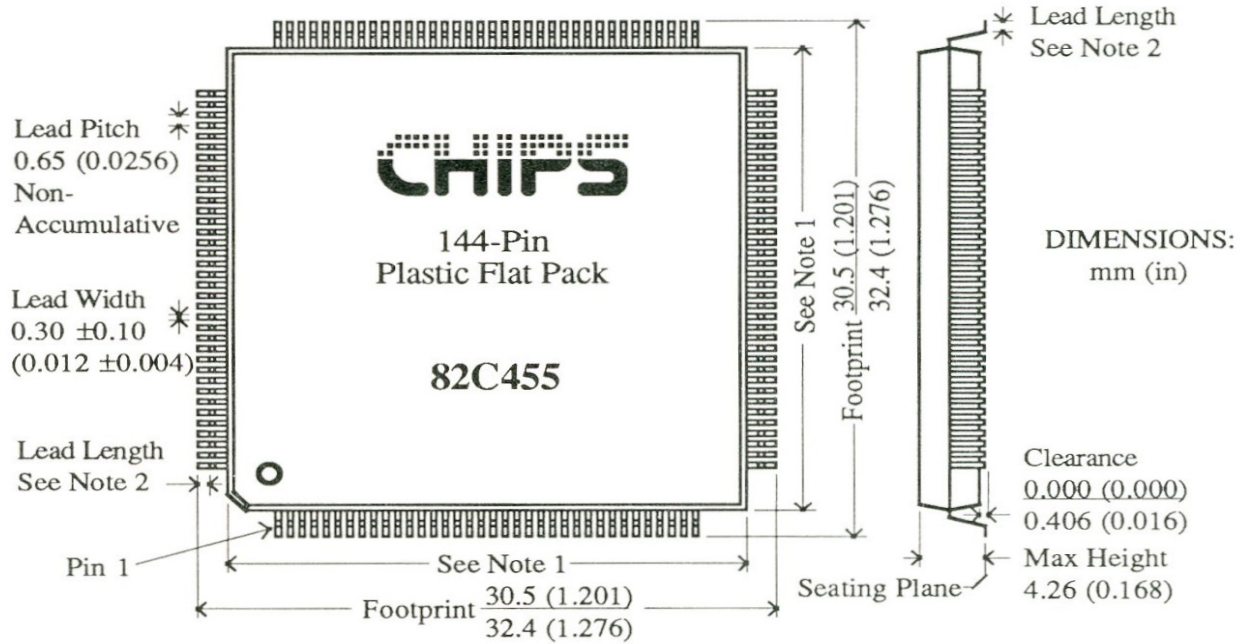
Note 1: Package Body Size = 26 ±0.2 (1.024 ±0.008)
Note 2: Lead Length = 1.2 ±0.2 (0.047 ±0.008)

82C455 Suggested PCB Pad Layout:

ABABAABABAABABAABABAABABAABABAABABAABABA

ABABAABABAABABAABABAABABA

144-Pin Plastic Flat Pack Suggested PCB Pad Layout

Pad Size = 2.54 mm x 0.30 mm (0.100 in x 0.012 in)

'A' Spacing = 0.65 mm (0.0256 or 0.026 in) (see note)
'B' Spacing = 0.65 mm (0.0256 or 0.025 in) (see note)

Note: If the PCB layout system to be used can handle fractional mils, use 0.0256 center-to-center spacing. If not, use a combination of 0.025 and 0.026 inch spacings as indicated ('ABABA' repeated) to approximate the exact spacing as closely as possible.

ABABAABABAABABAABABAABABA

Footprint 33.0 mm (1.300 in)

ABABAABABAABABAABABAABABAABABAABABAABABA

Footprint 33.0 mm (1.300 in)

Chips & Technologies 82C455, 82C456, and 82C457 Related Document Files

(Extracted)
- 82C456 Datasheet
- 82C457 Datasheet
- Development History of 82C455, 82C456, and 82C457