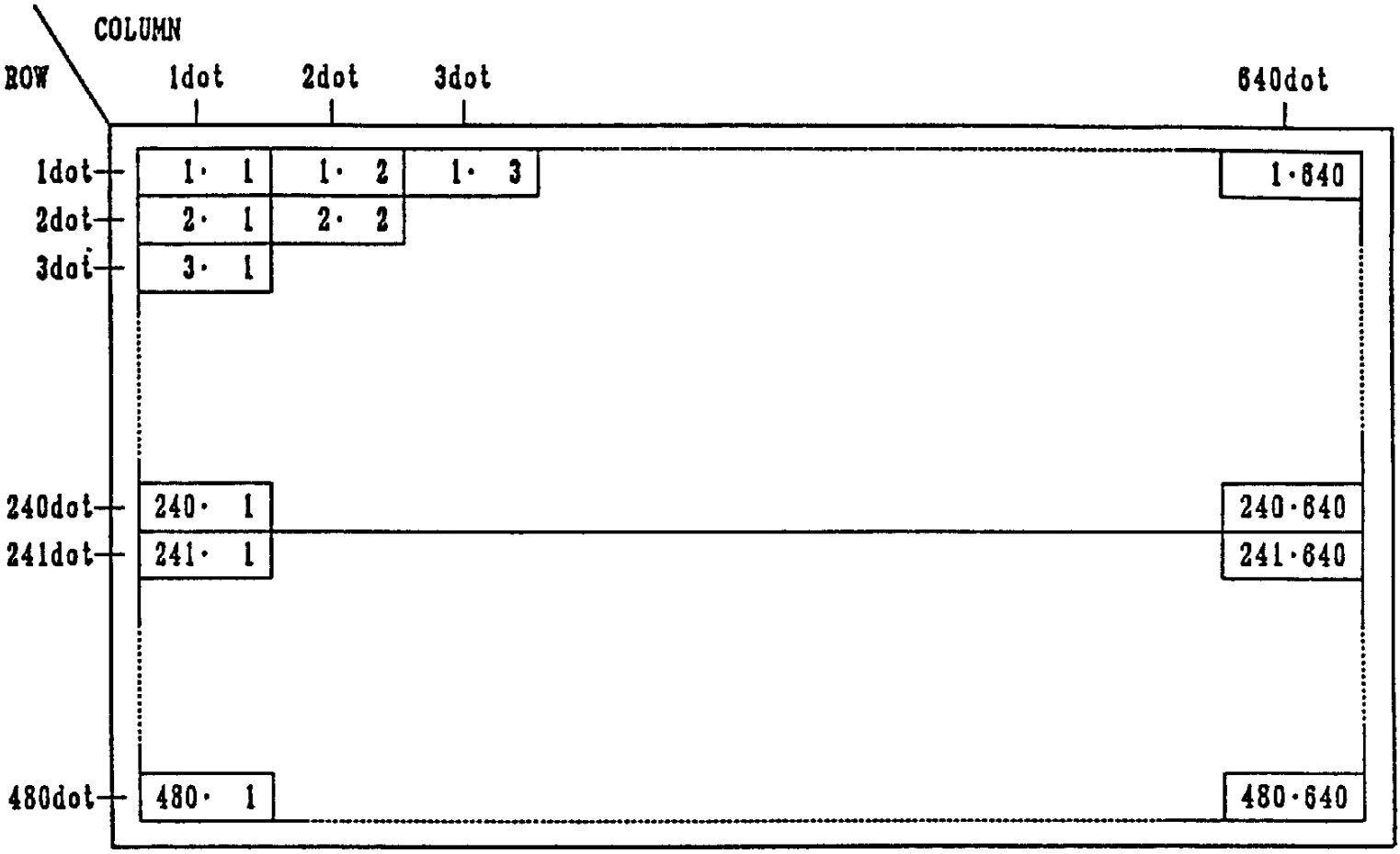
Sharp 640 x 480 DD (Dual panel, Double drive) STN (Super Twisted Nematic) panel specification
(extracted)

○LCD

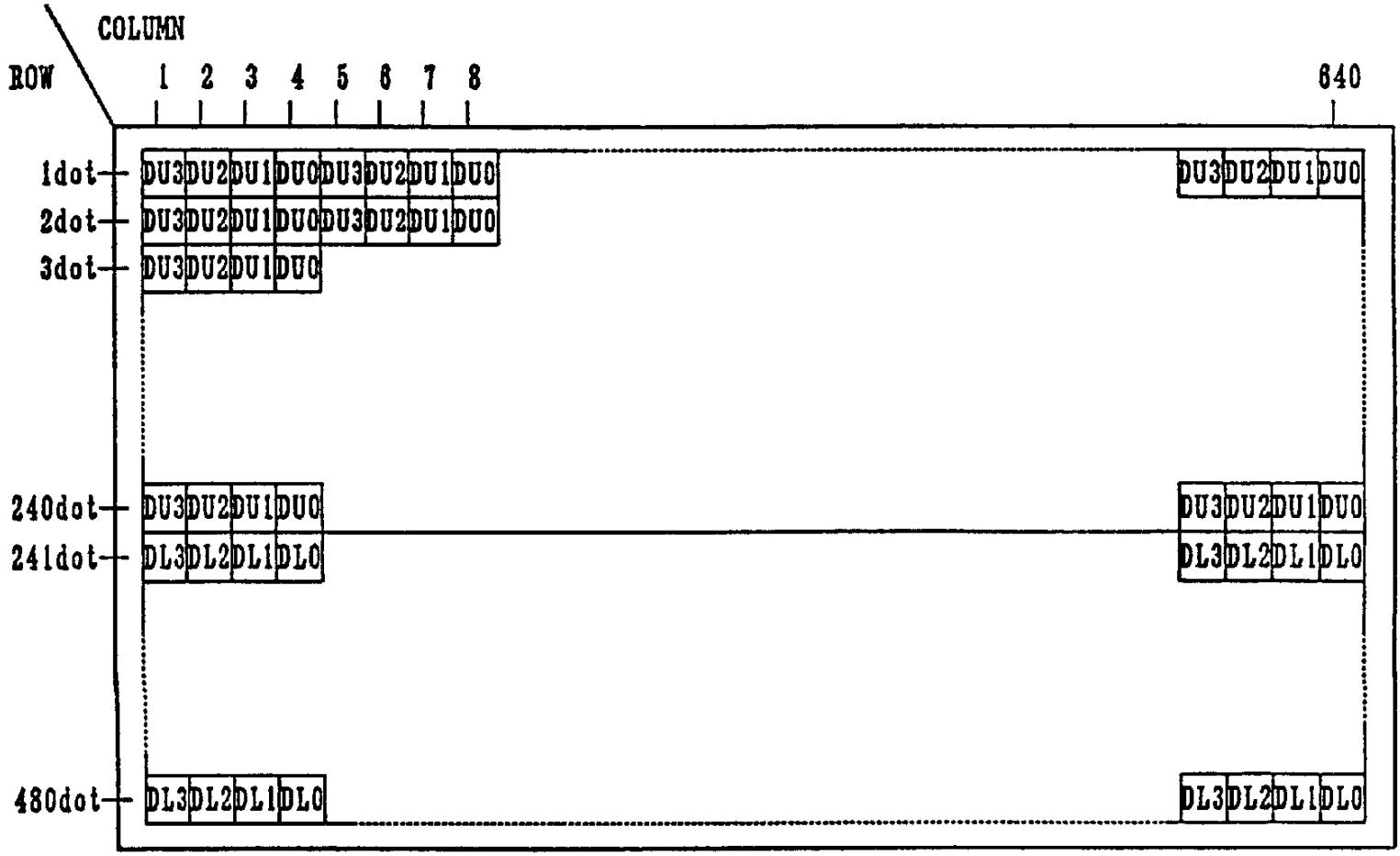
Pin No	Symbol	Description	Level
1	S	Scan start-up signal	"H"
2	CP1	Input data latch signal	H→L
3	CP2	Data input clock signal	H→L
4	DISP	Display control signal	Display on .."H" off.."L"
5	VDD	Power supply for logic and LCD (+5V)	
6	VSS	Ground potential	
7	VEE	Power supply for LCD (-)	
8	DU0	Display data signal (Upper half)	H (ON), L (OFF)
9	DU1		
10	DU2		
11	DU3		
12	DL0	Display data signal (Lower half)	H (ON), L (OFF)
13	DL1		
14	DL2		
15	DL3		

○CCFT

Pin No	Symbol	Description	Level
1	GND	Ground line (from Inverter)	-
2	NC	-	-
3	NC	-	-
4	HV	High voltage line (from Inverter)	-



Note) 1·2 means 1st row 2nd column dot.



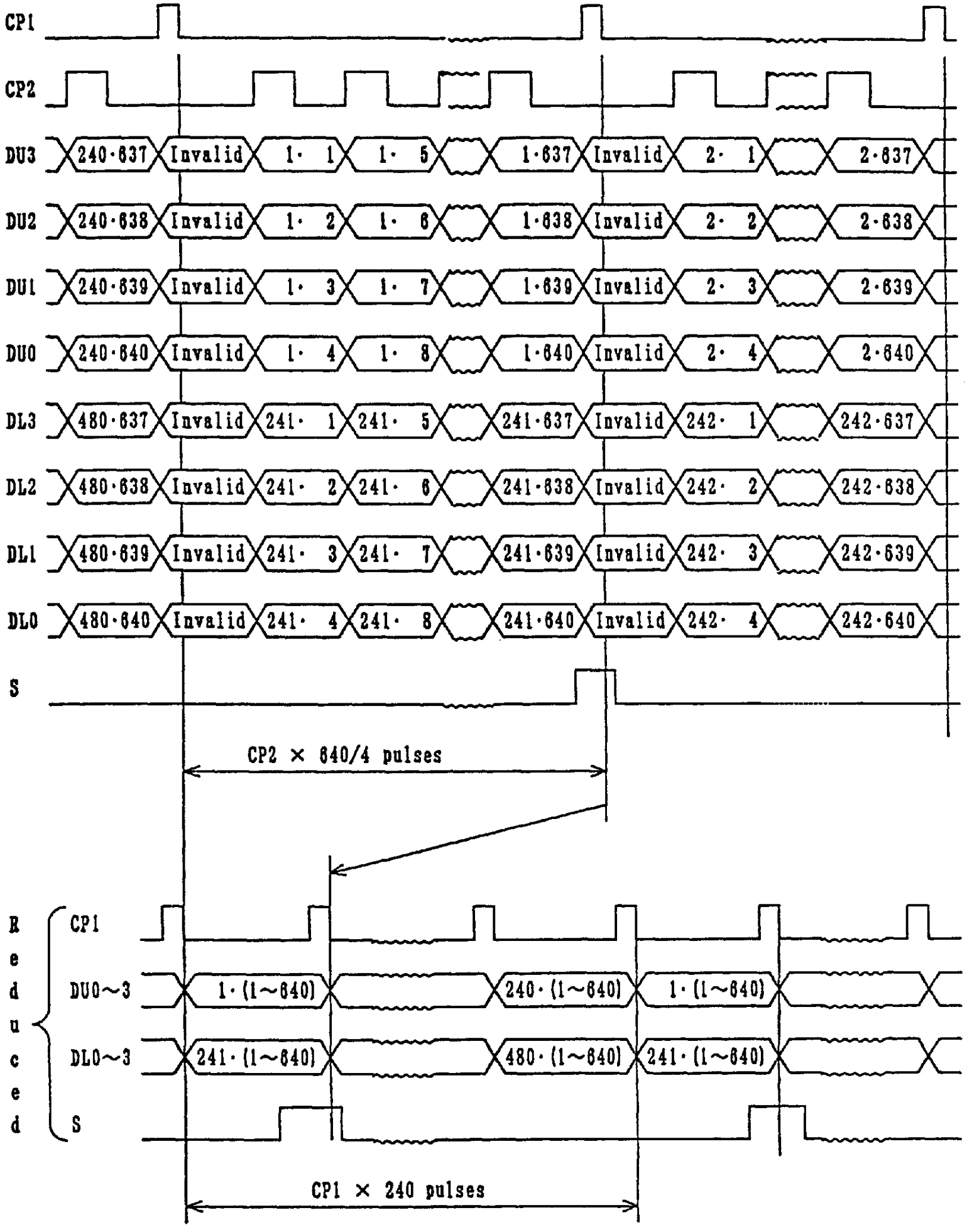
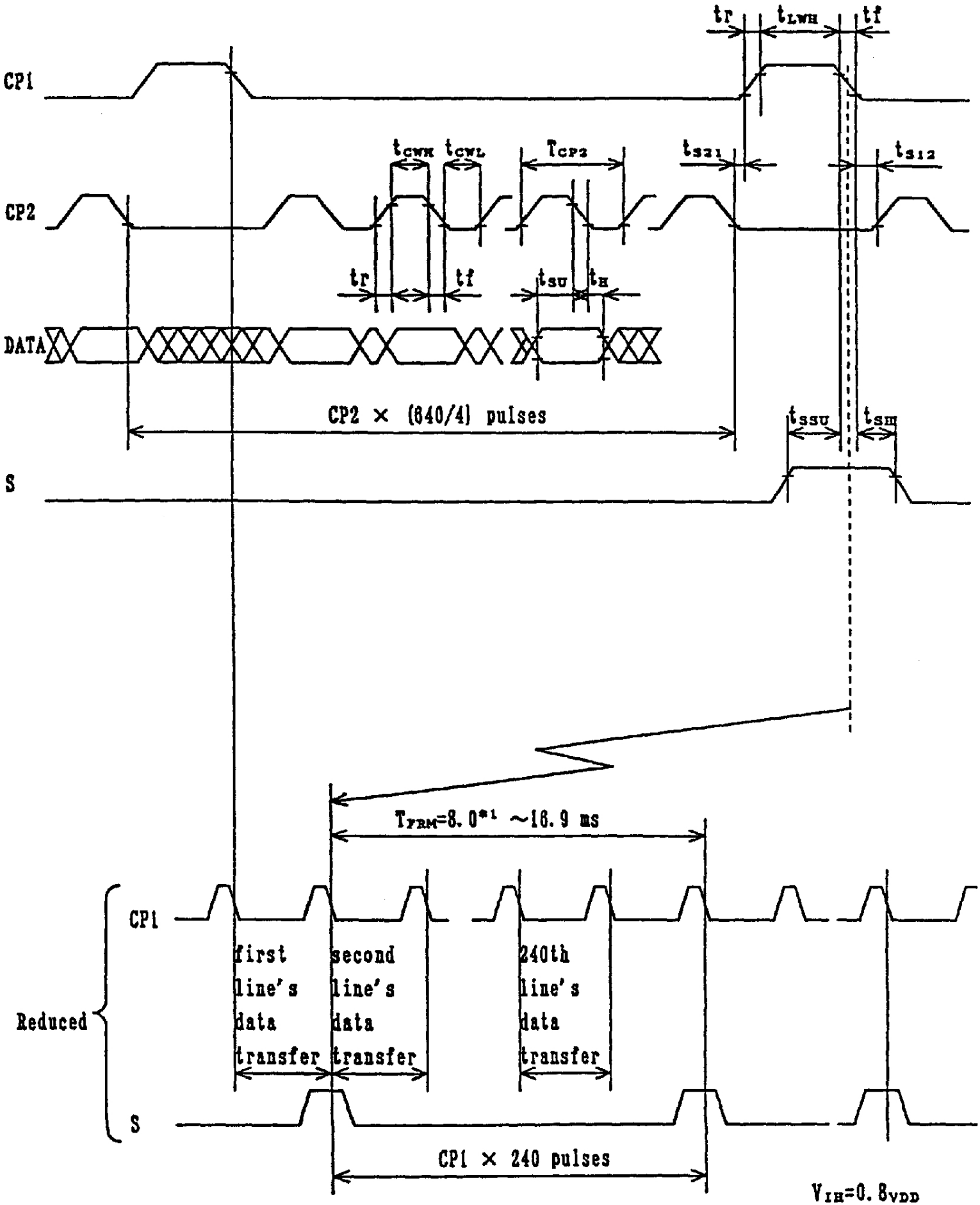


Fig. 2 Data input timing



*1 See table 7

Fig. 3 Interface timing chart

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle	T_{FRM}	8.0*1		16.9	ms
CP2 clock cycle	T_{CP2}	152			ns
'H' level clock width	t_{CWH}	65			ns
'L' level clock width	t_{CWL}	65			ns
'H' level latch clock width	t_{LWH}	70			ns
Data set up time	t_{SU}	50			ns
Data hold time	t_H	40			ns
S set up time	t_{SSU}	100			ns
S hold time	t_{SH}	100			ns
CP2↑ clock allowance time from CP1↓	t_{S21}	0			ns
CP1↑ clock allowance time from CP2↓	t_{S12}	0			ns
Clock rise/fall time	tr, tf			t_{rf}*2	ns

*1 : LCD unit functions at the minimum frame cycle of 8 ms (Maximum frame frequency of 125Hz). Owing to the characteristics of LCD unit, 'shadowing' will become more eminent as frame frequency goes up, while flicker will be reduced.

According to our experiments, frame cycle of 11.7 ms Min. or frame frequency of 85 Hz Max. will demonstrate optimum display quality in terms of flicker and 'shadowing'. But since judgement of display quality is subjective and display quality such as 'shadowing' is pattern dependent, it is recommended that decision of frame cycle or frame frequency, to which power consumption of the LCD unit is propotional, be made based on your own through testing on the LCD unit with every possible patterns displayed on it.

*2 : $t_{rf} = 50$ in case $t_{CT}=(T_{CP2}-t_{CWH}-t_{CWL})/2 \geqq 50$

$t_{rf} = t_{CT}$ in case $t_{CT}=(T_{CP2}-t_{CWH}-t_{CWL})/2 < 50$

6. Unit Driving Method

6.1 Circuit configuration

Fig. 9 shows the block diagram of the Unit's circuitry.

6.2 Display Face Configuration

The display face electrically consists of two (upper and lower) display segments so that the unit may offer higher contrast by reducing drive duty ratio. Each display segment (640×240 dots) is driven at 1/240 duty ratio.

6.3 Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits.

Display data which are externally divided into data for each row (640dots) will be sequentially transferred in the form of 4-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

When data of one row (640dots) have been input, they will be latched in the form of parallel data for 640 lines of signal electrodes by latch signal CP1. Then the corresponding drive signal will be transmitted to the 640 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal S has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st rows of upper and lower half of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.

While the 1st rows of data are being displayed, the 2nd rows of data are entered. When 640 dots of data have been transferred then latched on the falling edge of CP1 clock, the display face proceeds to the 2nd rows of display.

Such data input will be repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing method. Then data input proceeds to the next display face.

Scan start-up signal S generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which will deteriorate LCD panel, drive waveform shall be inverted at every display frame to prevent the generation of such DC voltage. Control signal M plays such role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up as the operating frequency CP2 increases. Thus the driver LSI applies the system of tranferring 4-bits parallel data through the 4 lines of shift registers to reduce the data transfer speed CP2. Thanks to the LSI, the power consumption of the unit will be minimized.

In this circuit configuration, 4-bit display data shall be therefore input to data input pins of DU_{0-3} (upper display segment) and DL_{0-3} (lower display segment).

Furthermore the LCD unit adopts bus line system for data input to minimize the power consumption. In this system data input terminal of each driver LSI activated only when relevant data input is fed.

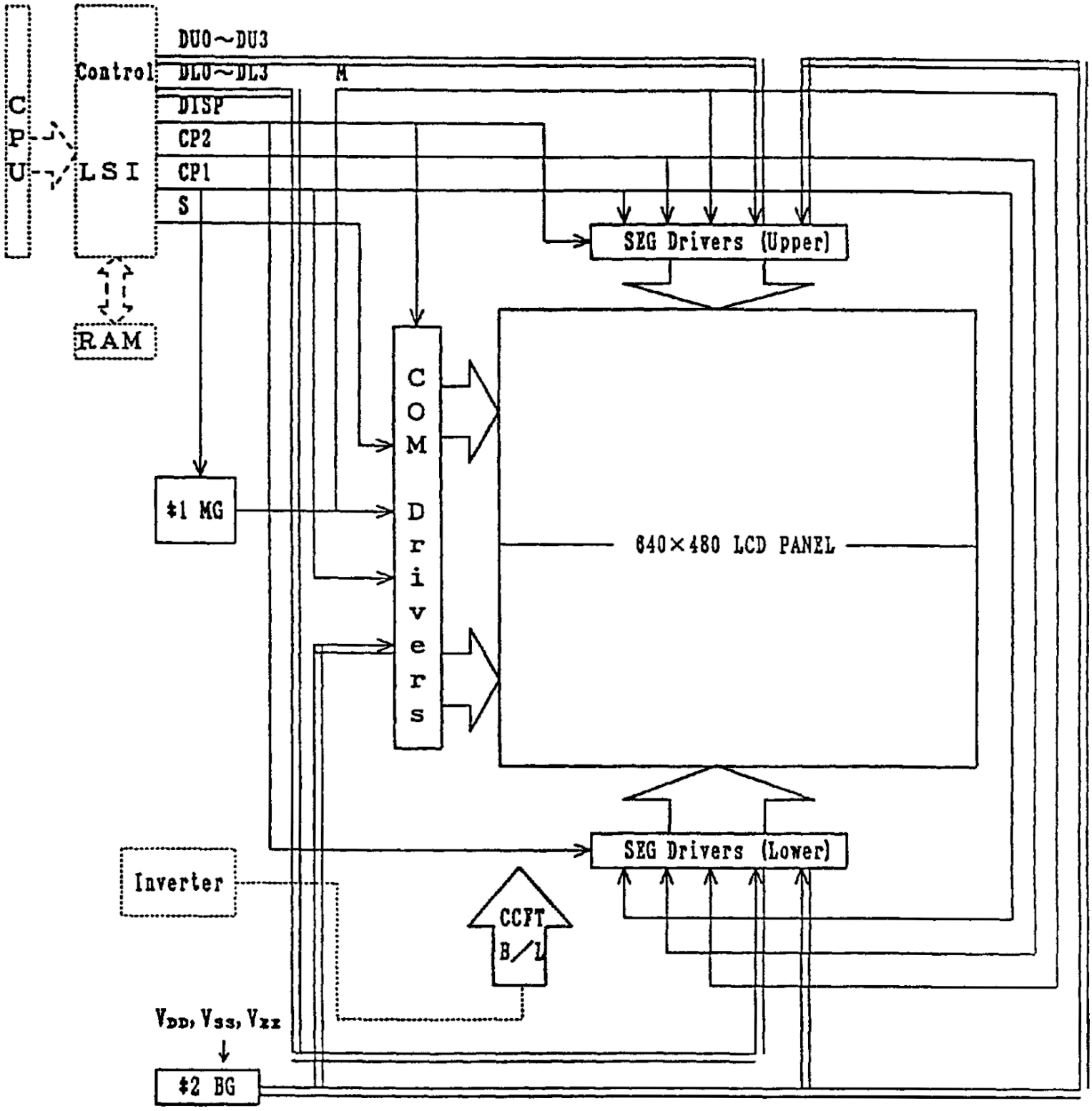
Data input for column electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This process is simultaneously followed at the column drivers LSI's of both the upper and the lower display segments. Thus data input for both the upper and the lower display segments must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no reflesh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig. 3 and Table 7.



#1 MG: M GENERATOR CIRCUIT

#2 BG: BIAS GENERATOR CIRCUIT

Fig. 9 Circuit block diagram